MAXIM

1988 Data Converters and Voltage References

Integrating A/D Converters
Successive Approximation A/D Converters
Half Flash A/D Converters
D/A Converters
Voltage References

Data Converters and Voltage References

Introduction to Data Converters and Voltage References

Maxim is a full line supplier of A/D and D/A converters as well as precision voltage references. These include improved versions of industry standard "AD" and "ICL" series devices, as well as several new proprietary designs. As with all Maxim's products (except hybrids), the parts described in this catalog are available in the popular Surface Mount package, making Maxim the largest supplier of Analog Products in SMDs.

Maxim's goal is to develop products which continue to advance the state of the art in data converters and precision voltage references in applications such as analog signal processing, data acquisition, test systems, and communications. Some of the significant product advances introduced in this data book include:

- Complete 8 and 12 bit CMOS A/D converters that include voltage references and track/hold functions (MAX150, AD7572 and MAX162).
- 3¾ digit μP compatible Digital Multi-Meter circuits that offer superior performance and flexibility compared with previous integrating A/D converters (MAX133 and MAX134).
- Kelvin sensed precision +10V references. These references allow precise +10 Volts with excellent temperature coefficients as low as 1 ppm/°C to be obtained directly at the load (MAX670 and MAX671).

Other Data Books currently available from Maxim are listed below. Please contact Maxim or your local representative for a copy.

- Power Supply Circuits
- Analog Switches and Multiplexers
- Product Selector Guide and Price List

Maxim will continue to serve data acquisition designers with new products offering the highest standards of performance, quality and reliability. We appreciate the opportunity to serve you.

The Maxim Advantage™

The "Maxim Advantage" on second source products signifies an up graded quality level. At no additional cost Maxim offers a second source device that is subjected to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters, and device enhancements, when needed, that result in improved performance without changing the functionality.

These Maxim Advantages are listed on the "Maxim Advantage" page (usually the third page of the data sheet) and are highlighted (shaded) in the Electrical Characteristics table. For reference purposes, the original manufacturer's Electrical Characteristics are reproduced on the page facing the "Maxim Advantage" page.

In addition to these advantages, Maxim provides enhanced Product Conditioning and Qualification at no additional cost, as described in the "Package Unit Process Flow" section (Page A-1).

Data Sheet Identifiers

IDENTIFIER	PRODUCT STATUS	COMMENTS
None	Full Production	Data Sheet Finalized
Introductory	Initial Production	Data Sheet based on limited number of devices
Advance Information	Samples Only	Data Sheet based on design goals

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MAX161	CMOS 20μs 8 Bit 8 Channel Data Acquisition System
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MAX7129	4½ Digit Single-Chip A/D Converter with Multiplexed LCD Drivers
AD578	High Speed 3μs 12 Bit A/D Converter
AD7572	CMOS High Speed 5 & 12μs 12 Bit A/D Converter with Voltage Reference
AD7574	CMOS μP Compatible 8 Bit A/D Converter
AD7581	CMOS 8 Bit 8 Channel Data Acquisition System
AD7820	CMOS High Speed 8 Bit A/D Converter with Track/Hold
AD7824	CMOS High Speed 8 Bit A/D Converter with 4 Channel Multiplexer
AD7828	CMOS High Speed 8 Bit A/D Converter with 8 Channel Multiplexer
ADC0820	CMOS High Speed 8 Bit A/D Converter with Track/Hold
ICL7106	3½ Digit A/D Converter with Direct LCD Drivers
ICL7107	3½ Digit A/D Converter with Direct LCD Drivers
ICL7109	12 Bit A/D Converter with Three-State Binary Outputs
ICL7116	3½ Digit A/D Converter with LCD Display Hold
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ICL7126	Low Power, 3½ Digit A/D Converter with Direct LCD Drivers
ICL7129A	Low Noise, 4½ Digit Single-Chip A/D Converter with Multiplexed LCD Drivers
ICL7135	4½ Digit A/D Converter with Multiplexed BCD Outputs
ICL7136	Low Power, 3½ Digit A/D Converter with Direct LCD Drivers
ICL7137	Low Power, 3½ Digit A/D Converter with Direct LED Drivers

D/A Converters

MAX7624	CMOS 8 Bit Buffered Multiplying D/A Converter
AD565A	High Speed 12 Bit Monolithic D/A Converter with Voltage Reference
AD566A	High Speed 12 Bit Monolithic D/A Converter
AD7224	CMOS Double Buffered 8 Bit D/A Converter with Voltage Output Amplifier
AD7225	CMOS Quad 8 Bit D/A Converter with Voltage Output Amplifier
AD7226	CMOS Quad 8 Bit D/A Converter with Voltage Output Amplifier
AD7520	CMOS 10 Bit Multiplying D/A Converter
AD7521	CMOS 12 Bit Multiplying D/A Converter
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Maxim Complete Product Listing (continued)

(Contact Maxim Representatives or Distributors Listed in the Appendix for Full Product Information)

Voltage References

MAX670	+10V Precision Kelvin Sensed Reference, 3 ppm/°C
MAX671	+10V Precision Kelvin Sensed Reference, 1 ppm/°C
MAX672	+10V Precision Voltage Reference
MAX673	+5V, Precision Voltage Reference
AD580	Precision 2.5V Reference
AD581	Precision 10V Reference
AD584	Pin Programmable 10V, 7.5V, 5V, 2.5V Precision Voltage Reference
AD2700	+10 Volt Precision Reference, 3 ppm/°C
AD2701	-10 Volt Precision Reference, 3 ppm/°C
AD2710	+10 Volt Precision Reference, 1 ppm/°C
ICL8069	1.2V Voltage Reference
REF01	+10V Precision Voltage Reference
REF02	+5V Precision Voltage Reference

Operational Amplifiers and Buffers

MAX400	Ultra Low Offset Operational Amplifier
MAX420	±15V Chopper Stabilized Operational Amplifier
MAX421	±15V Chopper Stabilized Operational Amplifier
MAX422	Low Power, ±15V Chopper Stabilized Operational Amplifier
MAX423	Low Power, ±15V Chopper Stabilized Operational Amplifier
MAX430	±15V Chopper Stabilized Operational Amplifier
MAX432	Low Power ±15V Chopper Stabilized Operational Amplifier
MAX450	10MHz CMOS Video Amplifier
MAX451	Low Bias Current 10MHz Video Amplifier
MAX452	45MHz CMOS Video Amplifier
MAX453	2 Channel Mux'ed 40 MHz Video Amplifier
MAX454	4 Channel Mux'ed 40 MHz Video Amplifier
MAX455	8 Channel Mux'ed 40 MHz Video Amplifier
MAX460	High Accuracy Fast Buffer
AD3554	Wideband, Fast-Settling Operational Amplifier
BB3553	Very Fast Buffer Amplifier
BB3554	Wideband, Fast Settling Operational Amplifier
ICL7611	Low Power, Single Operational Amplifier
ICL7612	Low Power, Single Operational Amplifier
ICL7614	Low Power, Single Operational Amplifier
ICL7616	Low Power, Single Operational Amplifier
ICL7621	Low Power, Dual Operational Amplifier
ICL7622	Low Power, Dual Operational Amplifier
ICL7631	Low Power, Triple Operational Amplifier
ICL7632	Low Power, Triple Operational Amplifier
ICL7641	Low Power, Quad Operational Amplifier
ICL7642	Low Power, Quad Operational Amplifier
ICL7650	Chopper Stabilized Operational Amplifier
ICL7652	Chopper Stabilized Operational Amplifier
LH0033	Fast Buffer Amplifier
LH0063	Very Fast Buffer Amplifier
LH0101	Power Operational Amplifier
LT1001	Low Offset Operational Amplifier
OP07	Precision Operational Amplifier
PGA100	Programmable Gain Amplifier

Maxim Complete Product Listing (continued)

(Contact Maxim Representatives or Distributors Listed in the Appendix for Full Product Information)

Power Supply Circuits

MAX600	Low Cost AC-DC Regulator (110/220VAC to 5VDC — Full Wave)
MAX601	Low Cost AC-DC Regulator (110/220VAC to 5VDC — Half Wave)
MAX602	Low Cost AC-DC Regulator (8V RMS to 5VDC — Full Wave)
MAX610	AC-DC Regulator (110/220VAC to 5VDC — Full Wave)
MAX611	AC-DC Regulator (110/220VAC to 5VDC — Half Wave
MAX612	AC-DC Regulator (8V RMS to 5VDC — Full Wave)
MAX630/4193	CMOS Micropower Step-up Switching Regulator
MAX631	CMOS +5V Fixed/Adjustable Output Step-up Switching Regulator
MAX632	CMOS +12V Fixed/Adjustable Output Step-up Switching Regulator
MAX633	CMOS +15V Fixed/Adjustable Output Step-up Switching Regulator
MAX634/4391	CMOS Micropower Inverting Switching Regulator
MAX635	CMOS -5V Fixed/Adjustable Output Inverting Switching Regulator
MAX636	CMOS -12V Fixed/Adjustable Output Inverting Switching Regulator
MAX637	CMOS -15V Fixed/Adjustable Output Inverting Switching Regulator
MAX638	CMOS +5V Fixed/Ajustable Step-down Switching Regulator
MAX641	CMOS +5V Fixed/Adjustable 10 Watt Step-up Switching Regulator
MAX642	CMOS +12V Fixed/Adjustable 10 Watt Step-up Switching Regulator
MAX643	CMOS +15V Fixed/Adjustable 10 Watt Step-up Switching Regulator
MAX663	CMOS +5V/Adjustable Micropower Positive Voltage Regulator
MAX664	CMOS -5V/Adjustable Micropower Negative Voltage Regulator
MAX666	CMOS +5V/Adjustable Voltage Regulator with Low Battery Detect
MAX680	+5V to ±10V Voltage Converter
MAX690	Microprocessor Watchdog/Battery Switchover/Reset Generator
MAX691	Microprocessor Watchdog/Battery Switchover/Reset Generator
MAX692	Microprocessor Watchdog/Battery Switchover/Reset Generator
MAX693	Microprocessor Watchdog/Battery Switchover/Reset Generator
MAX8211	Programmable Voltage Detector
MAX8212	Programmable Voltage Detector
ICL7660	+5V to -5V Voltage Converter
ICL7663	Low Power, Programmable Positive Voltage Regulator
ICL7664	Low Power, Programmable Negative Voltage Regulator
ICL7665	Low Power Under/Over-voltage Detector

Display Drivers/Counters

ICM7211	4 Digit LCD Decoder/Driver
ICM7212	4 Digit LED Decoder/Driver
ICM7217	4 Digit LED Presettable Up/Down Counter
ICM7218	8 Digit Multiplexed LED Decoder/Driver
ICM7224	4½ Digit LCD High Speed Counter/Decoder/Driver
ICM7225	4½ Digit LED High Speed Counter/Decoder/Driver
ICM7231	8 Digit Triplexed LCD Decoder/Driver
ICM7232	10 Digit Triplexed LCD Decoder/Driver
ICM7233	4 Character Triplexed LCD Decoder/Driver
ICM7234	5 Character Triplexed LCD Decoder/Driver
MM74C945	4 Digit Up/Down Counter/Decoder/Driver
MM74C947	4 Digit Up/Down Counter/Decoder/Driver

Maxim Complete Product Listing (continued)

(Contact Maxim Representatives or Distributors Listed in the Appendix for Full Product Information)

Timers/Counters

ICM7240	Programmable RC Timer/Counter
ICM7242	Fixed RC Timer/Counter
ICM7250	Programmable RC Timer/Counter
ICM7260	Programmable RC Timer/Counter
ICM7555	Low Power, General Purpose Timer
ICM7556	Low Power, General Purpose Dual Timer

Interface

MAX230	+5V Powered, Five RS-232 Transmitters with Power Shutdown
MAX231	+5V and +12V Powered, Dual RS-232 Transmitters and Receivers
MAX232	+5V Powered, Dual RS-232 Transmitters and Receivers
MAX233	No External Component +5V Powered, Dual RS-232 Transmitters and Receivers
MAX234	+5V Powered, Quad RS-232 Transmitters
MAX235	No External Component +5V Powered, Five RS-232 Transmitters and Receivers with Power Shutdown and Receiver Three-State Enable
MAX236	+5V Powered, Four RS-232 Transmitters and Three RS-232 Receivers with Power Shutdown and Receiver Three-State Enable
MAX237	+5V Powered, Five RS-232 Transmitters and Three RS-232 Receivers
MAX238	+5V Powered, Quad RS-232 Transmitters and Receivers
MAX239	+5V and +12V Powered, Three RS-232 Transmitters and Five RS-232 Receivers with Three-State Receiver Enable
MAX240	+5V Powered, Five RS-232 Transmitters and Receivers with Power Shutdown and Receiver Three-State Enable in Plastic Flatpak
MAX241	+5V Powered, Four Transmitters, Five Receivers with Power Shutdown and Receiver Three-State Enable in 28 Pin Small Outline

Switched Capacitor Filters

MAX260	μP Programmable Universal Switch Capacitor Filter
MAX261	μP Programmable Universal Switch Capacitor Filter
MAX262	μP Programmable Universal Switch Capacitor Filter
MF10	Dual Second Order Universal Switch Capacitor Filter

Analog Multiplexers

MAX310	RF/Video 8 Channel Multiplexer/Demultiplexer
MAX311	RF/Video Differential 4 Channel Multiplexer/Demultiplexer
MAX312	RF/Video 8 Channel Latched Multiplexer/Demultiplexer
MAX313	RF/Video Differential 4 Channel Latched Multiplexer/Demultiplexer
MAX358	Fault Protected 8 Channel Multiplexer
MAX359	Fault Protected Differential 4 Channel Multiplexer
MAX368	Fault Protected 8 Channel Latched Multiplexer
MAX369	Fault Protected Differential 4 Channel Latched Multiplexer
DG506A	16 Channel CMOS Analog Multiplexer
DG507A	Differential 8 Channel CMOS Analog Multiplexer
DG508A	8 Channel CMOS Analog Multiplexer
DG509A	Differential 4 Channel CMOS Analog Multiplexer
HI-508A	Fault Protected 8 Channel Multiplexer
HI-509A	Fault Protected Differential 4 Channel Multiplexer
IH5108	See MAX358
IH5208	See MAX359
IH6108	See DG508A
IH6116	See DG506A
IH6208	See DG509A
IH6216	See DG507A

Maxim Complete Product Listing (continued)

(Contact Maxim Representatives or Distributors Listed in the Appendix for Full Product Information)

Analog Switches

MAX331	Quad SPST Normally Closed CMOS Analog Switch
MAX332	Quad SPST Normally Open CMOS Analog Switch
MAX333	Quad SPDT CMOS Analog Switch
MAX340	SPST High Voltage CMOS Analog Switch
MAX341	Dual SPST High Voltage CMOS Analog Switch
MAX342	SPDT High Voltage CMOS Analog Switch
MAX343	Dual SPDT High Voltage CMOS Analog Switch
MAX344	DPST High Voltage CMOS Analog Switch
MAX345	Dual DPST High Voltage CMOS Analog Switch
MAX348	Low Ron Dual SPST High Voltage CMOS Analog Switch
DG200	Dual SPDT CMOS Analog Switch
DG201A	Quad SPST Normally Closed CMOS Analog Switch
DG202	Quad SPST Normally Open CMOS Analog Switch
DG211	Quad SPST Normally Closed CMOS Analog Switch
DG212	Quad SPST Normally Open CMOS Analog Switch
DG300/A	TTL Compatible CMOS Analog Switch
DG301/A	TTL Compatible CMOS Analog Switch
DG302/A	TTL Compatible CMOS Analog Switch
DG303/A	TTL Compatbile CMOS Analog Switch
DG304/A	CMOS Analog Switch
DG305/A	CMOS Analog Switch
DG306/A	CMOS Analog Switch
DG307/A	CMOS Analog Switch
DG381/A	General Purpose CMOS Analog Switch
DG384/A	General Purpose CMOS Analog Switch
DG387/A	General Purpose CMOS Analog Switch
DG390/A	General Purpose CMOS Analog Switch
IH5040	SPST Normally Open CMOS Analog Switch
IH5041	Dual SPST Normally Open CMOS Analog Switch
IH5042	SPDT CMOS Analog Switch
IH5043	Dual SPDT CMOS Analog Switch
IH5044	DPST Normally Open CMOS Analog Switch
IH5045	Dual DPST Normally Open CMOS Analog Switch
IH5048	Low Charge Injection Dual SPST Normally Open Analog Switch
IH5049	Low Charge Injection Dual DPST Normally Open Analog Switch
IH5050	Low Charge Injection SPDT Analog Switch
IH5051	Low Charge Injection Dual SPDT Analog Switch
IH5140	Low Power Fast SPST Normally Open CMOS Analog Switch
IH5141	Low Power Fast Dual SPST Normally Open CMOS Analog Switch
IH5142	Low Power Fast SPDT CMOS Analog Switch
IH5143	Low Power Fast Dual SPDT CMOS Analog Switch
IH5144	Low Power Fast DPST Normally Open CMOS Analog Switch
IH5145	Low Power Fast Dual DPST Normally Open CMOS Analog Switch
IH5341	Dual SPST Normally Open RF/Video Switch
IH5352	Quad SPST Normally Open RF/Video Switch

A/D Converters

A/D Converter Selector

Part Number	Resolution	Output Type	Supply Voltage	Supply Current (Typ/Max mA)	Typical Applications and Comments	Page No.
MAX133	3¾ Digit ±4000 Counts	µP	9V	0.09/0.2	Digital Multimeters	1-1
MAX134	3¾ Digit ±4000 Counts	µP	+5V	0.09/0.2	Weigh Scales, Instruments	1-1
MAX136	3½ Digit ±2000 Counts	LCD	9V	0.06/0.15	Hold function, low power	1-19
ICL7106	3½ Digit ±2000 Counts	LCD Drive	9V	0.6/1.8	Digital Multimeters	1-99
ICL7107	3½ Digit ±2000 Counts	LED Drive	±5V	0.6/1.8	Digital Panel Meters	1-99
ICL7109	12 Bits + Sign ±4096 Counts	8/16 bit µP and UART	±5V	0.7/1.5	Data loggers, Process Control Up to 30 conversions/second	1-111
ICL7116	3½ Digit ±2000 Counts	LCD	9V	0.8/1.8	Same as ICL7106, but adds Hold function	1-129
ICL7117	3½ Digit ±2000 Counts	LED	±5V	0.8/1.8	Same as ICL7107, but adds Hold function	1-129
ICL7126	3½ Digit ±2000 Counts	LCD	9V	0.06/0.1	Use ICL7136 for new designs	1-133
MAX7129 ICL7129A	4½ Digit ±20,000 Counts	Triplexed LCD	9V	1.0/1.4	DPMs, Instruments Lowest Noise A/D — 3µV (7129A)	1-141
ICL7135	4½ Digit ±20,000 Counts	Multiplexed BCD	±5V	1.0/2.0	DMM, DPM, Data Loggers	1-153
ICL7136	3½ Digit ±2000 Counts	LCD	9V	0.06/0.1	Low Power version of ICL7106 Very Low Noise	1-165
ICL7137	3½ Digit ±2000 Counts	LED	±5V	0.06/0.2	Low Power when LED display turned off	1-173

A/D Converter Selector (continued)

Part Number	Resolution	Integral Linearity	Conversion Time	Supply Voltage	Input Range	Features	Page No.
MAX150	8 bits	½ LSB	1.34μs	+5V	+5V	Internal Reference	1-23
MAX154	8 bits/4 ch	½ LSB	2.0μs	+5V	+5V	Internal Reference	1-35
MAX158	8 bits/8 ch	½ LSB	2.0μs	+5V	+5V	Internal Reference	1-35
MAX160	8 bits	½ LSB	4μs	+5V	±15V	Fast AD7574	1-47
MAX161	8 bits/8 ch	½ LSB	20μs	+5V	±15V	Fast AD7581	1-59
MAX162	12 bits	½ LSB	3μs	+5/-12V	+5V	Internal Reference	1-67
MAX172	12 bits	½ LSB	10μs	+5V/-12V	+5V	Internal Reference	1-83
AD578	12 bits	½ LSB	3μ2	±15V	±10V	Onboard Reference	1-87
ADC0820	8 bits	½ LSB	1.4μs	+5V	+5V	Half-Flash	1-93
AD7572	12 bits	½ LSB	5.0μs	+5/-15V	+5V	Internal Reference	1-67
AD7574	8 bits	½ LSB	15μs	+5V	±15V	Analog $V_{IN} > V_{SUPP}$	1-47
AD7581	8 bits	½ LSB	66.6μs	+5V	±15V	8 byte RAM	1-59
AD7820	8 bits	½ LSB	1.34μs	+5V	+5V	Half-Flash	1-23
AD7824	8 bits/4 ch	½ LSB	2.0μs	+5V	+5V	4 Channels	1-35
AD7828	8 bits/4 ch	½ LSB	2.0μs	+5V	+5V	8 Channels	1-35

Analog/Digital Converter Terminology

Absolute Accuracy: The difference between the ideal expected ADC output code and the actual output for a specified input or range of inputs.

Analog-To-Digital Converter: Also ADC, A/D, and A-to-D. A device which translates an analog signal to a digital code.

Bipolar: Describes an ADC input range covering positive and negative input signals, +V to -V inputs.

Differential Inputs: Allow an ADC to measure the difference between two input signals. Improves noise rejection and simplifies connections to tranducers by reducing external circuitry.

Flash ADC: A type of ADC where a number of comparators simultaneously compare the analog input to a number of reference voltages. Decoding logic generates an output code based on the comparator decisions. The main advantage is very high conversion speed.

Full-Scale Error: Also Gain Error. The difference between the actual and ideal ADC output for a Full-Scale input. Expressed in % of FSR, or LSBs.

Integrating ADC: A type of ADC where the analog input is integrated over a specified time. A deintegration cycle then gates a digital counter so that its accumulated total is proportional to the input voltage. Advantages included high resolution, noise rejection and linearity.

Least Significant Bit (LSB): The ADC digital output bit that has the smallest weight. Also the analog input change that causes an output code change of 1. As an analog quantity, 1 LSB = FSR × 2^{-N}, where N is the number of ADC output bits.

Linearity: Also Nonlinearity and Integral Nonlinearity. See Relative Accuracy.

Most Significant Bit (MSB): The ADC digital output bit that has the largest weight.

No Missing Codes: Describes a property of an ADC whereby every possible output code can be obtained by "sweeping" through the analog input range. It is similar to Monotonicity in DACs.

R-2R Ladder: A resistor network used to generate binarily weighted currents or voltages in Successive Approximation Analog-to-Digital Converters.

Ratiometric Conversion: Where the unknown input signal is derived from a reference voltage that is also used as the reference for the ADC. Eliminates the need for a precision reference source since the transfer function is independent of the reference value. Commonly employed with strain gauges.

Relative Accuracy: (or End-Point Nonlinearity) The maximum deviation from a straight line which passes through the endpoints of the ADC transfer function (Zero and Full Scale). It is expressed in % or ppm of the Full Scale Range (FSR) or in LSBs.

Resolution: The number of counts that an ADC divides the input signal. Expressed in number of bits. An ADC with N-bit resolution divides its input range into 2^N steps.

Rollover Error: For an ADC with a Bipolar Input Range, the output difference for inputs of equal magnitude but opposite polarity. Specified in Counts or LSBs.

Sample-Hold: Also Track-and-Hold. A device which takes a "snap shot" of an analog signal so that it is held stationary for an A/D Conversion. Generally, Sample-Holds are only required for Successive Approximation ADCs which require that the input signal be ½ LSB stable during the conversion time.

Successive Approximation ADC: A type of ADC where the analog input is subject to a sequence of comparisons with binarily weighted references to determine output code. The input is first compared to a reference of ½ Full Scale. The MSB will be 1 if the input is greater, and 0 if it is less. This result determines if the input is then compared to ¼ FS or ¾ FS for the next bit. The tests continue until all bits are determined. Advantages are speed combined with high resolution.

Temperature Coefficient: The variation of a parameter (such as Zero Error, Full Scale Gain, or Linearity) with ambient temperature. Specified in %/°C or ppm/°C.

Total Unadjusted Error: Includes Full Scale, Relative Accuracy, and Zero Code Error specifications. The Maximum output deviation from the ideal expected values. Specified in LSBs or % of FSR at a fixed reference voltage, usually +10V.

Unipolar: Describes an ADC input range covering one polarity of signal, either 0 to +V or 0 to -V input.

Zero Error: Also Offset Error. The ADC output code for an input of 0V.

MAXIM

3¾ Digit DMM Circuit

General Description

The MAX133 and MAX134 are integrating A/D converters for 3¾ digit multimeters and data acquisition systems such as data loggers and weigh scales. The A/D's internal resolution is ±40,000 counts. An extra digit is supplied as a guard digit to allow autozero or tare of a 4000 count displayed reading to 1/10 of a displayed count. The conversion time is 50ms.

The MAX133 and MAX134 differ only in their microprocessor interface. The MAX133 has a 4 bit multiplexed address/data bus while the MAX134 has 3 separate address lines and a 4 bit bidirectional data bus. Both devices can be used with 4, 8, and 16 bit microprocessors.

When controlled by a microprocessor, the MAX133 and MAX134 can perform auto-ranging measurements from ±400.0mV to ±4000V full scale. External attenuator resistors are required, but range switching is performed by the A/D.

The power supply is typically a 9V battery or ±5V. Operating current is typically 100μA while standby current in only 25μA.

Applications

Digital Panel Meters
Weigh Scales
Data Loggers
Data Acquisition Systems

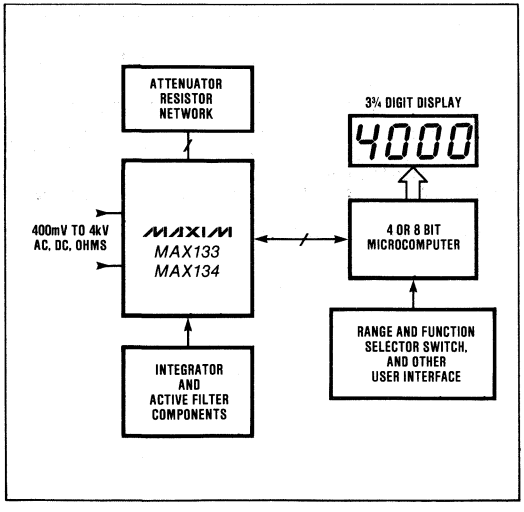
Features

- **40,000 Count Resolution**
- **0.025% Accuracy**
- **20 Conversions per Second**
- **Microprocessor Interface**
- **100μA Operating Supply Current**
- **Low External Component Count**
- **5μV Resolution**
- **Demonstration Kit Available MAX134/DEMO**

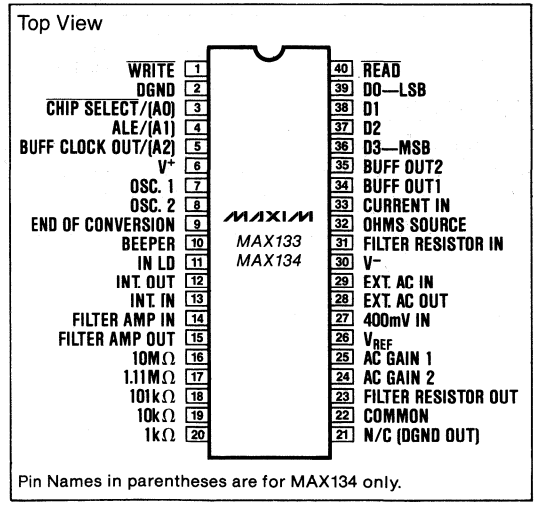
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX133CPL	0° C to +70° C	40 Lead Plastic DIP
MAX133CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX133C/D	0° C to +70° C	Dice
MAX133EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX133EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier
MAX134CPL	0° C to +70° C	40 Lead Plastic DIP
MAX134CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX134C/D	0° C to +70° C	Dice
MAX134EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX134EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier

Typical Operating Circuit



Pin Configuration



Pin Names in parentheses are for MAX134 only.

3¾ Digit DMM Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V^+ to V^- ..... +15V
- V^+ to DGND ..... +6V
- V^- to DGND ..... -9V

Analog Input Voltage (any input) (Note 1) ..... V^+ to V^-

Reference Input Voltage ..... V^+ to V^-
Digital Inputs ..... (DGND - 0.3V) to (V^+ + 0.3V)
Power Dissipation 800mW
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

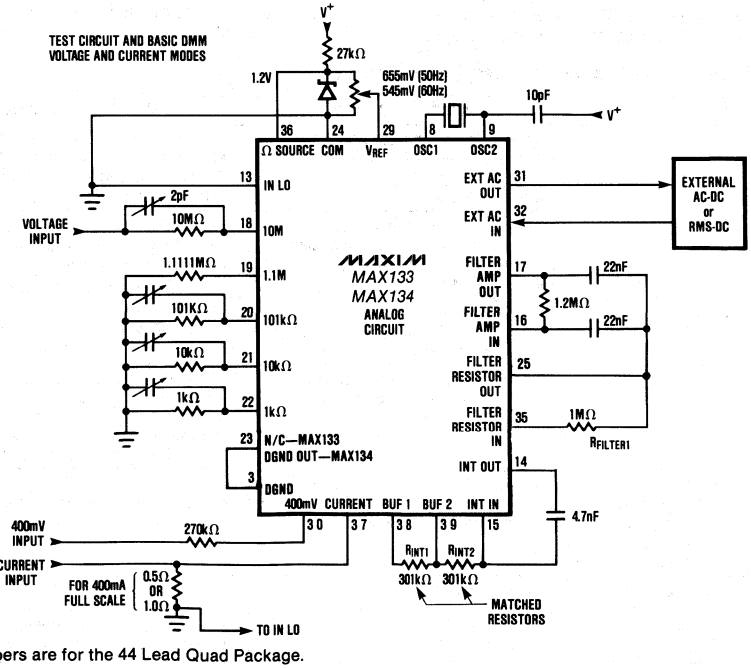
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Zero Input Reading	Read Zero Mode, DC Volts Zero Input Offset Reading will be corrected Digitally in the µP			±5000	Count
Δ Zero Input Reading	Difference between 1000VDC Scale, V_{IN} = 0 and 3VDC and Scale, V_{IN} = 0 (Note 3)	-2		+2	Count
$I_{10m\Omega}$	Leakage Current into 10MΩ Pin			20	pA
Rollover Error	$\|V_{IN}+\| = \|V_{IN}-\|$ = 3V	-10		+10	Count
Integral Linearity	Best Fit Line 300mVDC Scale Not production tested	-10		+10	Count
Differential Nonlinearity	Deviation from ideal Count size Not production tested		0.1	5	Count
Recovery Time	Number of Conversions to settle to within 2 Counts of final reading on 3 VDC Scale after a attempting to measure a 2.95V Input on the 300mV Scale. Unfiltered DC Mode		1		Conv.
	Settle to 1 Count		2		
CMRR	V_{CM} = ±500mV V_{CM} is (IN LO - Common)		86		dB
Noise	300mVDC Scale Zero Reading Mode Pk-Pk Value exceeded less than 5% of readings		2 2		Count
Zero Reading Drift			0.1		Count/C
Scale Factor Tempco	300 mVDC scale 0ppm ext Reference			5	ppm/°C

Note 1: Input Voltage may exceed supply voltages, provided the Input Current is limited to ±1mA.
Note 2: Analog performance is specified in counts relative to a 40,000 count full scale; i.e. a spec of 5 counts would correspond to 1/2 of one count on a 3¾ digit meter.
Note 3: This parameter is guaranteed by testing the input bias currents of the input pins 10MΩ and 1.11MΩ.

ELECTRICAL CHARACTERISTICS (continued)

(V^+ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY AND DIGITAL SECTION						
Digital Ground Voltage	DGND	Referenced to V^+ $5\mu A < I_{SINK} < 500\mu A$	-4.5	-5	-5.5	V
Analog COMMON Voltage		(V^+ - Common) 250kΩ between V^+ and COMMON	2.8	3.0	3.3	V
Analog COMMON Sink Impedance		ΔV, I_{COMMON} = 10μA to I_{COMMON} = 2mA		4	20	Ω
Analog Common Source Capability		For $\Delta V_{COMMON} < 0.5V$		1		μA
Tempco of Common				80		ppm/°C
Output High	V_{OH}	D_{0-3}, Data Ready I_{OUT} = -100μA	V^+ - 0.5			V
Output Low	V_{OL}	D_{0-3}, Data Ready I_{OUT} = 400μA			0.4	V
Input High	V_{IH}	D_{0-3}, A_{0-3}, Data Ready, RD, WR	60	45		% (V^+ - DGND)
Input Low	V_{IL}	D_{0-3}, A_{0-3}, Data Ready, RD, WR		40	20	% (V^+ - DGND)
Supply Current	I_{SUPP}			100	250	μA
Sleep Current	I_{SLEEP}			25		μA
Low Battery	V_{LBAT}	Low Battery Flag On	6.3	6.8	7.5	V



NOTE: Pin Numbers are for the 44 Lead Quad Package.

3¾ Digit DMM Circuit

System Considerations

The MAX133/134 is intended for use with a microprocessor. The MAX133/134 contains an A/D and auxilliary circuitry such as attenuator range switches, a piezoelectric beeper driver, an active filter, a low battery detector, and both analog and digital power supplies; but it does not include any display drive capability. The MAX133/134 reduces the component count and system cost by minimizing the external components required for the analog portion of the system, but does not restrict final product features by including autoranging or other digital control functions. The MAX133/134 is intended to work as the analog front end of a microprocessor, with the features of the end product being determined by the microprocessor software. Table 1 shows how the execution of several typical functions is partitioned between the MAX133/134 and the microprocessor.

The MAX133/134 provides all of the logic and counters for control of the conversion sequence, and the external microprocessor does not have to perform any critical timing or complex control of the MAX133/134. The MAX133/134 has range switches for a 5 decade attenuator which uses external resistors, and has additional mode-selection circuitry for performing voltage, current, AC or DC, ohms, and continuity measurements. The 5 decade attenuator and mode-selection circuitry is controlled by an external microprocessor via control bits written into the MAX133/134.

The MAX133/134 has normal mode rejection of line frequency of at least 80dB on the voltage ranges; the microprocessor selects rejection of either 50Hz or 60Hz by setting a MAX133/134 control bit. A two pole active filter can also be turned on by the microprocessor, adding about 40 dB normal mode rejection above 50Hz. See the "Digital Interface" section for details on which functions can be controlled by the external microprocessor.

The basic blocks of the MAX133/134 are

- A/D section
- Input Range Switching
- Ohms Circuitry
- Active Filter
- Power Supply, Common, Low Battery Detector
- Oscillator and Beeper Driver
- Digital Interface

A/D Section

The A/D uses a "residue multiplication" conversion scheme to provide a full ±40,000 count resolution reading every 50 milliseconds, while still providing the excellent noise performance and power line normal mode rejection associated with integrating A/Ds. See "Conversion Method and Timing" below for details of the conversion method. All timing and A/D conversion phase control is performed by the MAX133/134 without microprocessor intervention. The A/D section will perform a non-zero-corrected conversion every 50 milliseconds (20 conversions per second).

The microprocessor must periodically direct the MAX133/134 to perform a read zero conversion, which also takes 50 milliseconds. This read zero conversion is a conversion performed with IN LO internally

Table 1. Coordination of the MAX133/134 and the Microprocessor

FUNCTION	MAX133/134 ACTION	MICROPROCESSOR ACTION
Autoranging	Contains the attenuator control switches. Selects 400mV to 4000V ranges as directed by the microprocessor.	Detects overload and commands the MAX133/134 to select the next higher range. Range switching hysteresis and manual range selection is controlled by the microprocessor.
Zero Reading (system offset correction)	Internally shorts the A/D inputs and performs a measurement of system offset when directed by the microprocessor.	Periodically commands the MAX133/134 to perform a zero reading. Subtracts this zero reading from normal readings to correct for the internal offset of the MAX133/134.
Range/Function Selection	Selects Ohms/Current/ AC-DC/Voltage/Continuity as directed by the microprocessor.	Maintains the user interface, and directs the MAX133/134 to select the desired range.
Display of Readings	Max 133/134 provides raw, non-zero-corrected data to microprocessor.	The microprocessor performs zero correction and any gain correction or scaling that is desired. The microprocessor then displays the information, using either its own display driver capability or an external display driver.
Value added DMM features such as display hold, peak hold, either manual range selection or autoranging, peak reading hold, min/max display, thermocouple linearization, etc.	Performs conversions as directed by the microprocessor, returning the A/D results to the microprocessor.	Uses the MAX133/134 conversion results and software routines to provide a multitude of product features.
Digital panel meter features such as zero and span adjustment, high/low limit alarms, display in engineering units, etc.	Performs conversions and range selection as directed by the microprocessor.	Takes the MAX133/134 readings, performs zero offset and scale corrections, then displays the results. The microprocessor also performs such functions as high/low limit alarms.

shorted to IN HI, and the result of this zero conversion must be subtracted (by the microprocessor) from normal measurements to obtain a zero-corrected reading. The zero correction that must be subtracted is determined by the MAX133/134's internal offsets. Since these offsets are relatively slow changing, zero conversion readings need only be taken often enough to track long term drifts and temperature changes. The zero conversion reading will change slightly with a change in common mode input voltage or reference voltage, and a new zero conversion reading should be taken if either of these change.

In ratiometric ohms measurement the reference voltage will change significantly as the value of the unknown resistor varies. To reduce the errors caused by the system offset the MAX133/134 "chops" the input buffer and integrator. The "chop" consists of a reversal of the input transistors during the conversion cycle. The timing of this chop is such that in the R/2 or ohms measurement mode, the system offset is almost completely nulled out if the X2 mode is not selected. Even if the X2 mode is selected, the system offset does not exceed 5000 counts on any range. Since the internal full scale range of the MAX133/134 is greater than ±49,000 counts, at least ±40,000 counts of resolution are available after zero offset correction.

Each conversion result is latched into a Conversion Register which can be read by the microprocessor. The data format is nines complement BCD (a zero reading is 00000, a -1 reading is 99999, a -25000 reading is 75000). The nines complement form is the most convenient BCD format since the addition of the nines complement of a number is equivalent to subtracting that number. See "Software Notes" for simple BCD to binary conversion algorithms.

The last digit of conversion is used for digital autozero and is usually not displayed. Note that each count of the least significant digit of the MAX133/134 output corresponds to 1/10 of a count if a 4000 count full scale display is used. For current ranges with a voltage drop of only 200mV, the measured reading can be multiplied by two by using the X2 ("times 2") function of the MAX133/134. The X2 function reduces the R_{INT} resistor value by a factor of two during the Integrate phase. With the X2 range, a 200mV input voltage will result in a full scale, 4000.0 measured reading. Alternatively, the normal 400mV range can be used, with the multiplication by two being done by the microprocessor digitally. In this case, each count of the least significant digit is 1/5 of a displayed count. A 100mV full scale voltage drop can be achieved by using both the MAX133/134 X2 range and a digital times 2 multiplication in the microprocessor.

Each of the 20 conversions per second has a Zero Integrator phase to ensure rapid recovery from overload, and the MAX133/134 will recover to within 2 counts one conversion after an overload of 10 times full scale when the onboard active filter is not used.

Input Range Switching

In voltage measurement ranges other than 400mV, voltages are applied to the pin labeled 10MΩ through a 10MΩ resistor. By selecting the proper shunt resistors (1.1MΩ through 1KΩ) the input voltage will be attenuated to a 400mV range. The input attenuator switch section includes analog switches to switch both the input current and to sense the voltage on the shunt resistor. Other input switching functions select between the output of the input attenuator and the voltage developed across the current sensing resistors during current measurement. See Figure 1.

The 5pA input bias current of the MAX133/134 might result in unacceptable errors with a 10MΩ input resistor on the 400mV scale, so a separate pin with a 100kΩ to 1MΩ input resistor is used for the 400mV scale. The 10MΩ resistor used on the higher voltage ranges does not cause appreciable error since the input leakage current is shunted to ground through the 1.11MΩ to 1kΩ attenuator shunt resistors.

To avoid errors that might occur through coupling of high frequency, high voltage signals from the input of the attenuator to the low level 400mV and Current inputs, these two inputs have 10kΩ switches which connect them to Common whenever they are not selected.

The input section also includes switches to allow an external AC-DC converter to be inserted into the signal path. Figure 10 shows a typical average-sensing RMS-calibrated AC-DC converter.

Ohms and Diode Measurement

The input attenuator resistors are also used as reference resistors in the ohms mode. Note that the 10MΩ resistor must be externally paralleled with the other resistors to get exactly 1MΩ, 100kΩ, etc. The ohms source buffer input is usually connected directly to the external bandgap reference or to another 1.25V source. In the 4kΩ through 40MΩ ranges there will be a total of 1.25V across the series combination of reference resistor, unknown resistor, and the input protection network; and the maximum voltage across the unknown resistor at full scale will be less than 400mV. On the 400Ω range, the ohms voltage source is a diode connected to V^+ through a 2kΩ p-channel switch. With a 3V Common voltage, this supplies approximately 2.2V across the series combination of reference resistor, unknown resistor, and input protection network. This higher voltage is used on the 400Ω range to compensate for the decrease in reference voltage caused by the input protection network. The MAX133/134 are designed to operate with PTC protection resistors of 2kΩ or less.

The voltage across the reference resistor is used as the reference voltage for the A/D when in the ohms mode, and the differential voltage between IN LO and IN HI is the input signal. The integration period is 500 counts, independent of the 50/60Hz control bit setting.

3¾ Digit DMM Circuit

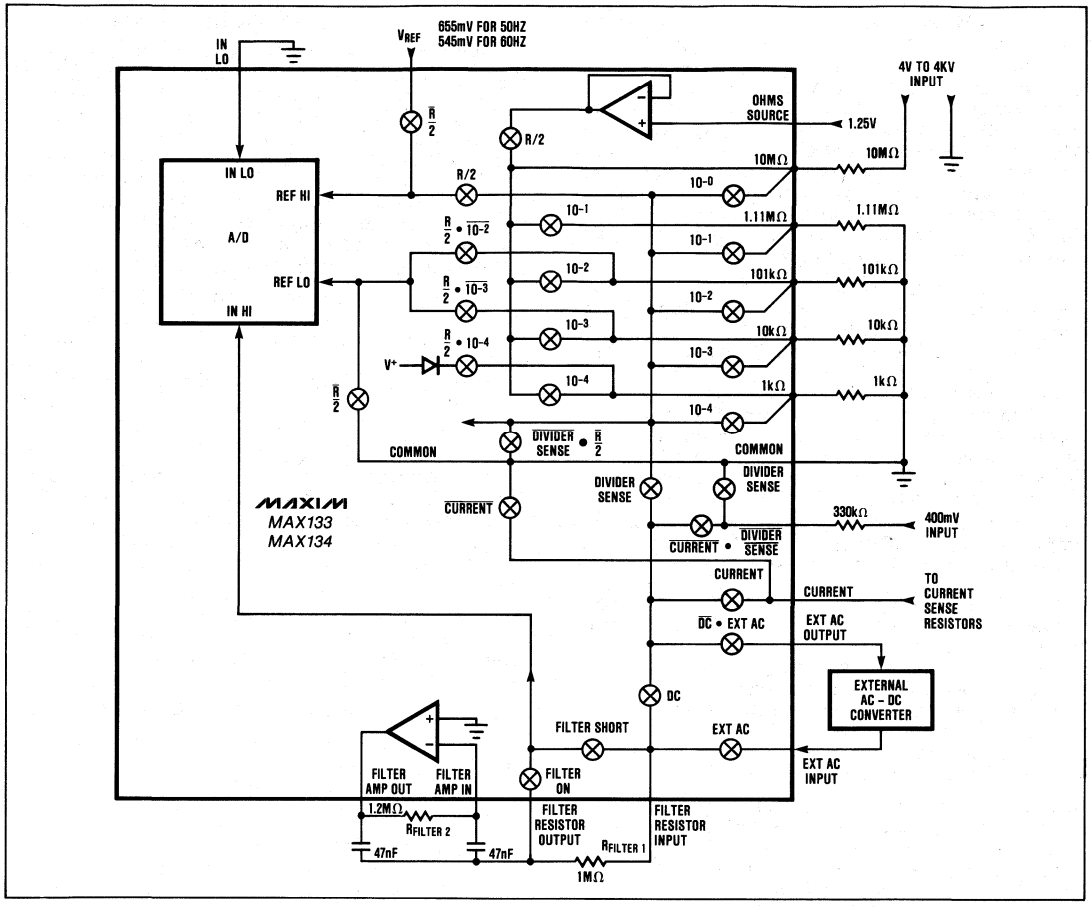


Figure 1. MAX133/134 Input Section

The digital output code is

$$50000 \times \frac{R_{UNKNOWN}}{R_{REF}}$$

with a maximum non-zero-corrected output code of ±49,520 and a maximum zero reading of 5000.

A 1kΩ reference resistor is used for the 400Ω full scale, a 10kΩ reference for a 4kΩ full scale, etc. A 10MΩ reference resistor is used for both the 4MΩ full scale and the 40MΩ full scale. To get the correct results in the ohms measurement or R/2 mode, the conversion result must be multiplied by two either digitally by the microprocessor or by using the X2 range, except on the 40MΩ scale. The 40MΩ range has the same reference resistor as the 4MΩ range but a times 10 scale factor is obtained by not multiplying by 2, and by activating the ÷5 function. If the times 2 multiplication is performed by the microprocessor, the Read Zero offset of the MAX133/134 in the ohms mode will be just a few counts, and will be nearly independent of the value of the unknown resistor being measured. If the MAX133/134 X2 mode is used to multiply by 2, then frequent Read Zero readings should be taken, since the read zero offset is inversely proportional to the reference voltage, and the reference voltage varies as the resistance of the unknown resistor varies.

Since the input protection PTC resistor shown in Figure 2 reduces the reference and input voltage, particularly on the 400Ω scale, the PTC resistance should be as low as is possible while maintaining the desired level of protection. Greater than 2kΩ PTC resistance will increase the noise level of measurements on the 400Ω range.

Since the MAX133/134 does not use a reference capacitor, the only limit on the response time in the ohms mode is the active filter. Even when the active filter is turned off, $R_{FILTER1}$ is still connected, and the input voltage must charge the filter capacitors. This will generally be noticed only on the 4MΩ and 40MΩ ranges.

A diode test range can be implemented by simply connecting to V^+ the PTC used for input protection in the ohms ranges. The PTC then delivers approximately 1mA of current to the diode. The diode voltage can be measured either on the standard 4V scale, or on the 400mV scale with the ÷5 function activated to result in a 2V full scale. As always, the latched continuity circuit is active, and it will latch whenever the input voltage goes below approximately 100mV. The microprocessor can also test the measured voltage at the end of each conversion if a more precise detection of continuity threshold is desired.

Active Filter

The 2 pole active filter circuit is shown in Figure 3. The op amp's offset has no effect on the DC accuracy since the op amp is only AC coupled and the DC signal path is only through the passive 1MΩ resistor. Note that the active filter will limit the speed of response of the MAX133/134 to input voltage changes, and for that reason it may be desirable to disconnect the input filter during autoranging. Since the source impedance at the filter input varies with the input attenuator selected, the response time will be slower on the 4V range.

Oscillator and Beeper Driver

The MAX133/134 is designed to operate with a 32768Hz tuning fork crystal similar to the Statek CX-1V, using only one external capacitor and no external resistors. If desired, the MAX133/134's OSC1 pin can be driven externally.

The 32kHz clock is used internally as the clock for the sequence and measurement counters. The 32kHz clock is also divided down to 2048Hz and 4096Hz for driving a beeper. The beeper output swings from V^+ to V^- and can directly drive piezoelectric beepers. Two control bits set by the microprocessor select the frequency (2048 or 4096 Hz) of the beeper and turn it on or off. Since the beeper is controlled by the microprocessor, it can be used for both continuity indication and for an audible operator feedback signal for peak hold or range changes.

Power Supply: Common, Digital Ground, Low Battery Detector

Both the MAX133 and MAX134 can operate from either a nominal 9V battery or a ±5V supply. The maximum power supply current in DC voltage and DC current modes is 250μA, with a typical operating current of 100μA.

Analog Common is derived from a zener and is nominally 3.0V below V^+. For lowest cost applications the Common voltage, with a tempco of 80ppm/°C, may be usable as a reference. In most applications, a bandgap reference will be connected to Common, with a pullup resistor to V^+, and a voltage divider connected across the bandgap reference to generate the 545mV (60Hz operation) or 655 (50 Hz operation) reference voltage. In a battery powered meter, the Analog Common pin is used as the system ground reference point.

The MAX133 and MAX134 also generate a Digital Ground voltage, which is nominally 5V below V^+,

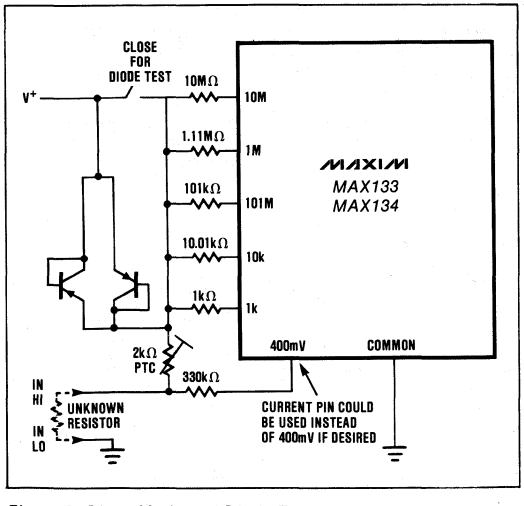


Figure 2. Ohms Mode and Diode Test

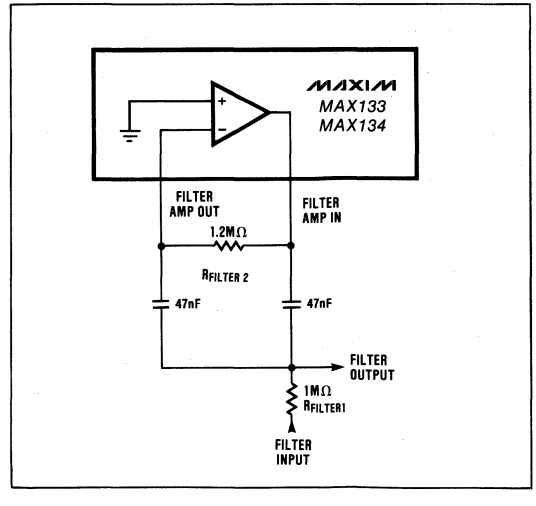


Figure 3. Active Filter

3¾ Digit DMM Circuit

and which will remain in the range of 5V ±10% while sinking 5μA to 500μA. The DGND generator has substantial current sinking capability, but can easily be pulled to a more negative voltage since the current sourcing capability is only 1 μA typical. The MAX133 internally connects the Digital Ground generator to the DGND pin. Normally the MAX133 is powered by a 9V battery and the Ground, V^-, or V_{SS} pin of the microprocessor is connected to the MAX133 DGND pin.

The MAX134 connects the DGND voltage generator to the pin, DGND Out, and the MAX134 DGND pin is an input only. For use with 9V batteries, externally connect the MAX134 DGND Out pin to the MAX134 DGND pin. For use with external ±5V power supplies, connect the DGND pin to ground, V^+ to +5V and V^- to -5V.

The MAX133/134 has an onboard low battery detect circuit that will indicate when the battery voltage is approaching the minimum operating voltage of the MAX133/134, which is approximately 6.8V.

Digital Interface

The MAX133 and MAX134 differ only in their digital interface. The MAX133 has a multiplexed address and bidirectional data bus, while the MAX134 has 3 separate address lines in addition to a bidirectional data bus. In both products, the data bus has 4 bits, allowing the use of the MAX133/134 with both 4 bit and 8 bit microprocessors.

MAX134 Digital Interface

The digital interface between the MAX134 and the controlling microporcessor is via a 4 bit bidirectional bus, D0-D3. In addition to the 4 data bus lines, there are 3 address lines and 2 control signals: A0-A2, $\overline{WR}$, and $\overline{RD}$.

The three address lines, A0-A2 select one of 5 control registers. When $\overline{WR}$ goes low, data will be written from the bus into the MAX134 control register addressed by A0-A2. When $\overline{RD}$ is low, the MAX134 will drive the bidirectional bus, placing on it the data contained in the results or status register addressed by the address inputs A0-A2. Figure 4 shows typical read and write sequences.

Digital Interface, MAX133

The MAX133 uses only 7 lines to interface with the microprocessor. The microprocessor first selects the register to be read or written to by placing the address of the register onto the 4 bit multiplexed address/data bus. The microprocessor then pulses the Address Latch Enable (ALE) line high to latch the register address into the MAX133. To read the selected register, the microprocessor then drives the $\overline{Read}$ line low, and the MAX133 places the register data onto the data bus. To write to the selected register the address is latched as described above, then the microprocessor places the data onto the bus and then pulses the $\overline{Write}$ line low. The MAX133 latches the data into the data into the selected register on the rising edge of $\overline{Write}$. See Figure 5. The Chip Select ($\overline{CS}$) line must be low to enable either the $\overline{RD}$ or $\overline{WR}$ lines, but ALE is not gated by $\overline{CS}$.

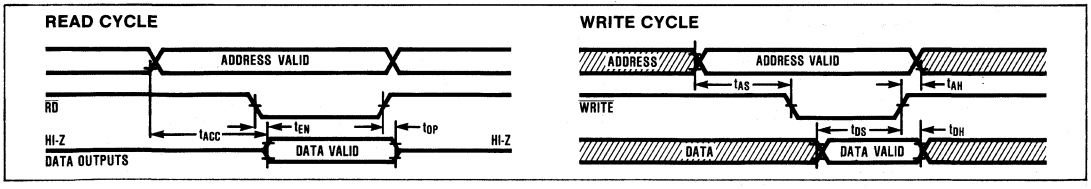


Figure 4. MAX134 Read and Write Sequence

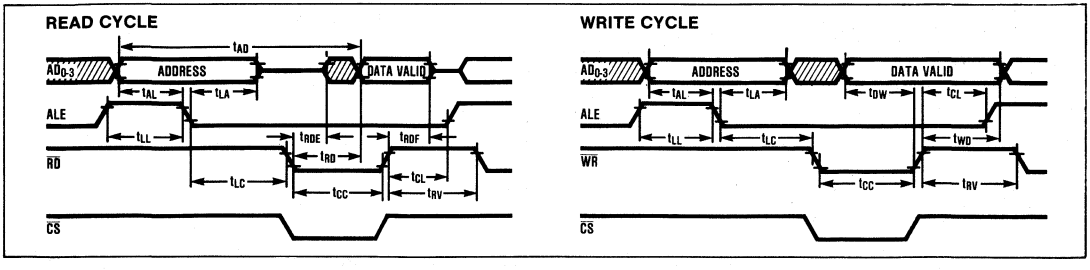


Figure 5. MAX133 Read and Write Sequence

Digital Interface, MAX133 and MAX134

In most cases, the EOC signal will be either monitored by an I/O pin, or it will drive an Interrupt pin on the microprocessor. In battery powered systems, it may be desirable to put the microprocessor into a sleep or standby mode until EOC goes high. The microprocessor then performs any required data processing and display updates, then reenters the sleep mode. This conserves battery power since the microprocessor power consumption is minimized.

The data that has been latched in the MAX133/134 control registers does not immediately affect operation. The input registers are double buffered, and the control bits take effect at the end of the current conversion. In the hold mode, the double buffered registers are transparent, and any updates to the registers take effect immediately, as do any changes made during the one clock cycle period at the end of each conversion during which the second rank of buffers are being updated.

Description of Output Bits

The data format is nines complement BCD. For example:

MEASUREMENT RESULT	BCD DATA
+40000	40000
—	—
+00100	00100
—	—
+00001	00001
+00000	00000
(there is NO -00000)	
-00001	99999
—	—
-00100	99900
—	—
-40000	60000

The Latched Continuity bit will be high if the input voltage has gone below the continuity threshold of approximately 100mV since the last time the register was read. Each time this register (Register 5) is read, the continuity latch is reset.

The Low Battery bit is high whenever the battery voltage is below the low battery detect voltage.

The $\overline{\text{Holding}}$ bit is low whenever the MAX133/134 is in the hold state.

Description of Control Bits

Hold. A 1 in Hold will stop conversions at the end of the next conversion. If the MAX133/134 is in the Hold mode, a conversion will start on the next clock cycle after Hold is set to 0. The oscillator continues to run and all circuitry is active during the Hold mode.

High Frequency. A 1 in the High Frequency bit will select 4096Hz as the beeper frequency. A 0 will select 2048Hz.

Beeper On. A 1 turns on the beeper driver.

Sleep. A 1 in Sleep puts the MAX133/134 into the standby or sleep mode. The Common voltage buffer is turned off and the internal analog circuits are turned off, but the DGND circuitry is still active. The oscillator continues to run. Current consumption is reduced to 25μA. Several conversions must be performed after exiting the Sleep mode before full conversion accuracy is obtained.

10-0 through 10-4. These bits control the attenuator network switches. The 10-0 bit selects the 10MΩ input without activating any shunt resistors. This is an alternate 400mV input. The 10-1 bit activates the 10:1 attenuation by selecting the 10MΩ input and connecting the 1.111MΩ shunt. Similarly, 10-2, 10-3, and 10-4 bits selects input attenuation factors of 100, 1000, and 10,000 respectively. In the ohms mode these bits set the resistance range.

Table 2: Register Map of Output Data From the MAX133/134 to the Microprocessor

ADDRESS OR REGISTER NUMBER	REGISTER NAME	REGISTER CONTENTS			
0	Ones	Conversion Result BCD data for least significant digit (The undisplayed digit used for digital autozero)			
1	Tens	BCD data of Conversion Result (Least significant displayed digit)			
2	Hundreds	BCD Data of Conversion Result			
3	Thousands	BCD Data of Conversion Result			
4	10 Thousands	BCD Data of Conversion Result			
5	Status	D3 Always 1	D2 Latched Continuity	D1 $\overline{\text{Holding}}$	D0 Low Battery

3¾ Digit DMM Circuit

Table 3. Register Map of Input Data From the Microprocessor to the MAX133/134

ADDRESS OR REGISTER NUMBER	D3	D2	D1	D0
0	Hold	High Frequency	Beeper ON	Sleep
1	10-0	Filter Short	÷5	50Hz
2	10-4	10-3	10-2	10-1
3	DC	Ext AC	Divider Sense	Ohms R/2
4	Current	X2	Read Zero	Filter On

BIT SET	VOLTAGE RANGE	OHMS RANGE
10-0	400mV	4MΩ and 40MΩ
10-1	4V	400kΩ
10-2	40V	40kΩ
10-3	400V	4kΩ
10-4	4000V	400Ω

NOTE: The divider sense bit must also be set to enable the 10-0 through 10-4 bits.

50Hz. When set to 1 the integration period for voltage measurement is one cycle of the 50Hz power mains (655 clock cycles). When 0, the integration period is one 60Hz power line cycle (545 clock cycles).

X2. Setting the bit to 1 activates the MAX133/134 "times 2" function. When X2 is active, R_{INT2} only is used as the integrator resistor during the integration phase. R_{INT1} and R_{INT2} in series are used as the integration resistor for all deintegration phases and for the integration phase when X2 is 0. If $R_{INT1} = R_{INT2}$ then setting the X2 bit doubles the digital output for a given input voltage.

÷5. When this bit is set to a 1 the integration period is reduced by a factor of 5. This reduces the digital output code by a factor of 5, and allows a higher input voltage to be used. The full scale input voltage is multiplied by 5 when this bit is set, but caution should be used to make sure that the 2μA maximum recommended integrator output current is not exceeded, or the MAX133/134 linearity will be degraded.

Ohms or R/2. Setting this bit to a 1 selects the ohms measurement mode. See "Ohms and Diode Measurement" section above. Set the Divider Sense to 0 for ohms measurements.

Read Zero. Setting this bit to a 1 causes the next conversion to be a Read Zero conversion. A read zero conversion is performed with In Hi and In Lo internally shorted, and the reference selected by the other control bits is used. The read zero conversion result is proportional to the internal offsets of the MAX133/134, and this result should be subtracted from other measurements to get zero-corrected readings.

Filter On and Filter Short. These bits control the active filter. See Figures 1 and 3.

FILTER ON	FILTER SHORT	FUNCTION
1	0	Normal filter on condition
1	1	Filter on, $R_{FILTER1}$ is bypassed. Use this bit combination to compensate for the higher source impedance of the 4V range.
0	1	Bypasses the Filter.
0	0	Invalid combination, do not use.

DC. This bit selects the DC mode when set to 1 and selects the AC mode when it is 0. This bit should also be set for ohms measurement.

External AC. This bit should be set to 1 whenever the AC mode is selected (DC=0).

Divider Sense. This bit, the 10-0 through 10-4, and the Current bits select the input signal source. Divider sense should be 1 whenever the input attenuator is selected. Set Divider Sense to 0 to select the 400mV input.

Current. Set divider sense to 0 and the Current bit to 1 to select the Current input. Note that while this bit and the associated pin are named "Current", the actual input is the voltage drop across an external current sensing resistor.

Component Selection

Integration Resistors

For an accurate times 2 multiplication in the X2 mode, the two R_{INT} resistors must be exactly equal. If the X2 mode is not needed, then connect a 604kΩ R_{INT1} between Buffer Out1 and the integration capacitor C_{INT}, and leave Buffer Out2 open. The value of both R_{INT1} and R_{INT2} is normally 301kΩ for a 545mV or 655mV reference. This sets the integrator output current to 2μA during the Deintegrate phase. If the reference voltage is different, scale the R_{INT} resistors proportionately.

Integration Capacitor

The normal value for the integration capacitor is 4.7nF. This value, in combination with the integrator output current and the clock frequency sets the integrator swing to about 3V for the voltage ranges when R_{INT1} = R_{INT2} = 301kΩ and the clock frequency is 32,768Hz. While the same integrator swing can be achieved with other values of capacitors by changing the value of R_{INT}, lower values of C_{INT} may introduce more noise through increased pickup of noise and 50/60Hz signals. Excessively high values of C_{INT} will also cause noise problems by reducing the integrator swing to unacceptably low values, causing the comparator noise to dominate the conversion errors. Large values of C_{INT} will also cause linearity errors since the settling time of the internal times 10 circuitry is affected by the value of C_{INT}.

The dielectric absorption of the integration capacitor directly affects the integral linearity, and high quality polypropylene capacitors are recommended. Polycarbonate and polystyrene capacitors may give satisfactory performance in less demanding applications, while the fourth choice, polyester (Mylar), will cause about 0.1% integral non-linearity.

Active Filter Components

The RC time constant of the active filter components sets the rolloff frequency of the filter. The effective value of the $R_{FILTER1}$ (Figure 3) is the sum of its value plus the source impedance driving the filter. In the 30V range for example, the effective source impedance is the 101kΩ resistor in the attenuator. In the 3V range, the effective source impedance is 1MΩ. This variable source impedance will alter the filter characterlstics somewhat as the different voltage ranges are selected. The effect of the different source impedances can be minimized by increasing the value of the filter resistors while decreasing the value of the filter capacitors proportionately. This, however, will increase the offset error caused by the A/D input leakage current flowing through the filter resistors. For most applications, filter resistor values between 1MΩ and 3MΩ are optimal.

The RC time constant sets the filter rolloff frequency. A low rolloff frequency improves the normal mode rejection, but at the expense of a longer settling time in response to input voltage step changes. Another consideration when an LCD bargraph is used is aliasing. If the bargraph is updated at 20 times per second and there is a 19Hz component in the signal being measured, the beat frequency of 1Hz will appear on the LCD bargraph display. To avoid aliasing effects, the filter time constant is normally set to less than 10Hz. A 3Hz rolloff (RC = 40ms) further reduces the aliasing effects and increases normal mode rejection while still maintaining an acceptable transient response with fast varying signals.

Dielectric absorption in the filter capacitors will create a small, long time constant settling error; therefore polypropylene capacitors are recommended.

Crystal, and Crystal Oscillator Capacitor

The MAX133/134 oscillator is designed to use high Q, low power 32,768Hz crystals such as the Statek CX-1V. The series resistance should be less than 30kΩ.

The oscillator capacitor connected to OSC2 is typically 10pF, but should be adjusted to optimize performance with the chosen crystal. If overtone oscillations are observed, then increase the value of the oscillator capacitor. If on the other hand, the oscillator has start-up problems, then reduce or eliminate the oscillator capacitor. Keep the stray capacitance across the crystal to a minimum since excessive stray capacitance will prevent oscillation.

Attenuator Network

The attenuator network and the associated range selection switches are shown in Figure 1. If the resistance of the internal range selection switches were 0Ω, then the theoretically ideal values for the attenuator network would be 10MΩ, 1.1111MΩ, 101.101kΩ, 10.01kΩ and 1.0001kΩ.

The voltage coefficient of the 10MΩ resistor should be as low as possible, since it will have high voltages applied to it in the 400V and 4,000V ranges. In addition, the temperature coefficients of the various attenuator resistors should be as low as practical since this affects the accuracy of the ohms measurements. The temperature coefficients of the attenuator resistors should track each other since the ratio of the resistor values sets the accuracy of the voltage measurements.

Input Attenuator Compensation Capacitors

The input attenuator is often compensated with low value capacitors to maintain a constant attenuation ratio over a wide bandwith. The value of the compensation capacitors should be as low as practical, otherwise the 10MΩ pin will be driven above V^+ or below V^- when high frequency, high voltage signals are applied to the attenuator input, causing gross conversion errors.

Positive Temperature Coefficient Resistor (PTC)

As shown in Figure 2, a PTC is normally used as part of the protection circuit in the ohms mode. Excessive values of PTC resistance, however, reduce the voltage across the unknown and reference resistors, particularly on the 400Ω range. PTC resistances above 2kΩ will degrade system performance by reducing the signal level on the 400Ω range, thereby increasing the conversion noise. Values above 5kΩ will cause additional error since the voltage drop across the PTC appears at the A/D as a common mode difference between IN HI and Ref LO.

Microprocessors

For low cost 2 chip digital multimeters, 4 bit microprocessors with LCD display drive capability are

3¾ Digit DMM Circuit

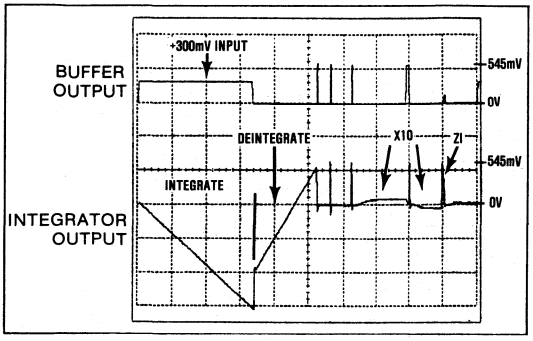


Figure 6. Buffer and Integrator Waveforms with Fullscale Positive Input Voltage

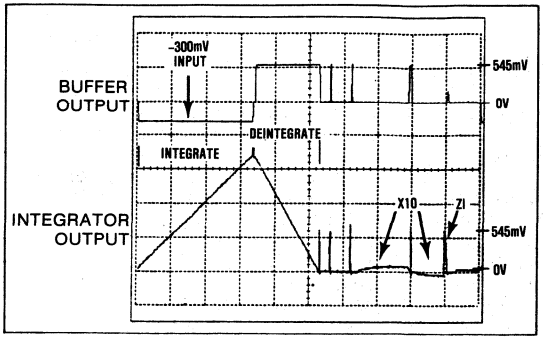


Figure 7. Buffer and Integrator Waveforms with Fullscale Negative Input Voltage

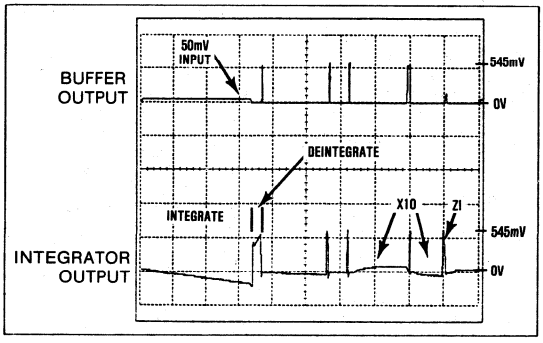


Figure 8. Buffer and Integrator Waveforms with a Small Positive Input Voltage

recommended. Typical 4 bit microprocessor families include the Sharp SM4 and SM5, the NEC μPD75XX family, and the Hitatchi LCD-III and LCD-IV families. If additional calculation power is needed, or if software development costs and time need to be minimized, then 8 bit microcontrollers such as the 8048, 8051 or 6803 should be used.

A/D Conversion Method and Timing

The MAX133/134 uses a "residue multiplication" technique to perform a ±40,000 count conversion in only 1638 clock cycles. Figures 6, 7 and 8 show typical integrator and buffer waveforms for a large positive, a large negative, and a small positive input voltage respectively.

Integration Phase

The unknown signal is integrated by connecting the non-inverting input of the integrator to IN LO, and the buffer input to In Hi. The integration period varies from 100 counts to 655 counts as shown in Table 5. The MAX133/134 is in the Zero Integration phase while in hold, between conversions, and before the start of the integration period.

Table 5. Integration Periods

MODE	INTEGRATION PERIOD (clock cycles)	
Voltage, 60Hz	545	(16.63ms)
Voltage, 50Hz	655	(19.99ms)
Voltage, 60Hz, ÷ 5	109	
Voltage, 50Hz, ÷ 5	131	
Ohms	500	
Ohms, ÷ 5	100	

$$\text{Digital Output Code} = \text{Integration Period} \times 100 \times \frac{V_{IN}}{V_{REF}}$$

where V_{IN} is the differential voltage applied to the A/D's internal In Hi and In LO, and V_{REF} is the differential voltage applied to the A/D's internal Ref Hi and Ref Lo.

First Deintegration Phase

The polarity of the first Deintegrate phase is determined by polarity of the voltage on the integration capacitor at the end of the integration period. Figure 9 shows the MAX133/134 A/D section. Note that no reference capacitor is needed, thereby improving the response time in ohms measurement. Also note that since the non-inverting input of the integrator is connected to Ref Hi for a positive deintegration, the voltage at the integrator output will have a step voltage change equal to the reference voltage.

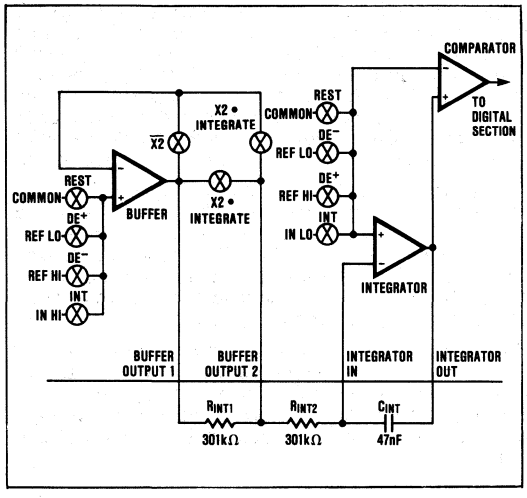


Figure 9. A/D Analog Section.

The first deintegration phase terminates when the comparator detects that the integration capacitor has been discharged. The MAX133/134 then goes into an "Idle" state where both the buffer input and the non-inverting input of the integrator are connected to common. This causes the system offset to be integrated.

Near the end of the maximum allowable deintegration period, the polarity of the voltage on the integration capacitor is again tested and either a positive or negative deintegration cycle occurs.

Times 10 (X10) Phase

When zero crossing is detected at the end of a deintegration phase the deintegration is continued until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. Any comparator delay causes an additional residual voltage on the integration capacitor. The times 10 phase inverts and multiplies this residual by a factor of 10.

Second Deintegration Phase

The second deintegration phase deintegrates the residual voltage on the integration capacitor that has been inverted and multiplied by 10 in the X10 phase. Note that, since the voltage across the integration capacitor has been multiplied by 10, each clock cycle of deintegration during the second deintegration corresponds to 1/10 of one clock cycle during the first deintegration.

Second X10 and Third Deintegration

The residual voltage left on the integration capacitor after the second deintegrate phase is multiplied by the second X10 phase, and this multiplied residual is deintegrated in the third deintegration phase. Since the residual voltage on the integration capacitor has twice been multiplied by 10, the third deintegration phase has 100 times finer resolution than does the first deintegration phase.

Sequence Counter and Results Counter

The sequencing or timing of the various conversion phases are controlled by a binary sequence counter. This counter counts upward continuously except during the hold mode. Some phases, such as the integration periods, are both started and stopped at preset counts. The deintegration phases are started at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegration phases. It is an up/down BCD counter, with the count direction being determined by the deintegration polarity. The first deintegration phase causes the results counter to count by hundreds. Since the second deintegration phase is deintegrating a residual voltage that has been multiplied by 10, the results counter is incremented or decremented by tens during the second deintegration phase. The results counter is incremented or decremented by ones during the third deintegration phase. The content of the results counter is transferred to the results register at the end of each conversion.

Application Notes

Sleep and Hold Mode

The Hold mode stops the internal sequence counter at the end of the next conversion but does not turn off the oscillator or any analog circuitry. The Hold mode can be used to speed up autoranging — see "Autoranging", below. Dielectric absoption in the integration capacitor will cause the first two or three readings after an extended Hold period to have a lower magnitude than the steady state reading.

The Sleep mode puts the MAX133/134 into a low power quiescent mode by shutting off all analog circuitry except the DGND power supply and the oscillator. A typical use of the Sleep mode is to reduce power consumption by turning off the MAX133/134 if the meter is idle for a long period. A

3¾ Digit DMM Circuit

typical method of detecting when the meter is no longer being used is to detect when the reading stays constant and there are no operator inputs such as range or mode changes for an extended period.

Since the Sleep mode turns off all analog circuitry, the first conversion after coming out of the sleep mode is not valid. It will take several readings before the reading has stabilized to within 1 count.

Input Protection for Digital Multimeters

Figure 2 shows a typical multimeter input circuit for ohms measurement. The positive temperature coefficient (PTC) thermistor normally has a resistance of only 2kΩ, but under overload conditions it limits the fault current since the fault current heats the PTC, thereby increasing its resistance several orders of magnitiude. Protection on the voltage ranges is automatic, since the 10MΩ input resistor will limit the input current to safe limits, even with 4000V applied. Current ranges must be protected with fuses or circuit breakers, and the current sense resistors should be bypassed with diodes to limit the voltage drop across the current sense resistors to no more than 2 diode drops.

External AC-DC Converter

Figure 10 shows a typical half wave external AC-DC converter. This circuit is an average-sensing, RMS-calibrated AC-DC converter. This means that the output is proportional to the average AC value rather than the RMS value, but that the output has been multiplied by the 1.11 to correct for the ratio of the average voltage to the RMS voltage of a sine wave. If desired, a true RMS to DC converter can be connected between Ext AC Out and Ext AC In.

Printed Circuit Board Layout

Since the integrator output makes common mode voltage steps equal to the reference voltage to perform a positive deintegration, any stray capacitance on the integration capacitor will cause errors. Stray capacitive loading on the Buffer output should also be minimized to avoid ringing on the buffer output.

The Integrator In node is particularly sensitive to stray pickup of noise and 50/60Hz, therefore C_{INT} should be located as near as possible to the Integrator In pin.

Minimize capacitance on the node that joins the two R_{INT} resistors since this capacitance sets up an RC time constant that rounds off the edges of the input to the integrator and can cause errors. If the times 2 mode is not used, then connect a single R_{INT1} directly from Buff OUT1 to the Integrator In pin. Locate the R_{INT1} resistor as close as possible to the Integrator In pin since the Buffer Output is a low impedance point while the Integrator In pin is a high impedance point.

Any resistance between the MAX133/134 1kΩ pin and the 1kΩ resistor adds the effective value of the 1kΩ resistor, as does any voltage drop between the 1kΩ resistor and the In Lo pin. These resistances should be minimized and/or the 1kΩ resistor value should be reduced to compensate for the resistance of the printed circuit board connections.

The effective resistance of any current sensing resistors is affected by where the voltage is sensed. Connect In Lo directly to one end of the current sensing resistor to avoid errors caused by voltage drops in the Common traces on the printed circuit board.

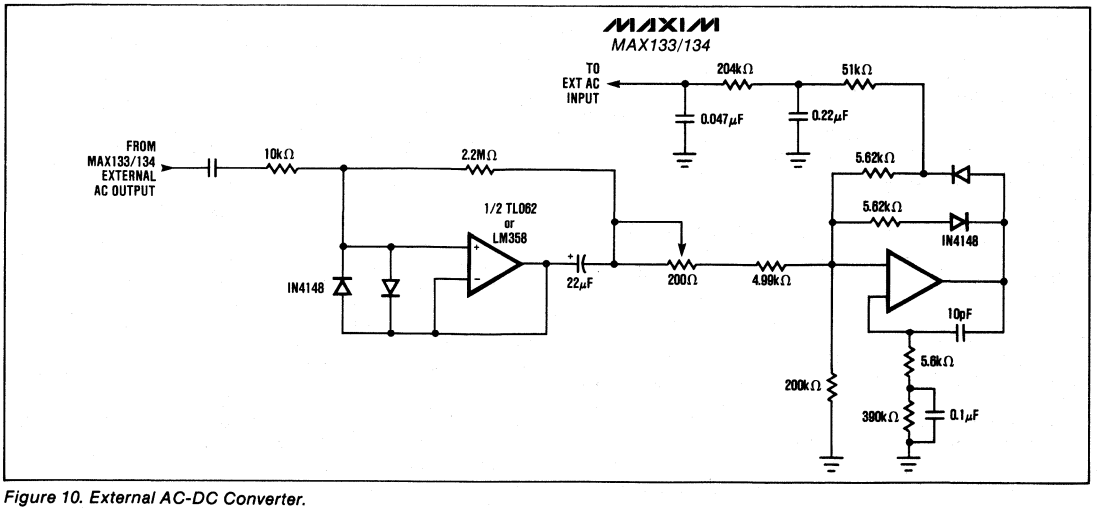


Figure 10. External AC-DC Converter.

Software Notes

Autoranging

The sequence in which the registers are loaded has no effect provided that all registers are loaded before the next end of conversion. Control bits take effect only when the MAX133/134 is in Hold or completes the current conversion. If the MAX133/134 runs continuously, the autoranging sequence will be as shown in Figure 11A. If the MAX133/134 is put into the hold mode during autoranging the autoranging time can be reduced in those cases where several ranges must be tried. See Figure 11B. A simple test that detects most overrange readings is to check if the most significant digit (Register 4) is greater than ±45. A second test of the zero-corrected reading should also be performed to make sure that it is within the desired full scale range.

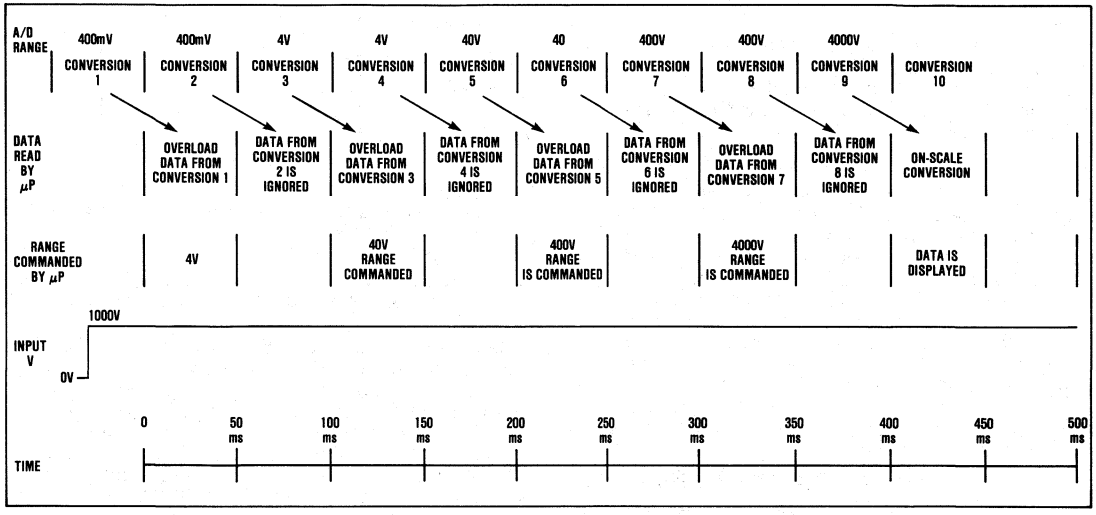


Figure 11a. Autoranging with MAX133/134 Running Continuously

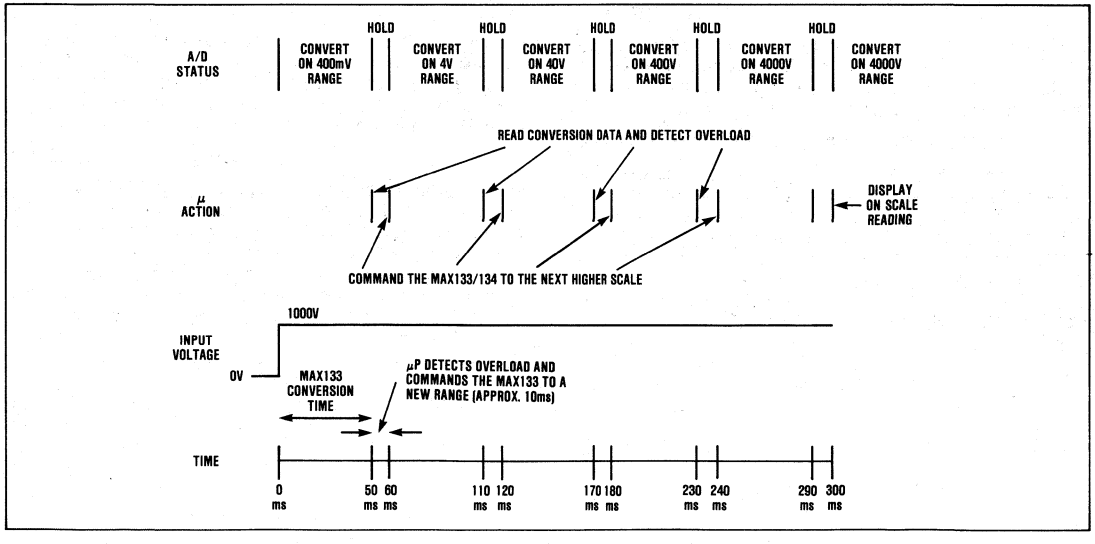


Figure 11b. Autoranging With Hold Between Conversions

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Reduction of Conversion Noise by Averaging Readings

The MAX133/134 has approximately ±1 counts of noise. In most cases where only 4000 counts are being displayed, averaging is not required since the noise is only 1/10 of one displayed count. In data acquisition systems where the full resolution is being used, averaging N readings will reduce the noise by a factor of

$\sqrt{N}$.

Since the noise of zero-corrected readings is the RMS sum of the noise of both the Read Zero reading and the normal reading, the Read Zero offset correction should also be averaged if optimum noise performance is desired.

BCD to Binary Conversion

Normally, if only a zero correction or tare correction is to be applied to the output of the MAX133/134, then the conversion result is left in the BCD format. If a scale factor or gain correction is to be made, the result is usually converted to a binary format. Any of the standard BCD to binary conversion algorithms can be used. A simple method of conversion is to read the MAX133/134 conversion result starting with the most significant digit. Put the most significant digit's result into a multi-byte accumulator and multiply it by 10. Then read the next digit's result and add it to the accumulator. Repeat the "multiply-read-add" sequence for all 5 digits.

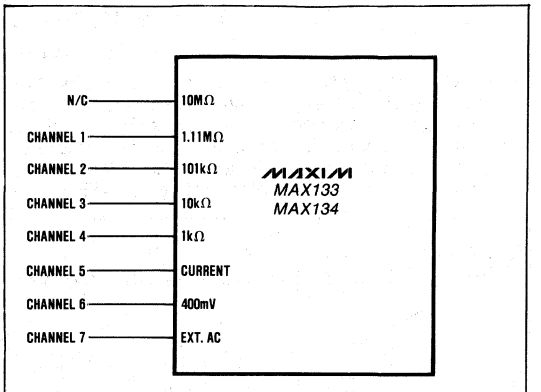
Using the MAX133/134 in Data Acquisition Systems

Using the Input Attenuator Inputs as a Multiplexer

In many data acquisition applications the voltage range is limited, and the 400mV to 4000V attenuator is not needed. In these cases, the input switches can be used as a multiplexer as shown in Figure 12.

Using Non-standard Voltage Ranges

In many data acquisition systems the voltage to be measured may have a full scale range other than 400mV, 4V, etc. For maximum resolution, the full scale range of the MAX133/134 should be adjusted to match the input signal voltage span. This can be done either through attenuation/amplification of the signal to make it match the ±400mV basic span of the MAX133/134, or by adjusting the MAX133/134 voltage span.



NOTES:
1. Channels 5 and 6 are connected to Common via a 5kΩ resistor when they are not selected.
2. Voltage Span is ±400mV.

Figure 12. MAX133/134 Input Section used as a Multiplexer.

Table 5 shows the integration periods of the various conversion modes. These different modes can be used to change the full scale span of the MAX133/134. If for example the reference voltage is 545mV, setting the 50Hz bit changes the integration time to 655 clock cycles and the 400mV full scale range becomes a 545/655 x 400mV = 333mV full scale range. Activating the ÷5 bit increases the full scale span by a factor of 5, while setting the X2 bit decreases the full scale span by a factor of 2 (assuming $R_{INT1} = R_{INT2}$).

In all cases, the values of R_{INT1}, R_{INT2}, and C_{INT} should be chosen so that integrator swing is at least 2V, and integrator current is always less than 3μA both during deintegrate and during integrate with a full scale input voltage. The common mode voltage range of IN Hi and In Lo is from (V^- +1.5V) to (V^+ -1.0V).

Unipolar Operation

Unlike most integrating A/Ds, the MAX133/134 does not have extra non-linearities around zero. This allows the use of the full 80,000 count resolution to measure unipolar signals. All that is needed is a resistive offset network to translate the unipolar signal so that it becomes bipolar. An external zero circuit must be included so that errors in the offset resistor can be

SELECTED CHANNEL	10^{-1}	10^{-2}	10^{-3}	10^{-4}	DIVIDER SENSE	CURRENT	DC	EXT AC
1	1	0	0	0	1	X	1	0
2	0	1	0	0	1	X	1	0
3	0	0	1	0	1	X	1	0
4	0	0	0	1	1	X	1	0
5	0	0	0	0	0	1	1	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	X	X	0	1

0 = set to 0 1 = set to 1 X = Don't Care

measured and subtracted. Note that the zero correction software is the same as would be used to correct for the internal zero error of the MAX133/134, except that in this case the external zero offset will be nearly 40,000 counts.

Ratiometric Measurements of Load Cell and Strain Gauges

In many weigh scale, pressure transducer, and load cell applications ratiometric measurements are desired. If the reference voltage is referenced to the ground or Common pin, then simply connect the reference voltage to the Ref In pin, connect the voltage to be measured to In Hi and In Lo and perform any of the voltage mode conversions. If, on the other hand, the reference voltage is a differential signal, use the circuit of Figure 13 and select the ohms measurement mode. Note that the non-inverting input of the integrator will be connected to either Ref Lo or REF Hi during deintegration. The integrator swing should be reduced if the integrator output goes within 0.5V of either V^+ or V^-. In no case should either Ref Hi or Ref Lo be lower than (V^- + 1.5V) or higher than (V^+ – 1.0V).

Operation with Clock Frequencies Other Than 32,768Hz

Operation with clock frequencies lower than 32kHz slightly improves the noise performance, while at the same time reducing the reading rate proportionately. With clock frequencies less than 10kHz, leakages during the X10 phase will introduce differential linearity errors at high temperatures.

Clock frequencies higher than 50kHz are not recommended since the X10 period will not completely settle within its allotted time period, causing differential nonlinearity errors. Another potential problem at very high clock frequencies is that, although the comparator delay is a fixed time period, it increases in terms of clock cycles as the clock frequency increases. At very high clock frequencies the residue cannot be fully deintegrated in the allotted number of clock cycles after having been multiplied by 10 in the X10 phase.

When using a clock frequency other than 32,768Hz, change the value of the integration capacitor C_{INT} to keep integrator swing at approximately 2V.

Converting the Times 2 Mode to a ± 40mV Full Scale Range

The sensitivity of the times two mode is increased by the factor

$$\frac{R_{INT1} + R_{INT2}}{R_{INT1}}$$

In the normal DMM aplication $R_{INT1} = R_{INT2}$ and the X2 mode increases the sensitivity of the MAX133/134 by a factor of 2. If the two resistors have a 9 to 1 ratio, the X2 bit will increase the sensitivity of the MAX133/134 by a factor of 10. This can be used to get 1μV resolution on a 40mV scale.

Disabling the Active Filter

Since the signal source impedance in many data acquisition systems is very low, the value of the filter resistors, $R_{FILTER1}$ and $R_{FILTER2}$, can be lowered to reduce the error caused by the leakage current of the A/D flowing through $R_{FILTER1}$. If rapid settling is needed in a multichannel data acquisition system, then the filter should be disabled by leaving the pins Filter Resistor In and Filter Resistor Out open, and shorting Filter Amp Out to Filter Amp In. Do not leave the filter amplifier connection open circuited, since oscillations may occur.

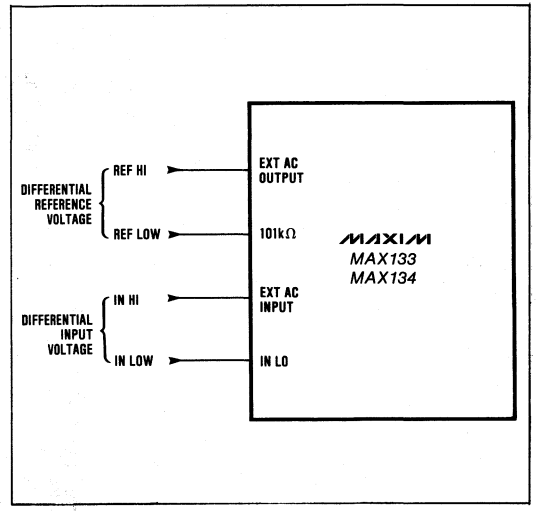


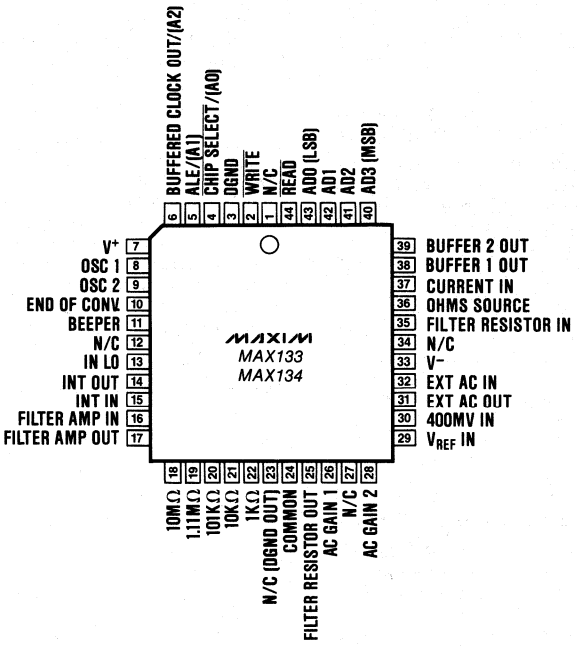
Figure 13. Configuration for Differential Reference Input.

BIT PATTERN					
10^{-0} TO 10^{-4}	R/2	DIVIDER SENSE	CURRENT	DC	EXT AC
0	1	1	0	0	1

3¾ Digit DMM Circuit

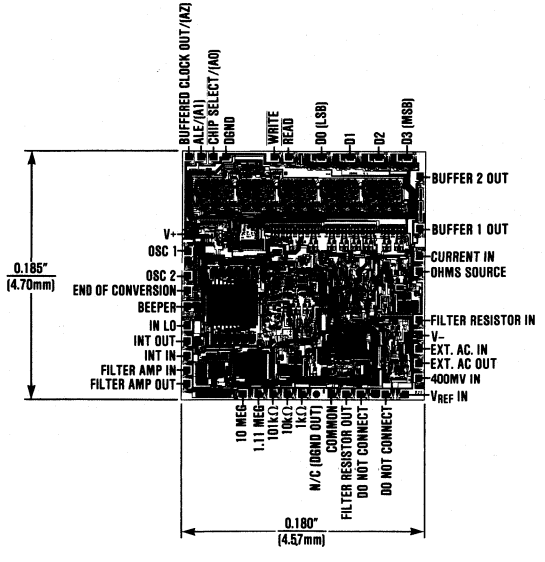
Pin Configuration

TOP VIEW



Pin Names in parentheses are for MAX134 only.

Chip Topography



MAXIM

Low Power, 3½ Digit A/D Converter With Display Hold

General Description

The Maxim MAX136 is a monolithic analog to digital converter with very high input impedance. It differs from the Maxim ICL7136 in that the MAX136 provides a Hold pin, which makes it possible to hold or "freeze" a reading. The MAX136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external drive circuitry. With minor external component changes, it is pin compatible with the ICL7116 but with significantly reduced power consumption, making the MAX136 a superior device for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. True differential inputs allow direct measurements of bridge transducer outputs or load cells. The zero-integrator phase eliminates overrange hangover and hysteresis effects. The MAX136 offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

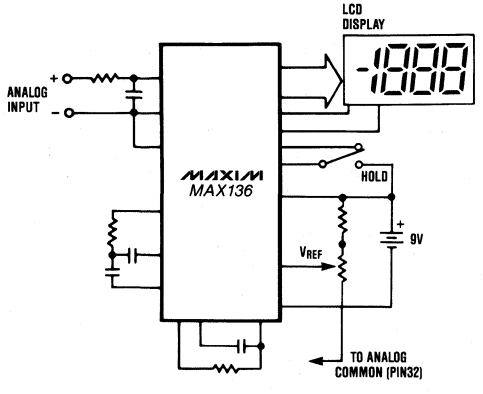
Features

- **Power dissipation guaranteed less than 1mW-9V battery life 3000 hours typical**
- **Hold pin allows indefinite display hold**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**
- **Key Parameters Guaranteed over Temperature**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX136CPL	0°C to +70°C	40 Lead Plastic DIP
MAX136CJL	0°C to +70°C	40 Lead CERDIP
MAX136CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX136C/D	0°C to +70°C	Dice

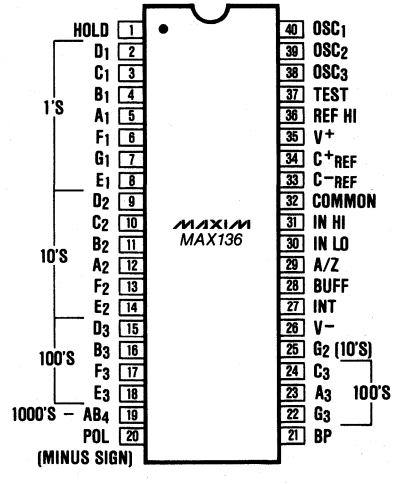
Typical Operating Circuit



(Detailed Circuit Diagram—See 3rd page)

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

Low Power, 3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input, Hold Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 800mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±1mA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1 unless noted.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 999 998	 999/1000 999/1000	 1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 -1	 ±0.2 ±0.2	 +1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	 -1	 ±0.2	 +1	Counts
Common Mode Rejection Ratio (Note 7)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		 5		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		 10		µV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C		 1 20	 10 200	pA
Zero Reading Drift	V_{IN} = 0, 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C 0° ≤ T_A ≤ 70°C		80	 150 200	µA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply	250kΩ between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1			1000		MΩ
V_{IL}, Pin 1				TEST +1.5	V
V_{IH}, Pin 1		V^+ -1.5			V
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V (Note 8)	4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V
Overload Recovery Time (Note 5)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 3: Test condition is V_{IN} applied between pins IN-HI and IN-LO, i.e., 1MΩ resistor in Figures 1 and 2.
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015 .2)
Note 5: Number of measurement cycles for display to give accurate reading.
Note 6: 1MΩ resistor is removed in Figures 1 and 2.
Note 7: Refer to "Differential Input" discussion (See Maxim's ICL7136 data sheet).
Note 8: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Detailed Description

The Maxim MAX136 3½ digit A/D converter is similar to the Maxim ICL7136 except for the addition of a Hold pin. For a detailed product description, and applications information (other than the operation of the Hold pin described below), refer to Maxim's ICL7136 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test. The MAX136 continuously performs conversions, independent of the Hold input. When the Hold input is at V^+ the display latch pulse is inhibited, and the display latches are not updated; when the Hold input is low or at the Test voltage, the display is updated at the end of each conversion. The MAX136 maintains low power dissipation even during display hold by eliminating the pull-down resistor between Hold and Test present on the ICL7116. The Hold input is CMOS compatible, and can also be driven by a switch connected between Test and V^+ (Figure 1).

Reference Input

Unlike the ICL7136, the MAX136 does not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

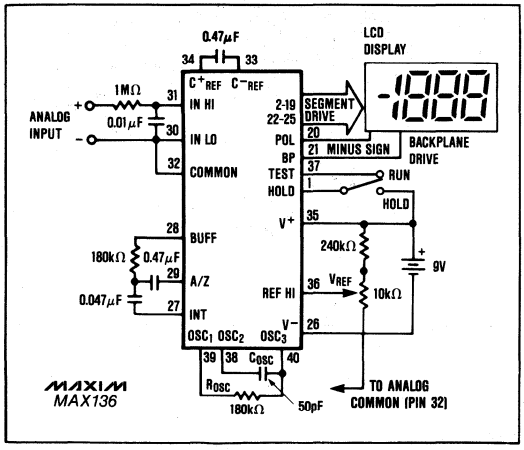


Figure 1. Maxim MAX136 Typical Operating Circuit, 200mV Full Scale.

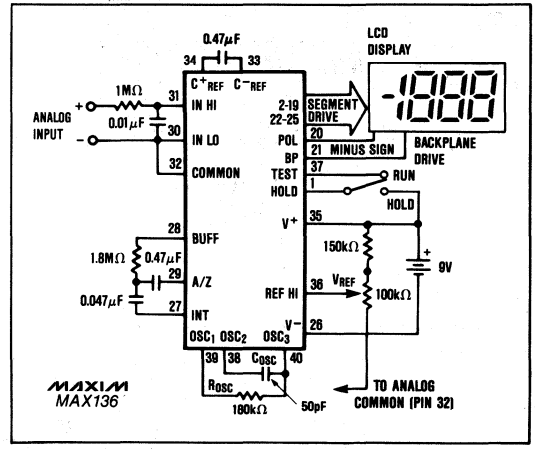
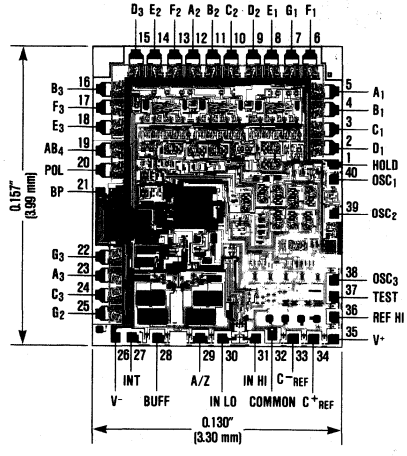
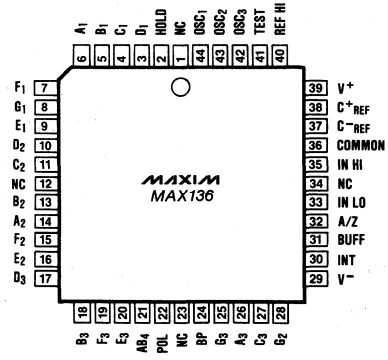


Figure 2. Maxim MAX136 Typical Operating Circuit, 2.0V Full Scale.

Chip Topography



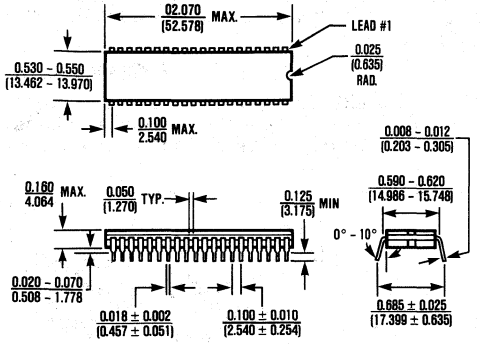
Pin Configuration



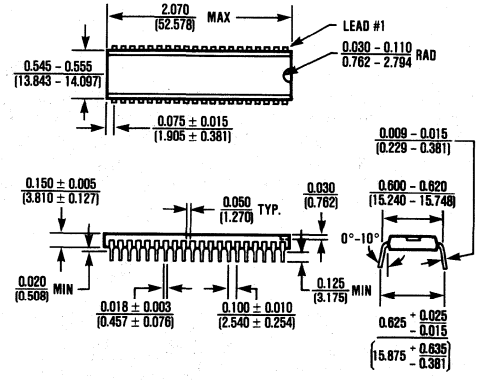
44 Lead Plastic Chip Carrier (Quad Pack)

Low Power, 3½ Digit A/D Converter With Display Hold

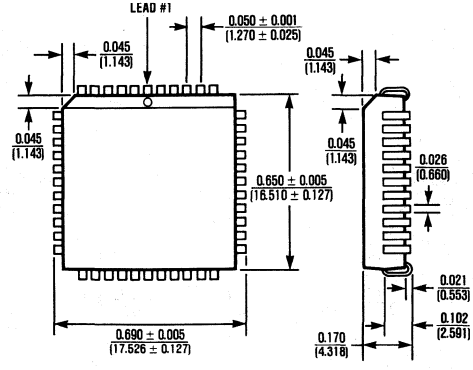
Package Information



40 Lead CERDIP (JL)
θ_{JA} = 45°C/W
θ_{JC} = 20°C/W



40 Lead Plastic DIP (PL)
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W



44 Lead Plastic Chip Carrier (Quad Pak) (QH)
θ_{JA} = 80°C/W
θ_{JC} = 40°C/W

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

General Description

The MAX150/AD7820 is a high speed, microprocessor compatible, 8 bit analog to digital converter which uses a half-flash technique to achieve a conversion time of 1.34 μs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/μs. The MAX150 also provides an on-chip 2.5 V reference output, making it a complete analog to digital converter.

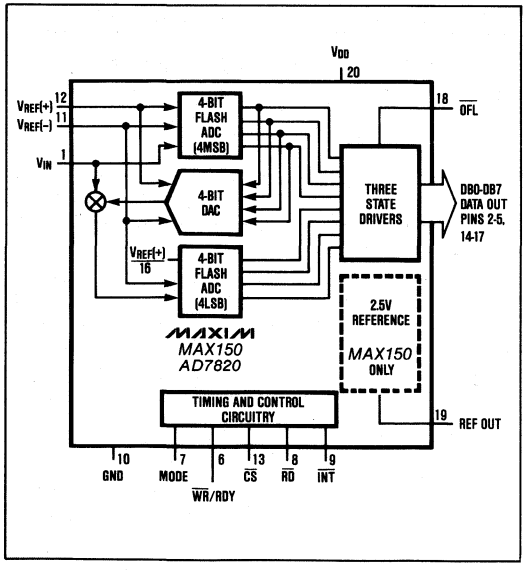
The A/Ds easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. An over-flow output is also provided for cascading devices to achieve higher resolution.

The AD7820 is pin compatible with Analog Devices' AD7820. The MAX150 is also compatible with the AD7820 but also includes an internal 2.5V reference.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Functional Block Diagram



Features

- Fast Conversion Time: 1.34μs Max.
- Built-in Track-and-Hold Function
- No Adjustment Required
- No External Clock
- Single +5V Supply
- Easy Interface To Microprocessors
- Internal 2.5V Reference (MAX150 only)

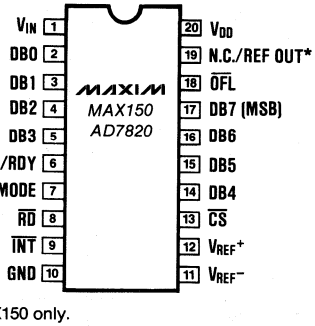
Ordering Information

PART	TEMP. RANGE	PACKAGE†	ERROR
MAX150ACPP	0°C to +70°C	Plastic DIP	±½ LSB
MAX150BCPP	0°C to +70°C	Plastic DIP	±1 LSB
MAX150BC/D	0°C to +70°C	Dice*	±1 LSB
MAX150ACWP	0°C to +70°C	Small Outline	±½ LSB
MAX150BCWP	0°C to +70°C	Small Outline	±1 LSB
MAX150AEPP	-40°C to +85°C	Plastic DIP	±½ LSB
MAX150BEPP	-40°C to +85°C	Plastic DIP	±1 LSB
MAX150AEWP	-40°C to +85°C	Small Outline	±½ LSB
MAX150BEWP	-40°C to +85°C	Small Outline	±1 LSB
MAX150AMJP	-55°C to +125°C	CERDIP	±½ LSB
MAX150BMJP	-55°C to +125°C	CERDIP	±1 LSB

† *All devices — 20 lead packages*
* *Consult factory for dice specifications.*
Ordering Information continued on last page

Pin Configuration

Top View



*MAX150 only.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +75°C by ..... 6mW/°C

Operating Temperature Ranges
MAX150XCXX, AD7820LN/KN/LCWP/KCWP ... 0°C to +70°C
AD7820BQ/CQ ..... -25°C to +85°C
MAX150XEXX ..... -40°C to +85°C
MAX150XMXX, AD7820TQ/UQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX150A, AD7820L/C/U MAX150B, AD7820K/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
REFERENCE OUTPUT MAX150 ONLY (Note 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	V
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	mV
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	mV
Temperature Drift (Note 3)		**MAX150XC T_A = 0°C to +70°C MAX150XE T_A = -40°C to +85°C MAX150XM T_A = -55°C to +125°C**		**40 40 60**	**70 70 100**	ppm/°C
Output Noise				**200**		µV/rms
Capacitive Load					**0.01**	µF
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V T_A = +25°C T_A = T_{MIN} to T_{MAX}			±0.3 ±3	µA
Slew Rate, Tracking (Note 4)	SR			0.2	0.1	V/µs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$; MAX150 AD7820 MODE	2.0 2.4 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C T_{MIN} to T_{MAX} $\overline{WR}$; T_A = +25°C T_{MIN} to T_{MAX} MODE; T_A = +25°C T_{MIN} to T_{MAX}		 50	0.3 1 0.3 3 150 200	µA

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} - 25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC INPUTS (continued)						
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE T_A = +25°C T_{MIN} to T_{MAX}			-0.3 -1	µA
Input Capacitance (Note 5)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V I_{OUT} = -360µA V_{DD} = +4.75V I_{OUT} = -10µA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0-DB7, RDY T_A = +25°C T_{MIN} to T_{MAX}			±0.3 ±3	µA
Output Source Current	I_{SRC}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0	-10	-25		mA
Output Sink Current	I_{SINK}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}	15	40		mA
Output Capacitance (Note 5)	C_{OUT}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	+5V ±5% for specified performance	4.75		5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

Note 5: Guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input; range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50µA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.

PIN	NAME	FUNCTION
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	TP REF OUT	Test pin for AD7820. No Connection. 2.5V Internal reference output for MAX150 only.
20	V_{DD}	Power supply voltage, +5V.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

TIMING CHARACTERISTICS (Note 1, 2) — MAX150, AD7820

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX150C/E AD7820K/L/B/C		MAX150M AD7820T/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to $\overline{RDY}$ Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}			1.2	1.6		2.0		2.5	µs
Data Access Time (RD Mode) (See Figure 4)	t_{ACC0}	(Note 3)		t_{CRD} + 10	t_{CRD} + 20		t_{CRD} + 35		t_{CRD} + 50	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 4)		40	60		80		100	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time ($\overline{WR}$/$\overline{RD}$ Mode)	t_{CWR-RD}		1.34			1.5		1.53		µs
Delay between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		600			700		700		ns
Data Access Time ($\overline{WR}$/$\overline{RD}$ Mode) (See Figure 6)	t_{ACC1}	$t_{RD} < t_{INTL}$, (Note 3)		110	160		225		250	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}			100	140		200		225	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time ($\overline{WR}$/$\overline{RD}$ Mode) (See Figure 5)	t_{ACC2}	$t_{RD} > t_{INTL}$, (Note 3)		60	70		90		110	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After $\overline{INT}$	t_{ID}			10	50		65		75	ns

Note 1: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 2: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 3: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 4: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

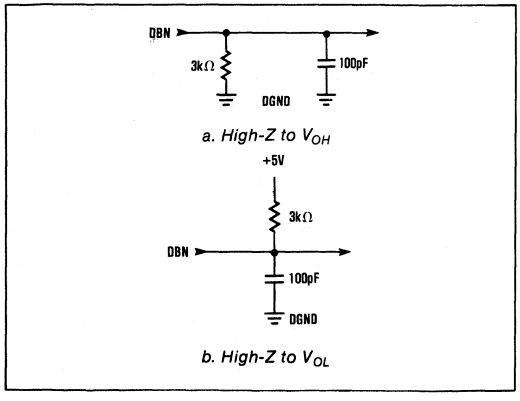


Figure 1. Load Circuits for Data Access Time Test

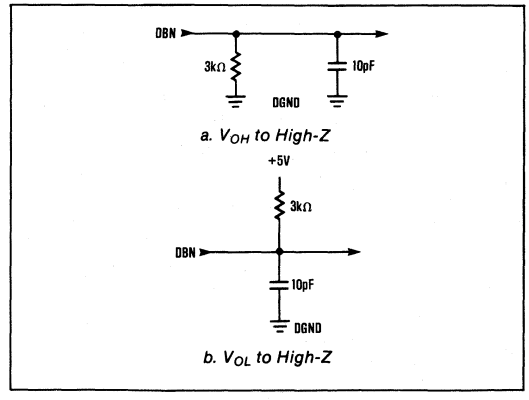
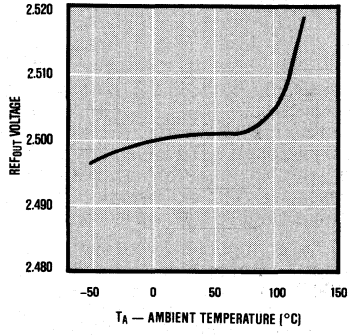


Figure 2. Load Circuits for Data Hold Time Test

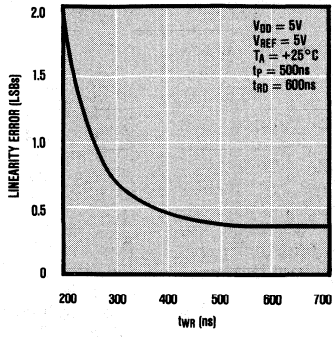
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Typical Operating Characteristics

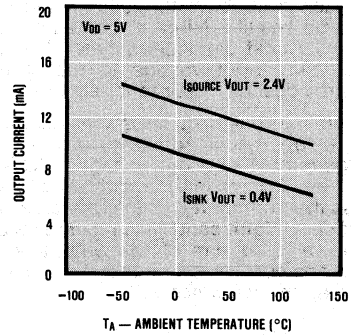
REFERENCE TEMPERATURE DRIFT (MAX150 ONLY)



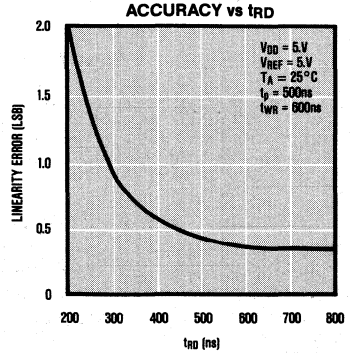
ACCURACY vs. tWR



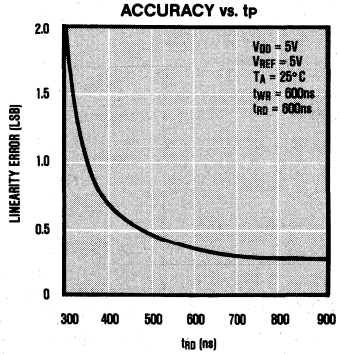
OUTPUT CURRENT vs. TEMPERATURE



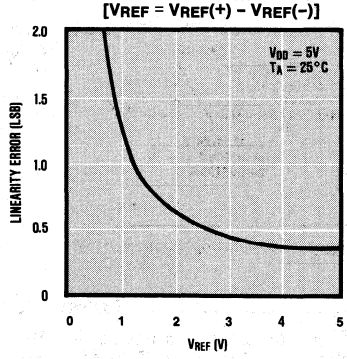
ACCURACY vs tRD



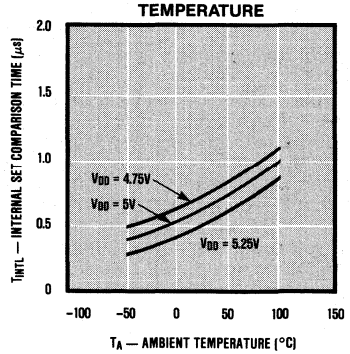
ACCURACY vs. tP



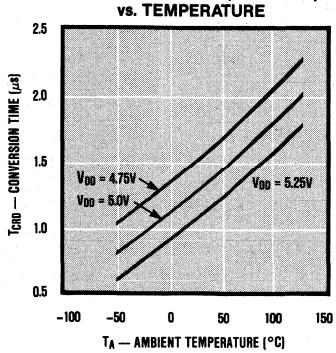
ACCURACY vs. VREF [VREF = VREF(+) - VREF(-)]



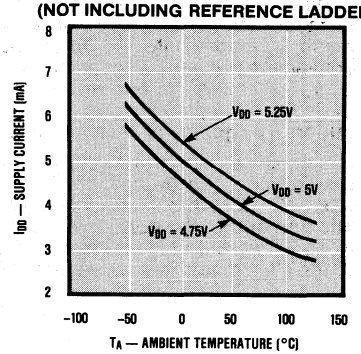
tINTL INTERNAL TIME DELAY vs. TEMPERATURE



CONVERSION TIME (RD MODE) vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



1

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Detailed Description

Converter Operation

The MAX150/AD7820 uses a "half-flash" conversion technique (see Functional Block Diagram). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper 4-bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate the analog result from the first flash conversion, and generates a residue voltage which is the difference of the unknown input and the DAC voltage. The residue is then compared to the reference ladder using 15 LS (least significant) flash comparators to obtain the lower four bits of the output. An additional overrange comparator detects if the analog input is greater than the reference voltage.

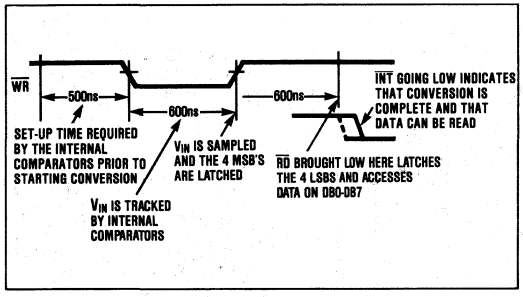


Figure 3. Operating Sequence (WR-RD Mode).

Operating Sequence

The operating sequence for the WR-RD Mode is shown in Figure 3. The conversion is initiated by a falling edge of $\overline{WR}$. The comparator inputs track the analog input voltage for the duration of $\overline{WR}$ low. A minimum of 600ns is required for the input voltage to be acquired. When $\overline{WR}$ returns high, the MS flash result is latched into the output buffers and the LS conversion begins. $\overline{INT}$ goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 data bits are latched into the output buffers. $\overline{RD}$ going low then accesses the data.

If an externally controlled conversion time is required, the $\overline{RD}$ line can be brought low as soon as 600ns after $\overline{WR}$ goes high. This will latch the lower 4 data bits and output the conversion result on DB0-DB7. At least 500ns setup time is required from $\overline{INT}$ going low to the start of another conversion ($\overline{WR}$ going low).

Digital Interface

The MAX150/AD7820 has two basic interface modes which are set by the status of the MODE input pin. When this pin is low, the converter is in the RD mode, when this pin is high the converter is set up for the WR-RD mode.

RD Mode

In RD mode, conversion control and data access is controlled by the $\overline{RD}$ input (see Figure 4). The conversion is initiated by taking $\overline{RD}$ low. $\overline{RD}$ is then kept low until output data appears. This mode is useful for microprocessors which can be forced into a WAIT state. The processor can start a conversion, wait, and then read data with a single READ instruction.

Pin 6 ($\overline{WR}$/RDY) is configured as a status output (RDY) in $\overline{RD}$ mode. This output can be used to drive the READY or WAIT input of a processor. RDY is an open collector output (with no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion. An $\overline{INT}$ output is also provided which goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

WR-RD Mode

In the WR-RD mode, pin 6 ($\overline{WR}$/RDY) is configured as the WRITE input for the converter. With $\overline{CS}$ low, a conversion is initiated on the falling edge of $\overline{WR}$. Several options exist for reading the data from the converter.

Using Internal Delay

In the first of these options the processor waits for $\overline{INT}$ output to go low before reading the data (Figure 5). $\overline{INT}$ typically goes low 600ns after the rising edge of $\overline{WR}$, indicating that the conversion is complete and the result is available in the output latch. With $\overline{CS}$ low, data outputs DB0-DB7 can be accessed by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset by the rising edge of $\overline{CS}$ or $\overline{RD}$.

Reading Before Delay

An alternative option can be used to externally control the conversion time (see Figure 6). The internally generated 600ns delay varies somewhat with temperature and supply voltage (see Typical Operating Characteristics) and can be overridden with $\overline{RD}$. To achieve this, the status of $\overline{INT}$ is ignored and $\overline{RD}$ is brought low as soon as 600ns after the rising edge of $\overline{WR}$. This completes the conversion and enables the output buffers, DB0-DB7, which contain the conversion result. $\overline{INT}$ also goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Pipelined Operation

In addition to the two standard WR-RD mode options, "pipe-lined" operation can be achieved by tying $\overline{WR}$ and $\overline{RD}$ together (see Figure 7). With $\overline{CS}$ low, $\overline{WR}$ and $\overline{RD}$ going low initiates a conversion, and reads the result of the previous conversion at the same time.

Stand-Alone Operation

The converter can also be used in a stand-alone operation (see Figure 8). $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low. Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

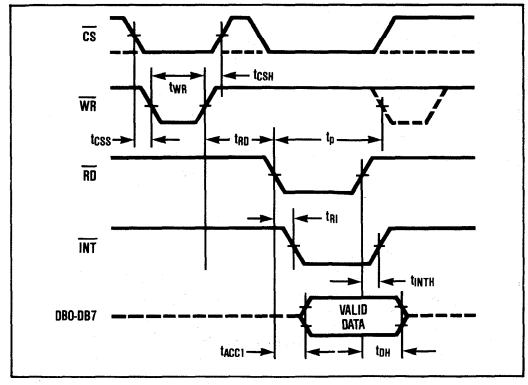


Figure 6. WR-RD Mode Timing ($t_{RD} < t_{INTL}$).

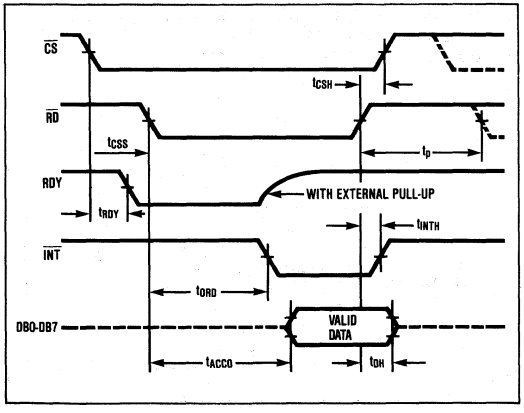


Figure 4. RD Mode Timing.

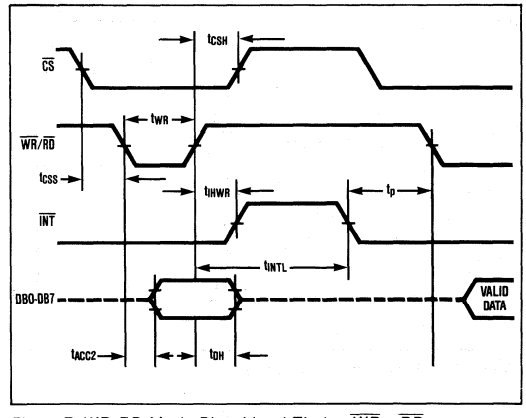


Figure 7. WR-RD Mode Pipe-Lined Timing $\overline{WR} = \overline{RD}$.

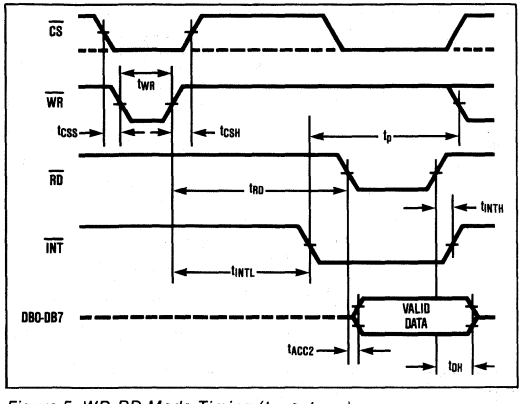


Figure 5. WR-RD Mode Timing ($t_{RD} > t_{INTL}$).

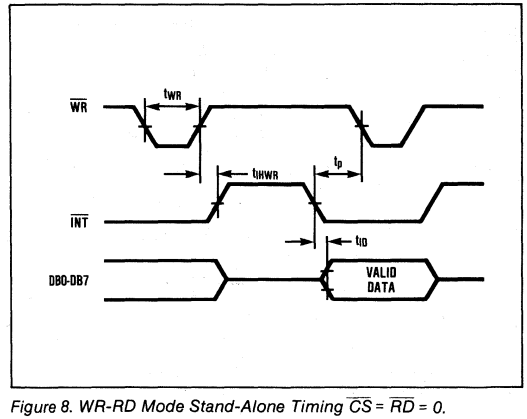


Figure 8. WR-RD Mode Stand-Alone Timing $\overline{CS} = \overline{RD} = 0$.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

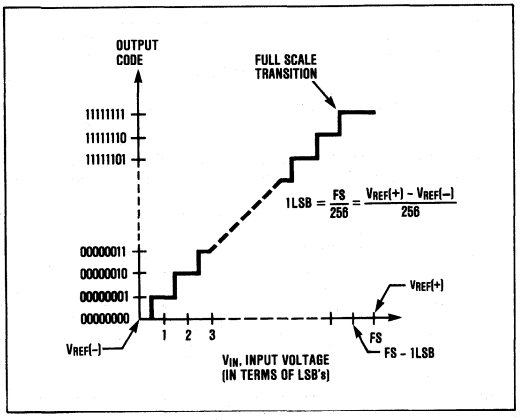


Figure 9. Transfer Function.

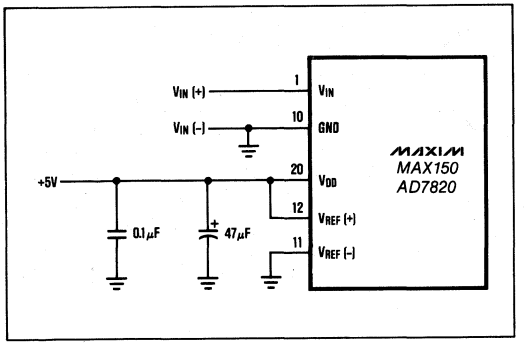


Figure 10a. Power Supply as Reference.

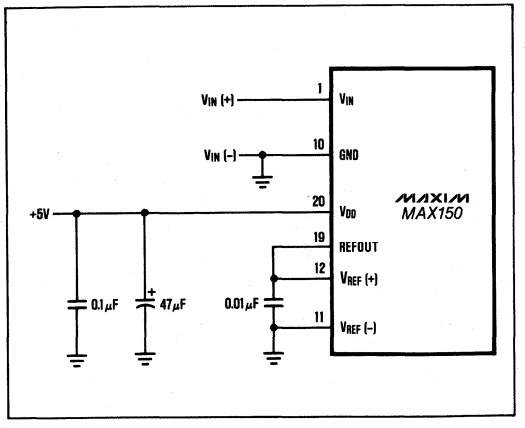


Figure 10c. Internal Reference (MAX150 only).

Analog Considerations

Reference

The MAX150 includes an internal 2.5V reference (REFOUT) which is appropriate for the majority of 8 bit measurement applications. To use the on-chip reference, connect REFOUT, pin 19, to V_{REF}^+, pin 12, and connect V_{REF}^-, pin 11, to ground. The 2.5V output is referred to GND, pin 10. Both the MAX150 and the AD7820, which does not have an on-chip reference, can be used with an external reference if desired.

Figure 10 shows some possible reference connections. For the MAX150, a 0.01μF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer.

The V_{REF}^+ and V_{REF}^- inputs of both converters set the full-scale and zero Input voltages of the A/D. In other words, the voltage at V_{REF}^- defines the input which produces an output code of all zeroes, and the voltage at V_{REF}^+ defines the input which produces an output code of all ones (see Figure 9).

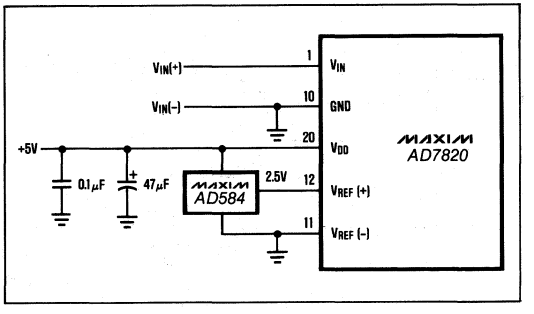


Figure 10b. External Reference 2.5V Full-Scale.

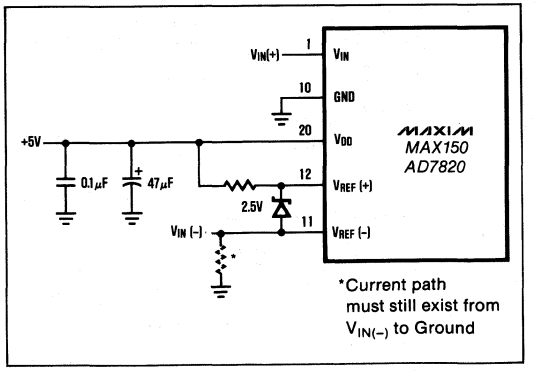


Figure 10d. Input Not Referenced to GND.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors should have the minimum possible lead length. Excess lead length may contribute to conversion errors and instability.

If the reference inputs (pins 11, 12) are driven by long lines, they should be bypassed to GND with 0.1 μF capacitors at the V_{REF} pins.

Input Current

The MAX150/AD7820 analog input behaves somewhat differently from conventional A/D converters. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in.

The equivalent circuit of the converter is shown in Figure 11. When the conversion starts and $\overline{WR}$ is low, V_{IN} is connected to the MS and LS comparators. Thus, V_{IN} is connected to thirty-one 1pF capacitors.

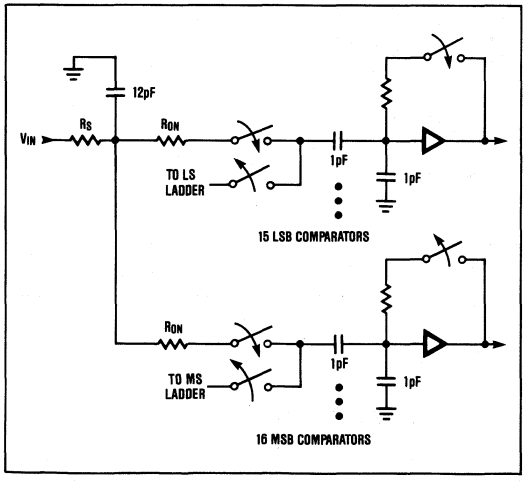


Figure 11a. Equivalent Input Circuit.

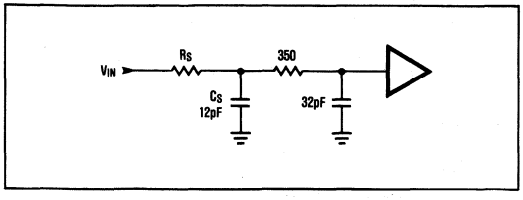


Figure 11b. RC Network Model.

During this acquisition phase ($\overline{WR}$ = Low in the WR-RD Mode) the input capacitors must be charged to the input voltage through the resistance of the internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 11. As R_S (source impedance) increases, the capacitors take longer to charge.

Typical input capacitances of 45pF allow source resistances of up to 1kΩ to be used without settling problems. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. Since the length of this acquisition time is internally set when in the RD mode, large source resistances (greater than 1kΩ) may cause settling errors. In this case, use the WR-RD mode and greater than 600ns $\overline{RD}$ time or use a buffer to drive the analog input.

Input Filtering

The transients in the analog input due to the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input while $\overline{WR}$ is low, and are latched once $\overline{WR}$ goes high. Therefore, at least 600ns will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the V_{IN} terminal.

Inherent Track-and-Hold

Due to its sampling behavior, the MAX150/AD7820 has the ability to measure a variety of high speed input signals without the help of an external sample-and-hold. In a conventional SAR type converter, the analog input must remain stable within 1/2 LSB for the duration of the conversion to maintain accuracy. This requires the use of external sample-and-holds whenever the input is a high speed signal. Although the conversion time for the MAX150/AD7820 is 1.34μs, the time for which the input must be stable is much less.

The MAX150/AD7820 tracks the input while $\overline{WR}$ is low (in the WR-RD mode) and finishes sampling it approximately 100ns after the rising edge of $\overline{WR}$. This aperture delay is caused by the internal logic propagation delay. Input signals with slew rates typically below 200mV/μs can be converted without error. However, faster signals may cause differential linearity errors due different delays through the MS and LS comparators. Still, the errors caused by fast input signals are far less than the errors caused in a conventional SAR type ADC without a sample-and-hold. A 1μs SAR converter would still not be able to measure a 1kHz, 5V sine wave without the aid of an external sample-and-hold. The MAX150/AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

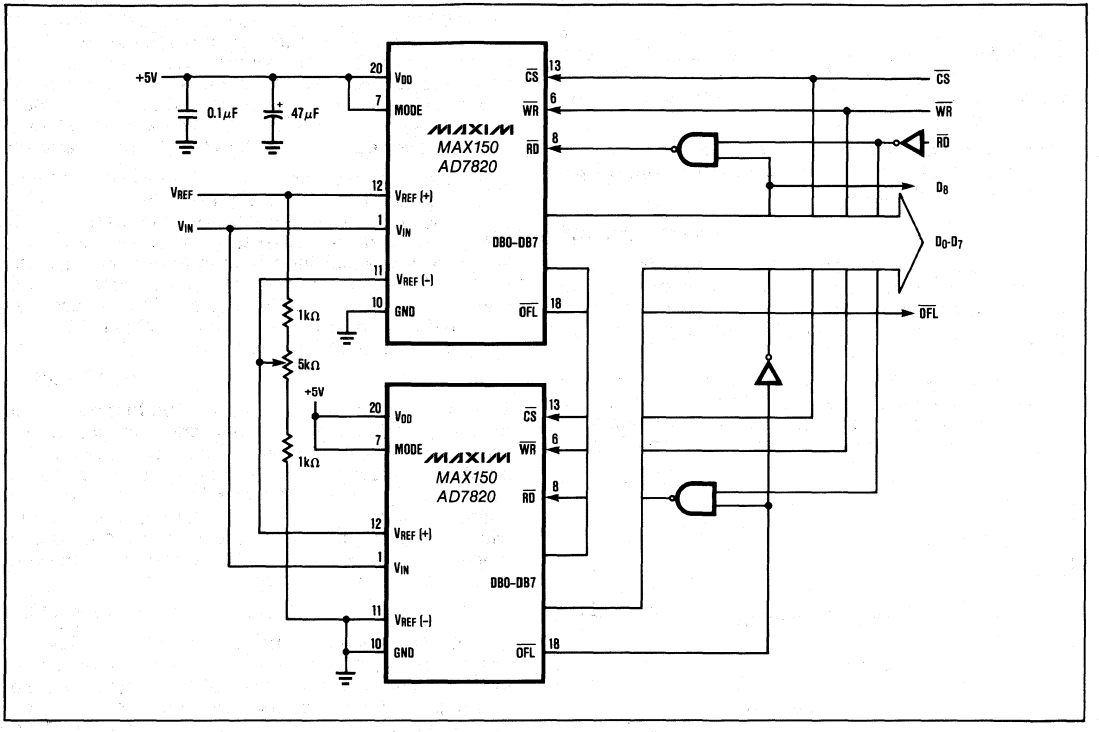


Figure 12. 9-Bit Resolution

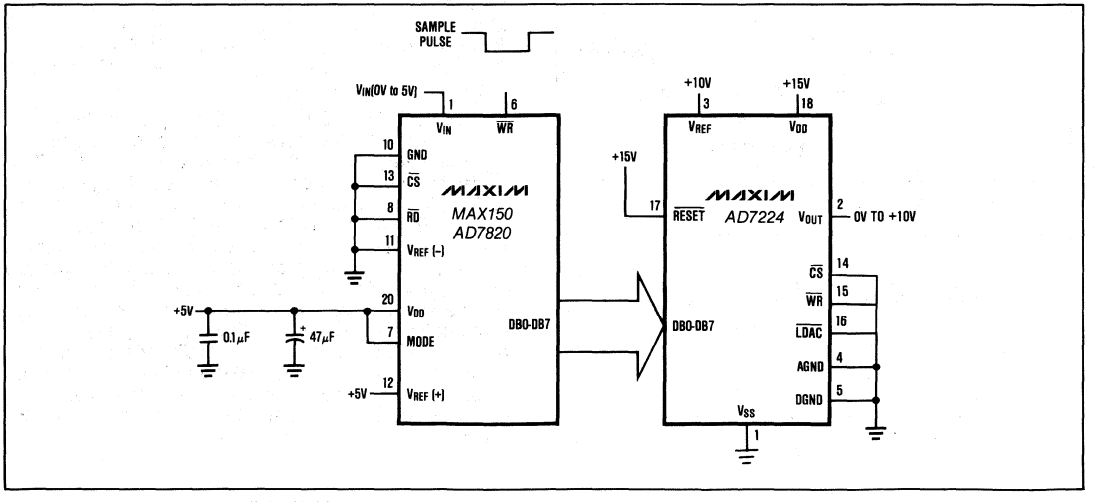


Figure 13. Fast Sample-and-Infinite Hold

CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

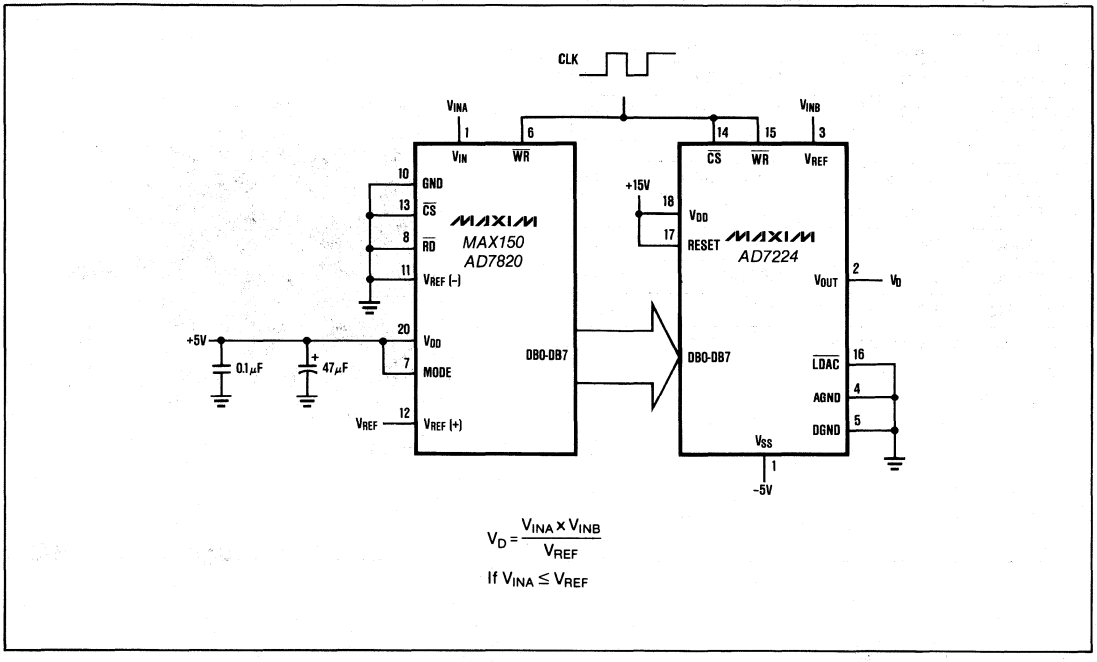


Figure 14. 8-Bit Analog Multiplier

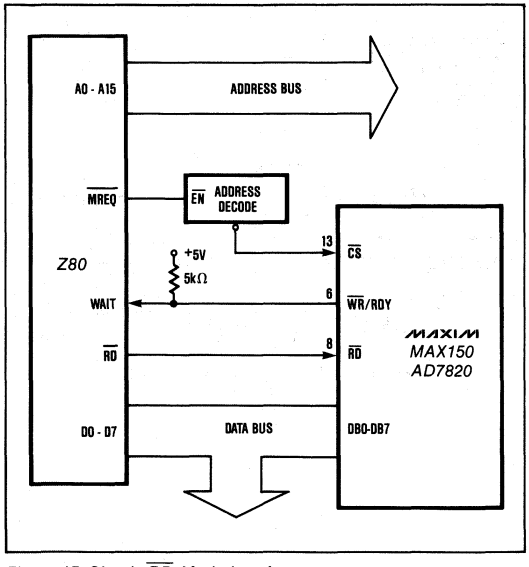


Figure 15. Simple $\overline{RD}$-Mode Interface

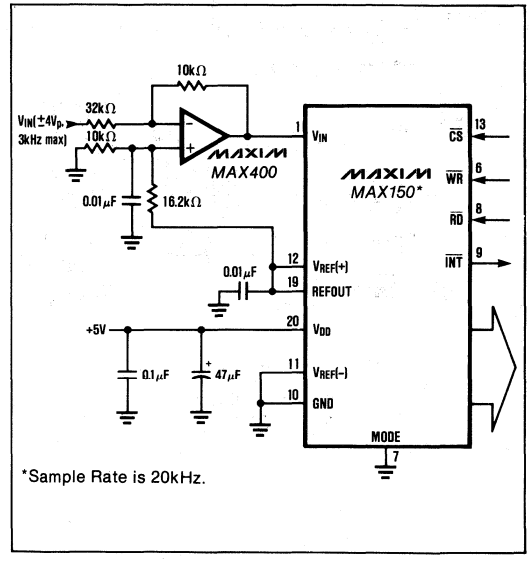


Figure 16. Telecom A/D Converter

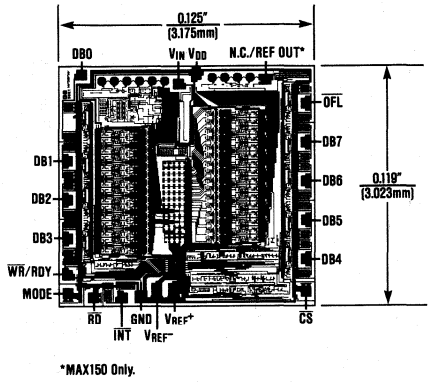
CMOS High Speed 8 Bit A/D Converter with Reference and Track/Hold Function

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
AD7820LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7820KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7820LCWP	0° C to +70° C	Small Outline	±½ LSB
AD7820KCWP	0° C to +70° C	Small Outline	±1 LSB
AD7820CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7820BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7820UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7820TQ	-55° C to +125° C	CERDIP	±1 LSB

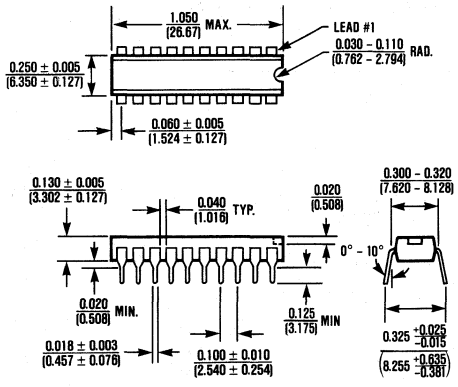
† *All devices — 20 lead packages*

Chip Topography

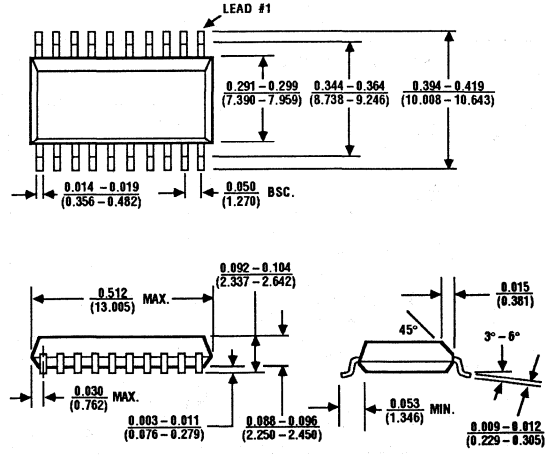


*MAX150 Only.

Package Information



20 Lead Plastic DIP (PP)
θ_{JA} = 125°C/W
θ_{JC} = 60°C/W



20 Lead Small Outline, Wide (WP)
θ_{JA} = 90°C/W
θ_{JC} = 50°C/W

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

General Description

The MAX154/MAX158 and AD7824/AD7828 are high speed multi-channel A/D converters. The MAX154 and AD7824 have 4 analog input channels while the MAX158 and AD7828 have 8 channels. Conversion time for all devices is 2.5μs. The MAX154/MAX158 also features a 2.5V on-chip reference, forming a complete high speed data acquisition system.

All converters include a built-in track-and-hold, eliminating the need for an external track-and-hold with many input signals. The analog input range is 0V to +5V although the A/D operates from a single +5V supply.

Microprocessor interface's are simplified by the ADC's ability to appear as a memory location or I/O port without the need for external logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port.

The AD7824 and AD7828 are pin compatible with Analog Devices' AD7824 and AD7828. The MAX154 and MAX158, which feature internal references, are also compatible with these products.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Control
Audio Instrumentation

Features

- ◆ **One-Chip Data Acquisition System**
- ◆ **4 or 8 Analog Input Channels**
- ◆ **2.5μs Per Channel Conversion Time**
- ◆ **Internal 2.5V Reference (MAX154/MAX158 only)**
- ◆ **Built in Track/Hold Function**
- ◆ **½ LSB Error Specification**
- ◆ **Single +5V Supply Operation**
- ◆ **No External Clock**

Ordering Information

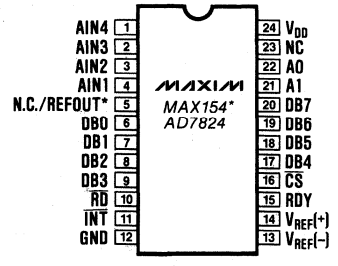
PART	TEMP RANGE	PACKAGE*	ERROR
MAX154ACNG	0° C to +70° C	Plastic DIP	±½ LSB
MAX154BCNG	0° C to +70° C	Plastic DIP	±1 LSB
MAX154BC/D	0° C to +70° C	Dice	±1 LSB
MAX154ACWG	0° C to +70° C	Small Outline	±½ LSB
MAX154BCWG	0° C to +70° C	Small Outline	±1 LSB
MAX154AENG	-40° C to +85° C	Plastic DIP	±½ LSB
MAX154BENG	-40° C to +85° C	Plastic DIP	±1 LSB
MAX154AEWG	-40° C to +85° C	Small Outline	±½ LSB
MAX154BEWG	-40° C to +85° C	Small Outline	±1 LSB
MAX154AMRG	-55° C to +125° C	CERDIP	±½ LSB
MAX154BMRG	-55° C to +125° C	CERDIP	±1 LSB

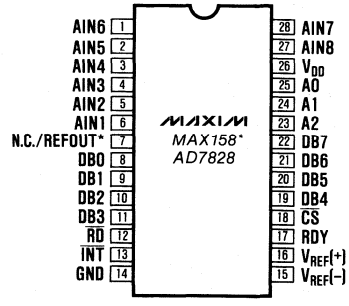
* *MAX154/AD7824 — 24 lead package, MAX158/AD7828 — 28 lead package*

Ordering Information continued on last page.

Pin Configurations

Top View





*REFOUT on MAX154/MAX158 only

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins ..... GND - 0.3V, V_{DD} +0.3V
Output current (REF_{OUT}) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +25°C by ..... 6mW/°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Operating Temperature Ranges
MAX154, MAX158
XCXX ..... 0°C to +70°C
XEXX ..... -40°C to +85°C
XMXX ..... -55°C to +125°C
AD7824, AD7828
KN/LN/KCWX/LCWX ..... 0°C to +70°C
BQ/CQ ..... -25°C to +85°C
TQ/UQ ..... -55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX15XA, AD782XL/C/U MAX15XB, AD782XK/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
Channel to Channel Mismatch					±1/4	LSB
REFERENCE INPUT						
Reference Resistance		T_A = T_{MIN} to T_{MAX}	1		4	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD}	V
V_{REF}^- Input Voltage Range			GND		V_{REF}^+	V
REFERENCE OUTPUT — MAX154/MAX158 ONLY (NOTE 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	**V**
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	**mV**
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	**mV**
Temperature Drift (Note 3)		**MAX15XXC T_A = 0°C to +70°C MAX15XXE T_A=-40°C to +85°C MAX15XXM T_A=-55°C to +125°C**		**40 40 60**	**70 70 100**	**ppm/°C**
Output Noise	**e_N**			**200**		**μV/rms**
Capacitive Load					**0.01**	**μF**
ANALOG INPUT						
Analog Input Voltage Range	A_{INR}		V_{REF}^-		V_{REF}^+	V
Analog Input Capacitance	C_{AIN}			45		pF
Analog Input Current	I_{AIN}	Any Channel, AIN = 0V to +5V			±3	μA
Slew Rate, Tracking (Note 4)	SR			0.7	0.157	V/μs
LOGIC INPUTS ($\overline{RD}$, $\overline{CS}$, A0, A1, A2)						
Input HIGH Voltage	V_{INH}		2.4			V
Input LOW Voltage	V_{INL}				0.8	V
Input High Current	I_{INH}				1	μA
Input Low Current	I_{INL}				-1	μA
Input Capacitance (Note 8)	C_{IN}			5	8	pF

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} -25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{INT}$; I_{OUT} = -360μA	4.0			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{INT}$; I_{OUT} = 1.6mA RDY; I_{OUT} = 2.6mA			0.4 0.4	V
Three-state Output Current		DB0-DB7, RDY; V_{OUT} = 0V to V_{DD}			±3	μA
Output Capacitance (Note 8)	C_{OUT}			5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ±5% for Specified Performance	+4.75		+5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = +2.4V			15	mA
Power Dissipation				25	75	mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS (Note 4, 5)

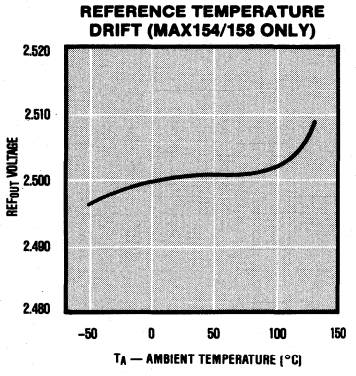
(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

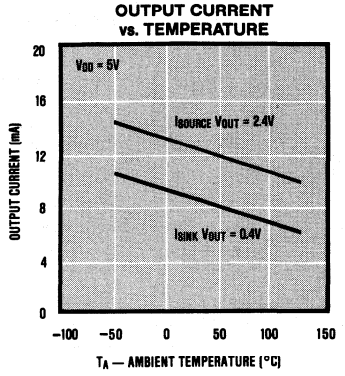
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX15XC/E AD782XK/L/B/C		MAX15XM AD782XT/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, Hold Time	t_{CSH}		0			0		0		ns
Multiplexer Address Setup Time	t_{AS}		0			0		0		ns
Multiplexer Address Hold Time	t_{AH}		30			35		40		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 5kΩ		30	40		60		60	ns
Conversion Time (Mode 0)	t_{CRD}			1.6	2.0		2.4		2.8	μs
Data Access Time After RD	t_{ACC1}	(Note 6)			85		110		120	ns
Data Access Time After INT, Mode 0	t_{ACC2}	(Note 6)		20	50		60		70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (Mode 1)	t_{INTH}	C_L = 50pF		40	75		100		100	ns
Data Hold Time	t_{DH}	(Note 7)			60		70		70	ns
Delay Time Between Conversions	t_P				500		500		600	ns
$\overline{RD}$ Pulse Width (Mode 1)	t_{RD}		60		600	80	500	80	400	ns

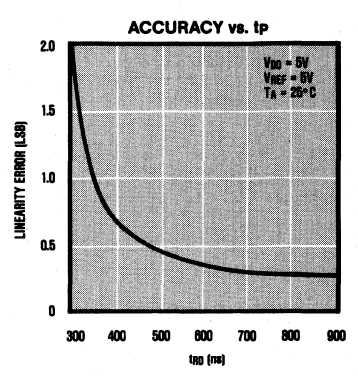
Note 5: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 6: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4 V.
Note 7: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Note 8: Guaranteed by design.

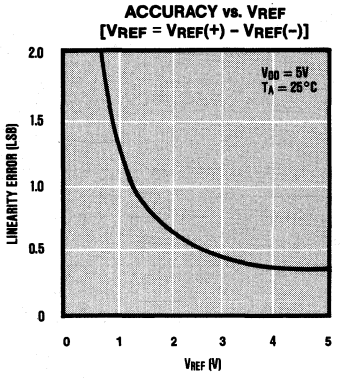
CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

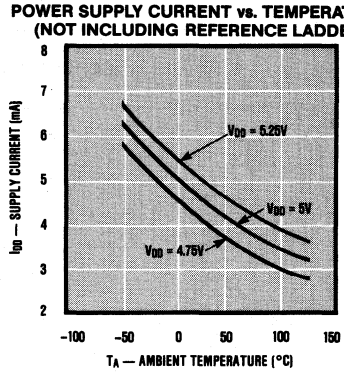
Typical Operating Characteristics











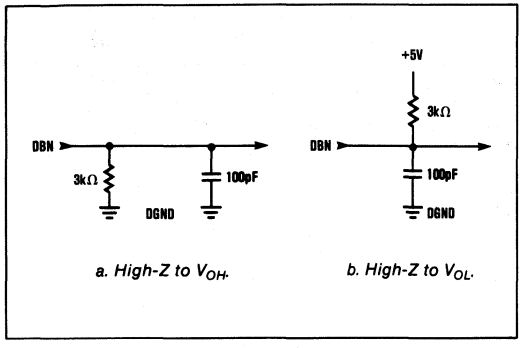


Figure 1. Load Circuits for Data Access Time Test

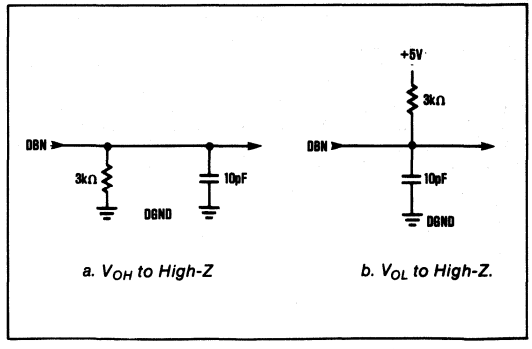


Figure 2. Load Circuits for Data Hold Time Test

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

MAX154/AD7824 Pin Description

PIN	NAME	FUNCTION
1	AIN4	Analog input channel 4
2	AIN3	Analog input channel 3
3	AIN2	Analog input channel 2
4	AIN1	Analog input channel 1
5	REFOUT N.C.	Reference output (2.5V) for MAX154 No Connect for AD7824
6	DB0	Three-state data output, bit 0 (LSB)
7	DB1	Three-state data output, bit 1
8	DB2	Three-state data output, bit 2
9	DB3	Three-state data output, bit 3
10	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
11	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
12	GND	Ground
13	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
14	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
15	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
16	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
17	DB4	Three-state data output, bit 4
18	DB5	Three-state data output, bit 5
19	DB6	Three-state data output, bit 6
20	DB7	Three-state data output, bit 7 (MSB)
21	A1	Channel Address 1 Input
22	A0	Channel Address 0 Input
23	NC	No Connect
24	V_{DD}	Power supply voltage, +5V

MAX158/AD7828 Pin Description

PIN	NAME	FUNCTION
1	AIN6	Analog input channel 6
2	AIN5	Analog input channel 5
3	AIN4	Analog input channel 4
4	AIN3	Analog input channel 3
5	AIN2	Analog input channel 2
6	AIN1	Analog input channel 1
7	REFOUT N.C.	Reference output (2.5V) for MAX158 No Connect for AD7828
8	DB0	Three-state data output, bit 0 (LSB)
9	DB1	Three-state data output, bit 1
10	DB2	Three-state data output, bit 2
11	DB3	Three-state data output, bit 3
12	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
13	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
14	GND	Ground
15	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
16	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
17	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
18	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
19	DB4	Three-state data output, bit 4
20	DB5	Three-state data output, bit 5
21	DB6	Three-state data output, bit 6
22	DB7	Three-state data output, bit 7 (MSB)
23	A2	Channel Address 2 Input
24	A1	Channel Address 1 Input
25	A0	Channel Address 0 Input
26	V_{DD}	Power supply voltage, +5V
27	AIN8	Analog input channel 8
28	AIN7	Analog input channel 7

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Detailed Description

Converter Operation

The MAX154/MAX158/AD7824/AD7828 uses what is commonly called a "half-flash" conversion technique (see Figure 3). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper four bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate an analog signal from the first flash conversion. A residue voltage representing the difference between the unknown input and the DAC voltage is then compared to the reference ladder by 15 LS (least significant) flash comparators to obtain the lower four output bits.

Operating Sequence

The operating sequence is shown in Figure 4. A conversion is initiated by a falling edge of RD and CS. The comparator inputs track the analog input voltage for approximately 1μs. After this first cycle the MS flash result is latched into the output buffers and the LS conversion begins. INT goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 bits are latched into the output buffers. The data can then be accessed using the CS and RD inputs.

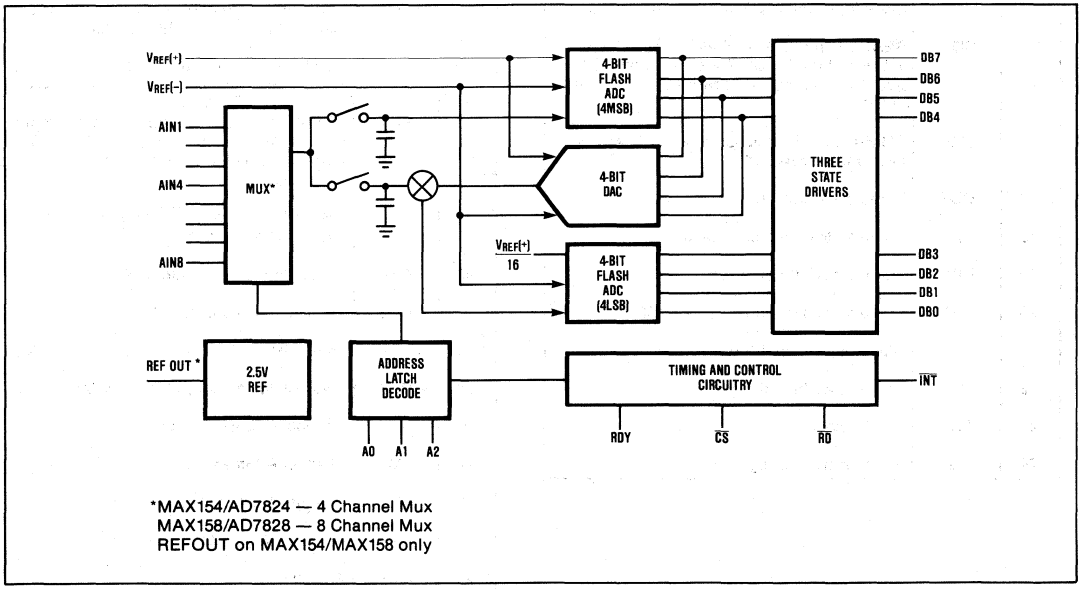
Digital Interface

The MAX154/MAX158 and AD7824/AD7828 use only Chip Select (CS) and Read (RD) as control inputs. A READ operation, taking CS and RD low, latches the multiplexer address inputs and starts a conversion (See Table 1).

Table 1.
Truth Table For Input Channel Selection

MAX154/AD7824		MAX158/AD7828			SELECTED
A1	A0	A2	A1	A0	CHANNEL
0	0	0	0	0	AIN1
0	1	0	0	1	AIN2
1	0	0	1	0	AIN3
1	1	0	1	1	AIN4
		1	0	0	AIN5
		1	0	1	AIN6
		1	1	0	AIN7
		1	1	1	AIN8

There are two interface modes which are determined by the length of the RD input. Mode 0, implemented by keeping RD low until the conversion ends, is designed for microprocessors that can be forced into a WAIT state. In this mode, a conversion is started with a READ operation (taking CS and RD low) and data is read when the conversion ends. Mode 1 on the other hand does not require microprocessor WAIT states. A READ operation simultaneously initiates a conversion and reads the previous conversion result.



*MAX154/AD7824 — 4 Channel Mux
MAX158/AD7828 — 8 Channel Mux
REFOUT on MAX154/MAX158 only

Figure 3. Functional Diagram

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

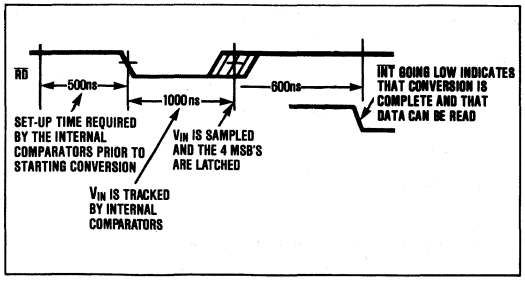


Figure 4. Operating Sequence

Interface Mode 0

Figure 5 shows the timing diagram for Mode 0 operation. This is used with microprocessors that have WAIT state capability, whereby a READ instruction is extended to accomodate slow memory devices. Taking $\overline{CS}$ and $\overline{RD}$ low latches the analog multiplexer address and starts a conversion. Data outputs DB0-DB7 remain in the high impedance condition until the conversion is complete.

There are two status outputs, Interrupt ($\overline{INT}$) and Ready (RDY). RDY, an open drain output (no internal pull-up device), is connected to the processor's READY/WAIT input. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion, when the conversion result appears on the data outputs. If the RDY output is not required, its external pull-up resistor can be omitted. $\overline{INT}$ goes low when the conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Interface Mode 1

Mode 1 is designed for applications where the microprocessor is not forced into a WAIT state. Taking $\overline{CS}$ and $\overline{RD}$ low latches the multiplexer address and starts a conversion (See Figure 6). Data from the previous conversion is immediately read from the outputs (DB0-DB7).

$\overline{INT}$ goes high at the rising edge of $\overline{CS}$ or $\overline{RD}$ and goes low at the end of the conversion. A second READ operation is required to read the result of this conversion. The second READ latches a new multiplexer address and starts another conversion. A delay of 2.5μs must be allowed between READ operations. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the rising edge of $\overline{CS}$. If RDY is not needed, its external pull-up resistor can be omitted.

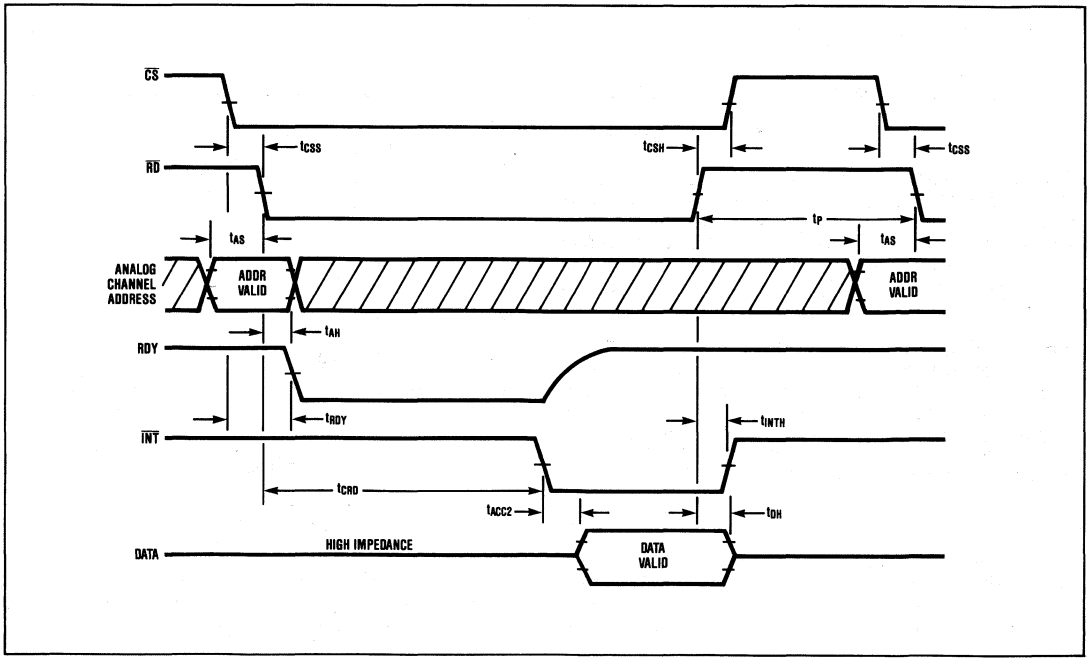


Figure 5. Mode 0 Timing Diagram

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

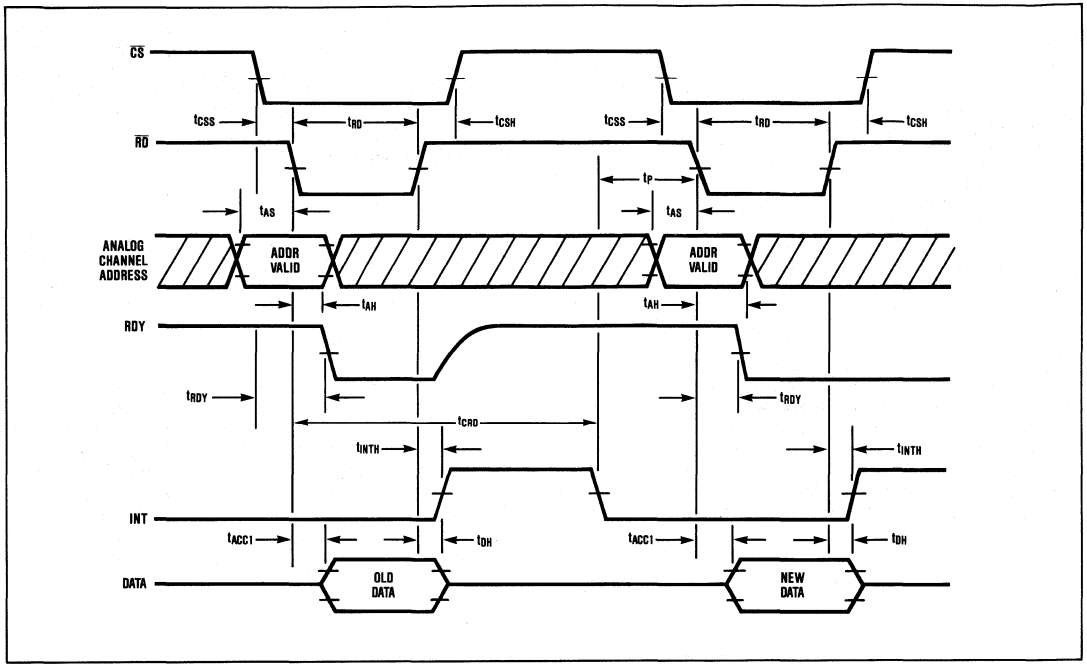


Figure 6. Mode 1 Timing Diagram

Analog Considerations

Reference and Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter define the zero and the full-scale of the ADC. In other words, the voltage at $V_{REF}(-)$ is equal to the input voltage which produces an output code of all zeroes and the voltage at $V_{REF}(+)$ is equal to input voltage which produces an output code of all ones (see Figure 7).

Figure 8 shows some possible reference configurations. For the MAX154/MAX158, a 0.01μF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer. The 2.5V reference output is with respect to the GND pin.

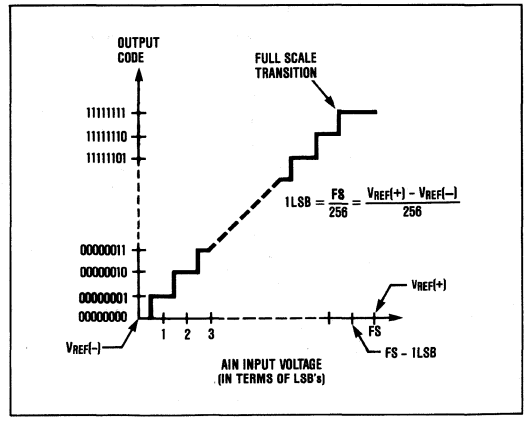


Figure 7. Transfer Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors must have minimum lead length since excess lead length may contribute to conversion errors and instability. If the reference inputs are driven by long lines, they should be bypassed to GND with 0.1μF capacitors at the reference input pins.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

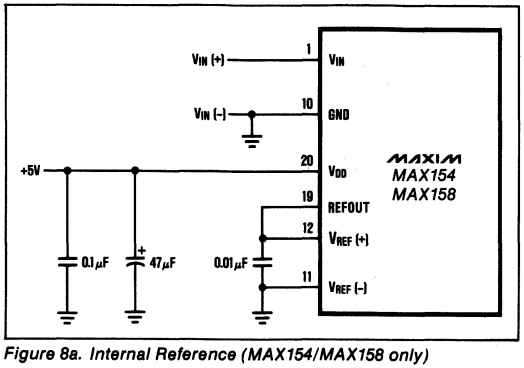


Figure 8a. Internal Reference (MAX154/MAX158 only)

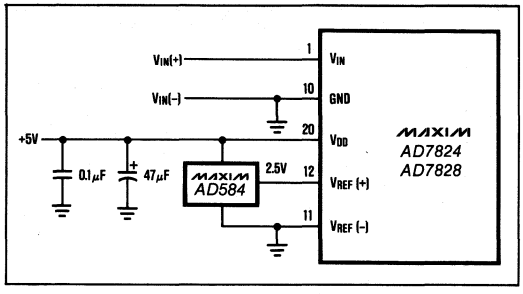


Figure 8b. External Reference +2.5V Full-Scale

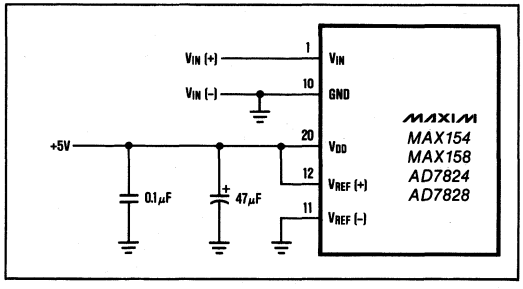


Figure 8c. Power Supply as Reference

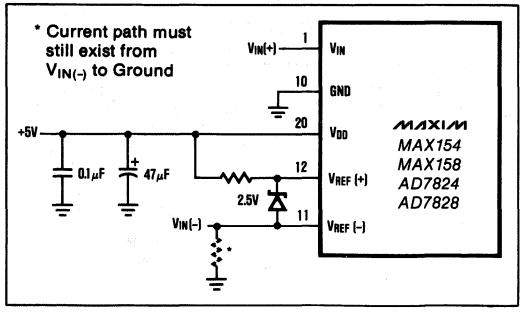


Figure 8d. Inputs Not Referenced to GND

Input Current

The converters' analog inputs behave somewhat differently from conventional ADCs. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in. The equivalent circuit of the converter is shown in Figure 9a. When the conversion starts AIN(n) is connected to the MS and LS comparators. Thus, AIN(n) is connected to thirty-one 1pF capacitors.

To acquire the input signal in approximately 1µs, the input capacitors must charge to the input voltage through the on resistance of the multiplexer (about 600Ω) and the comparator's analog switches (2kΩ to 5kΩ per comparator). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 9b. As R_S (source impedance) increases, the capacitors take longer to charge.

Since the length of the input acquisition time is internally set, large source resistances (greater than 100Ω) will cause settling errors. The output impedance of an op-amp is its open loop output impedance divided by the loop gain at the frequency of interest. It is important that the amplifier driving the converter input have sufficient loop gain at approximately 1MHz to maintain low output impedance.

Input Filtering

The transients in the analog input caused by the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input during the first 1µs of the conversion, and are then latched. Therefore, at least 1µs will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the AIN terminals.

Sinusoidal Inputs

The MAX154/MAX158 and AD7824/AD7828 can measure input signals with slew rates as high as 157mV/µs to the rated specifications. This means that the analog input frequency can be as high as 10kHz without the aid of an external track-and-hold. The maximum sampling rate is limited by the conversion time (typical t_{CRD} = 2µs) plus the time required between conversions (t_P = 500ns). It is calculated as:

$$f_{MAX} = \frac{1}{t_{CRD} + t_P} = \frac{1}{(2.0 + 0.5)\ \mu s} = 400kHz$$

f_{MAX} permits a maximum sampling rate of 50kHz per channel when using the MAX158/AD7828 and 100kHz per channel when using the MAX154/AD7824. These rates are well above the Nyquist requirement of 20kHz sampling rate for a 10kHz input bandwidth.

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Bipolar Input Operation

The circuit in Figure 10a. can be used for bipolar input operation. The input voltage is scaled by an amplifier so that only positive voltages appear at the ADC's inputs. An external reference should be used for the AD7824/AD7828 but is not needed with the MAX154/MAX158. The analog input range is ±4V and the output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 10b.

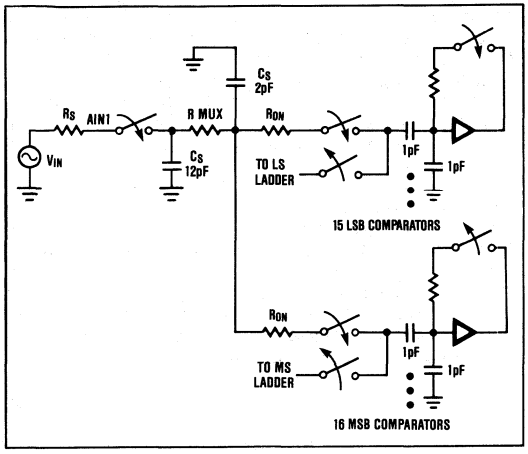


Figure 9a. Equivalent Input Circuit

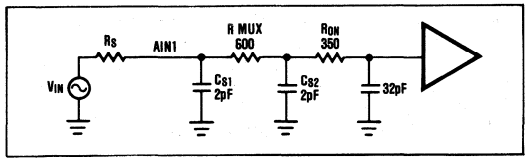


Figure 9b. RC Network Model

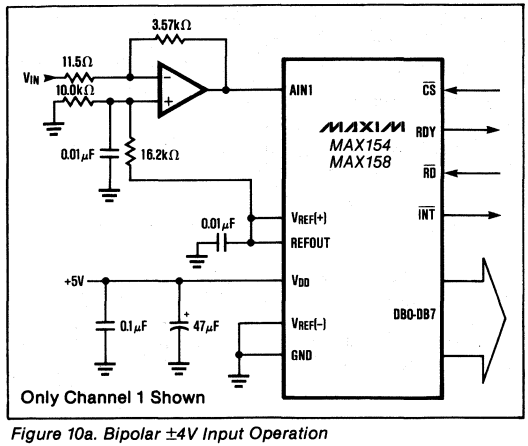


Figure 10a. Bipolar ±4V Input Operation

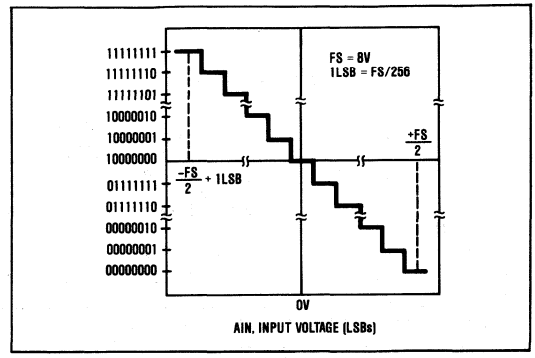


Figure 10b. Transfer Function for ±4V Input Operation

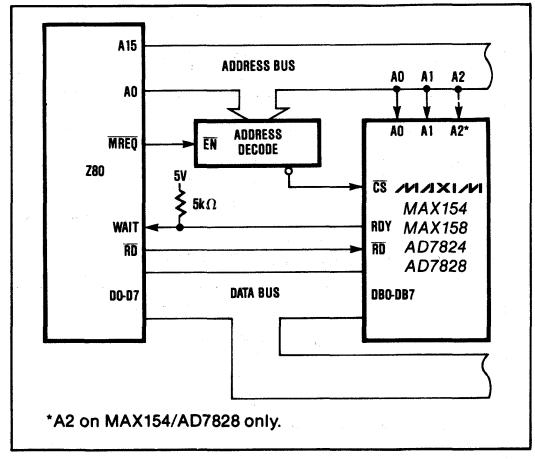


Figure 11. Simple Mode 0 Interface

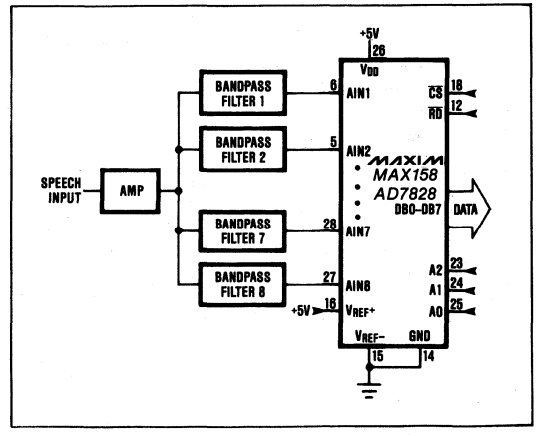


Figure 12. Speech Analysis Using Real Time Filtering

MAXIM

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

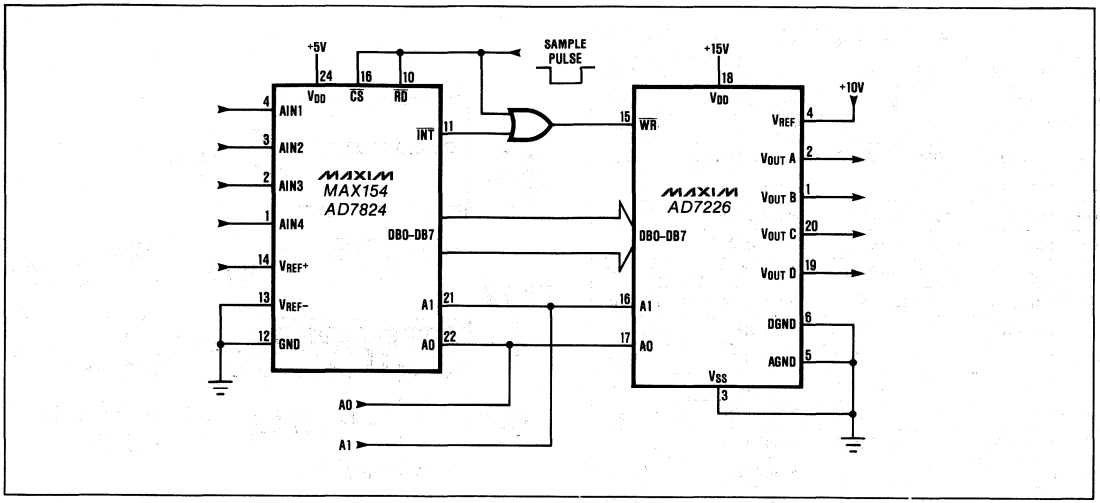
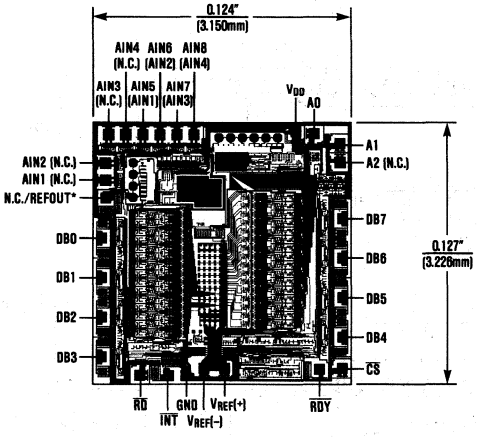


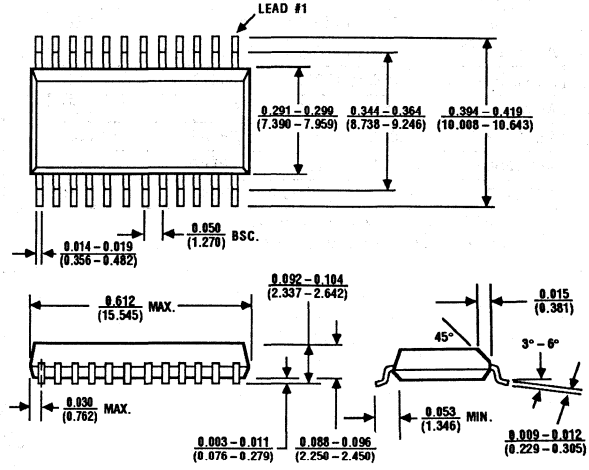
Figure 13. 4-Channel Fast Sample and Infinite Hold

Chip Topography



Note: Connections in parentheses ( ) are for MAX154/AD7824
* REFOUT on MAX154/MAX158 only

Package Information



24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W

θ_{JC} = 45° C/W

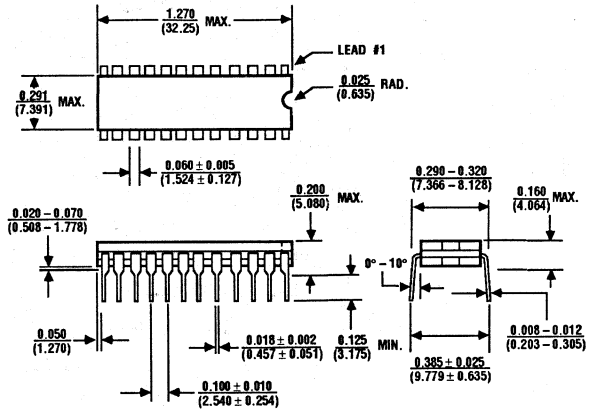
CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Ordering Information (continued)

PART	TEMP RANGE	PACKAGE*	ERROR
MAX158ACPI	0° C to +70° C	Plastic DIP	±½ LSB
MAX158BCPI	0° C to +70° C	Plastic DIP	±1 LSB
MAX158BC/D	0° C to +70° C	Dice	±1 LSB
MAX158ACWI	0° C to +70° C	Small Outline	±½ LSB
MAX158BCWI	0° C to +70° C	Small Outline	±1 LSB
MAX158AEPI	-40° C to +85° C	Plastic DIP	±½ LSB
MAX158BEPI	-40° C to +85° C	Plastic DIP	±1 LSB
MAX158AEWI	-40° C to +85° C	Small Outline	±½ LSB
MAX158BEWI	-40° C to +85° C	Small Outline	±1 LSB
MAX158AMDI	-55° C to +125° C	CERDIP	±½ LSB
MAX158BMDI	-55° C to +125° C	CERDIP	±1 LSB
AD7824LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7824KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7824LCWG	0° C to +70° C	Small Outline	±1 LSB
AD7824KCWG	0° C to +70° C	Small Outline	±½ LSB
AD7824CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7824BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7824UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7824TQ	-55° C to +125° C	CERDIP	±1 LSB
AD7828LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7828KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7828LCWI	0° C to +70° C	Small Outline	±1 LSB
AD7828KCWI	0° C to +70° C	Small Outline	±½ LSB
AD7828CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7828BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7828UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7828TQ	-55° C to +125° C	CERDIP	±1 LSB

* *MAX154/AD7824 — 24 lead package, MAX158/AD7828 — 28 lead package*

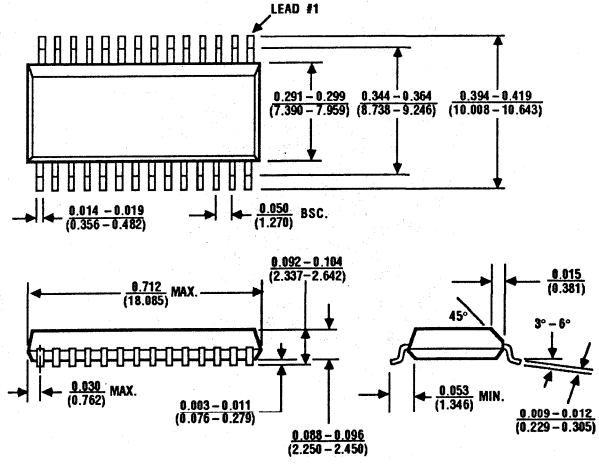
Package Information



24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W



28 Lead Small Outline, Wide (WI)

θ_{JA} = 80°C/W

θ_{JC} = 45°C/W

μP Compatible 8 Bit A/D Converter

General Description

The MAX160 and AD7574 are low cost, microprocessor compatible 8 bit analog-to-digital converters which use the successive-approximation technique to achieve conversion times of 4μs (MAX160) and 15μs (AD7574).

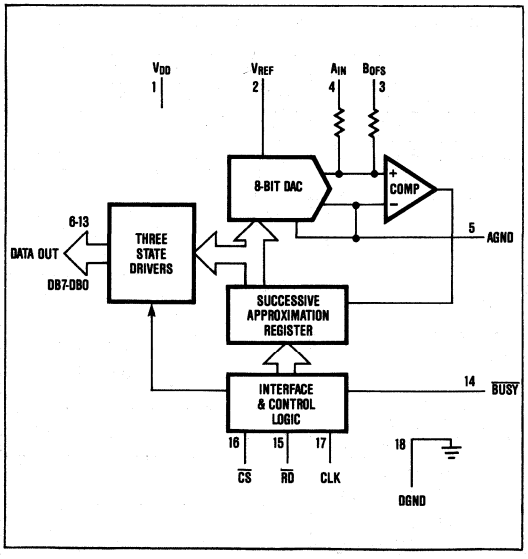
The A/Ds are designed to easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port. Operation is simplified by an on-chip clock, +5V power supply requirement, and low supply current (5mA max).

The MAX160 provides major performance improvements over the AD7574 in accuracy and speed specifications as well as compatibility with TTL logic levels.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
Process Automation
Instrumentation
Avionics

Functional Diagram



Features

- **Improved Second Source (MAX160)**
- **Fast Conversion Time: 4μs (MAX160) 15μs (AD7574)**
- **No Missing Codes Over Temperature**
- **Single +5V Supply**
- **Ratiometric Operation**
- **No External Clock Necessary**
- **Easy Interface To Microprocessors**

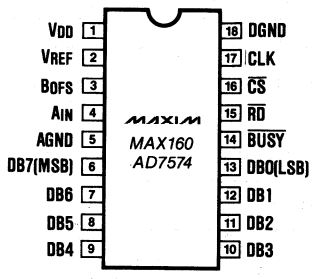
Ordering Information

PART	TEMP. RANGE	PACKAGE†	ERROR
MAX160CPN	0°C to +70°C	Plastic DIP	±½ LSB
MAX160CC/D	0°C to +70°C	Dice*	±½ LSB
MAX160CWN	0°C to +70°C	Small Outline	±½ LSB
MAX160EPN	-40°C to +85°C	Plastic DIP	±½ LSB
MAX160EWN	-40°C to +85°C	Small Outline	±½ LSB
MAX160MJN	-55°C to +125°C	CERDIP**	±½ LSB
AD7574KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7574JN	0°C to +70°C	Plastic DIP	±¾ LSB
AD7574KCWN	0°C to +70°C	Small Outline	±½ LSB
AD7574JCWN	0°C to +70°C	Small Outline	±¾ LSB

† *All devices — 18 lead packages*
* *Consult factory for dice specifications.*
** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP packages.*
Ordering Information continued on last page

Pin Configuration

Top View



μP Compatible 8 Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS — MAX160, AD7574

Supply Voltage, V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... -0.3V, V_{DD}
Digital Inputs/Outputs (Pins 6-17) .... DGND - 0.3V, V_{DD}+ 0.3V
Analog Inputs (Pins 2-4) ..... -20V, +20V
Power Dissipation (Any Package) to +70°C 670mW
Derate Above +70°C by ..... 8.3mW/°C

Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Ranges
MAX160CPN, AD7574JN/KN/JCWN/KCWN ... 0°C to +70°C
AD7574AD/BD/AQ/BQ ..... -25°C to +85°C
MAX160EPN ..... -40°C to +85°C
MAX160MDN/MJN ..... -55°C to +125°C
AD7574SD/TD/SQ/TQ ..... -55°C to +125°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS — MAX160, AD7574

(V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, Slow Memory Mode using External Clock f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for AD7574 (Fig. 9), T_A = T_{MIN} to T_{MAX}, unless specified otherwise.)

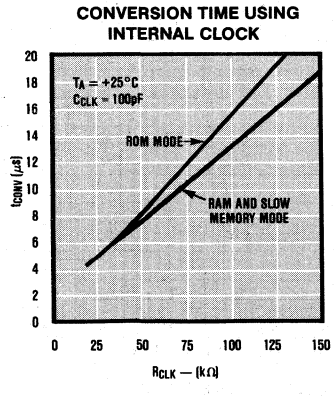
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY (f_{CLK} = 2.0MHz for MAX160 and 0.5MHz for AD7574)						
Resolution			8			bits
Relative Accuracy Error		MAX160, AD7574K/B/T			±½	LSB
		AD7574J/A/S			±¾	
Differential Non-Linearity		MAX160, AD7574K/B/T			±¾	LSB
		AD7574J/A/S			±⅞	
Full Scale Error (Note 1) (Gain Error)		MAX160, AD7574K/B/T; T_A = +25°C			±3	LSB
		MAX160, AD7574K/B/T; T_A = T_{MIN} to T_{MAX}			±4.5	
		AD7574J/A/S; T_A = +25°C			±5	
		AD7574J/A/S; T_A = T_{MIN} to T_{MAX}			±6.5	
Offset Error (Note 2)		**MAX160; T_A = +25°C**			**±20**	mV
		MAX160; T_A = T_{MIN} to T_{MAX}			**±30**	
		AD7574K/B/T; T_A = +25°C			±30	
		AD7574K/B/T; T_A = T_{MIN} to T_{MAX}			±50	
		AD7574J/A/S; T_A = +25°C			±60	
		AD7574J/A/S; T_A = T_{MIN} to T_{MAX}			±80	
Mismatch Between B_{OFS} and A_{IN} Resistances (Note 3)					±1.5	%
ANALOG INPUTS						
V_{REF} Input Resistance			5	10	15	kΩ
A_{IN} Input Resistance			10	20	30	kΩ
B_{OFS} Input Resistance			10	20	30	kΩ
Reference Voltage	V_{REF}	±5% for specified transfer accuracy		-10		V
Reference Voltage Range (Note 4)			-5		-15	V
Nominal Analog Input Range		Unipolar Mode	0		$\|V_{REF}\|$	V
		Bipolar Mode	$-\|V_{REF}\|$		$+\|V_{REF}\|$	
LOGIC INPUTS						
Logic Input High Voltage	V_{INH}	MAX160; $\overline{RD}$, $\overline{CS}$	2.4			V
		AD7574; $\overline{RD}$, $\overline{CS}$	3.0			
		MAX160, AD7574; CLK	3.0			
Logic Input Low Voltage	V_{INL}	MAX160, AD7574; $\overline{RD}$, $\overline{CS}$			0.8	V
		MAX160; CLK			0.8	
		AD7574; CLK			0.4	
Logic Input Current	I_{IN}	$\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = +25°C			1	μA
		$\overline{RD}$, $\overline{CS}$, V_{IN} = 0, V_{DD}; T_A = T_{MIN} to T_{MAX}			10	
Clock Input High Current		V_{IN} = V_{DD}; T_A = +25°C			2	mA
		V_{IN} = V_{DD}; T_A = T_{MIN} to T_{MAX}			3	
Clock Input Low Current		V_{IN} = 0V; T_A = +25°C			1	μA
		V_{IN} = 0V; T_A = T_{MIN} to T_{MAX}			10	
Input Capacitance (Note 5)	C_{IN}	$\overline{RD}$, $\overline{CS}$		5	7	pF

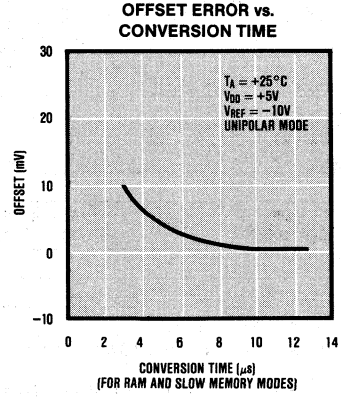
ELECTRICAL CHARACTERISTICS — MAX160, AD7574 (continued)

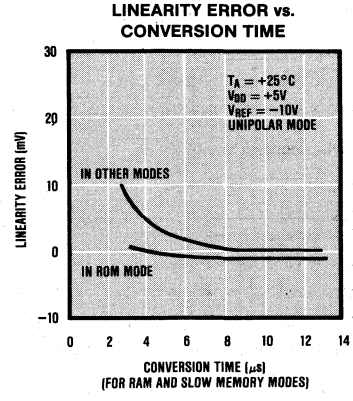
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS							
Logic Output High Voltage	V_{OH}	$\overline{BUSY}$, DB0-DB7 I_{SRC} = 200μA		4.0			V
Logic Output Low Voltage	V_{OL}	$\overline{BUSY}$, DB0-DB7, I_{SINK} = 1.6mA	T_A = +25°C			0.4	V
			T_A = T_{MIN} to T_{MAX} MAX160 AD7574			 0.4 0.8	
Floating State Leakage	I_{LKG}	DB0-DB7, V_{OUT} = 0, V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}			1 10	μA
Floating State Capacitance (Note 5)		DB0-DB7			5	7	pF
POWER REQUIREMENTS							
Power Supply Requirement	V_{DD}	+5V ±5% for specified performance		4.75		5.25	V
Power Supply Current	I_{DD}	A_{IN} = 0V, ADC in reset condition			1	5	mA
Reference Current	I_{REF}	Conversion complete, before reset				$V_{REF}/5$	V/kΩ

Note 1: Full scale error is measured after correcting for offset error. Max full-scale change from +25°C to T_{MIN} or T_{MAX} is ±1LSB.
Note 2: Maximum offset change from +25°C to T_{MIN} or T_{MAX} is ±10mV. Typical offset temperature coefficient is 50μV/°C.
Note 3: R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and gain term when using the circuit of Figure 9b.
Note 4: Typical value, not guaranteed or subject to test.
Note 5: Guaranteed but not tested.

Typical Operating Characteristics







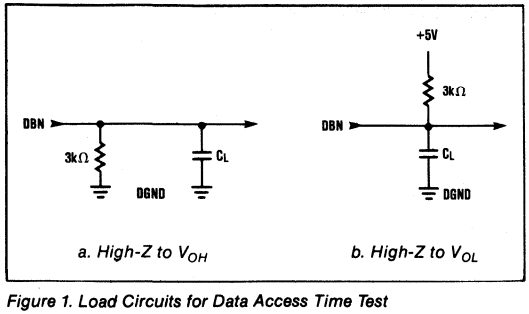


Figure 1. Load Circuits for Data Access Time Test

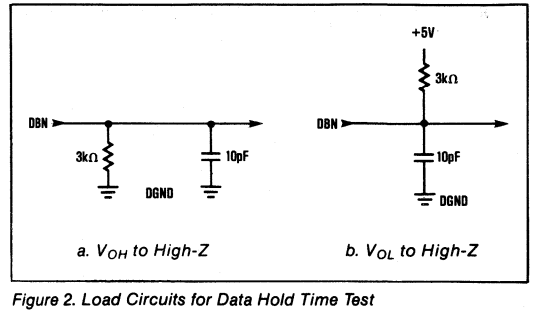


Figure 2. Load Circuits for Data Hold Time Test

TIMING CHARACTERISTICS (Note 1, 2) — MAX160

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 22kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		230		500	ns
Reset Time Requirement	t_{RESET}		1.5			1.5		1.5		μs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
Internal Clock Temperature Drift				250						ppm/°C
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		μs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		800	1200		1200		1200	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		50 60	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		0 0	90 100		90 100		120 140	ns
Data Hold Time (Note 4)	t_{RHD}			80	120		120		180	ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		60 70	100 110		100 110		130 150	ns
Reset Time Requirement			1.5			1.5		1.5		μs
Conversion Time Using Int CLK	t_{CONV}	R_{CLK} = 22kΩ	4	5	6	4	6	4	6	μs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 2.0MHz	4			4		4		μs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

TIMING CHARACTERISTICS (Note 1, 2) — AD7574

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN}		T_A = T_{MAX}		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
STATIC RAM INTERFACE MODE (See Figure 5 and Table 5)										
$\overline{CS}$ Pulse Width Requirement	t_{CS}		100			150		150		ns
$\overline{RD}$ to $\overline{CS}$ Setup Time	t_{WSCS}		0			0		0		ns
$\overline{CS}$ to $\overline{BUSY}$ Propogation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		50 70	120 150		120 150		180 200	ns
$\overline{BUSY}$ to $\overline{RD}$ Setup Time	t_{BSR}		0			0		0		ns
$\overline{BUSY}$ to $\overline{CS}$ Setup Time	t_{BSCS}		0			0		0		ns
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{RHCS}				250		200		500	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int CLK	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext CLK	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs
ROM INTERFACE MODE (See Figure 6 and Table 6)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{RD}$ HIGH to $\overline{BUSY}$ Delay (Note 2)	t_{WBPD}	C_L = 20pF		700	1500		1000		2000	ns
$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	t_{BSR}	(Note 5)								
Conversion Time Using Int CLK	t_{CONV}	See Graph		25						μs
SLOW MEMORY INTERFACE MODE (See Figure 7 and Table 7)										
Data Access Time (Note 3)	t_{RAD}	C_L = 20pF C_L = 100pF		40 60	150 300		150 300		220 400	ns
Data Hold Time (Note 4)	t_{RHD}	AD7574S/T AD7574J/K/A/B	50 50	80 80	120 120	30 30	80 120	80 50	180 180	ns ns
$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay (Note 2)	t_{CBPD}	C_L = 20pF C_L = 100pF		40 60	120 150		120 150		180 200	ns
Reset Time Requirement			3			3		3		μs
Conversion Time Using Int Clk	t_{CONV}	See Graph		23						μs
Conversion Time Using Ext Clk	t_{CONV}	f_{CLK} = 500kHz	15			15		15		μs

Note 1: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
Note 2: Busy output crosses 0.8V or 2.4V.
Note 3: Outputs are loaded with circuits in Figure 1 and defined as the time required for an output to cross 0.8 or 2.4V.
Note 4: Outputs are loaded with circuits in Figure 2 and defined as the time required for an output to change 0.5V.
Note 5: $\overline{RD}$ can go low prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table 6.

μP Compatible 8 Bit A/D Converter

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power supply voltage, +5V.
2	V_{REF}	Reference Input, nominal -10V.
3	B_{OFS}	Bipolar Offset Input, +10V for bipolar mode, connect to A_{IN} for unipolar mode.
4	A_{IN}	Analog input, 0 to +10V for unipolar mode, -10V to +10V for bipolar mode.
5	AGND	Analog Ground.
6	DB7	Three-state data output, bit 7 (MSB).
7	DB6	Three-state data output, bit 6.
8	DB5	Three-state data output, bit 5.
9	DB4	Three-state data output, bit 4.
10	DB3	Three-state data output, bit 3.

PIN	NAME	FUNCTION
11	DB2	Three-state data output, bit 2.
12	DB1	Three-state data output, bit 1.
13	DB0	Three-state data output, bit 0 (LSB).
14	$\overline{BUSY}$	BUSY output, $\overline{BUSY}$ goes low at the start of a conversion and returns high when the conversion is complete.
15	$\overline{RD}$	READ input, $\overline{RD}$ must be low to access data. See Digital Interface section.
16	$\overline{CS}$	CHIP-SELECT input. Used for conversion control or device addressing. See Digital Interface section.
17	CLK	External clock input/Internal clock frequency set input.
18	DGND	Digital Ground.

Detailed Description

Converter Operation

The MAX160/AD7574 uses the successive approximation technique to convert an unknown analog input to an 8 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only passive clock components, a -10V reference, and a +5V power supply.

Figure 3 shows the MAX160/AD7574 functional diagram. When a start command is received from $\overline{CS}$ or $\overline{RD}$ (see Digital Interface Section), BUSY goes low indicating that the conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of the bit causes the DAC output to be larger or smaller than the analog input, A_{IN}. If the DAC output is greater than A_{IN}, the trial bit is turned OFF, otherwise it is kept ON. Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made.

When all bits have been tried, $\overline{BUSY}$ goes high, indicating that the conversion is complete and the successive approximation register contains a valid representation of the analog input. The data can then be read using the $\overline{RD}$ input (see Digital Interface Section).

DAC Circuit Details

A thin film R-2R resistor network provides binarily weighted currents for each bit in the internal multiplying DAC (see Figure 4). N-channel MOS switches are used to steer current to either the summing junction or AGND depending on the DAC digital code. The A_{IN} and B_{OFS} input resistors also use series MOS switches (always ON) that match the DAC switches to maintain gain temperature tracking.

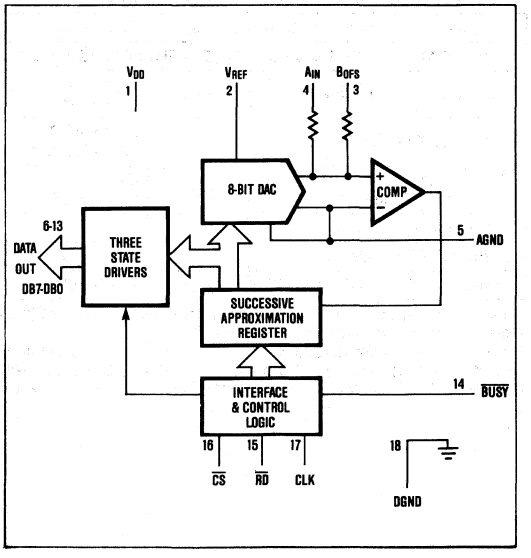


Figure 3. MAX160/AD7574 Functional Diagram

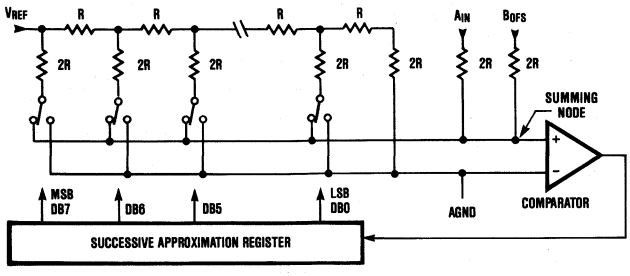


Figure 4. D/A Converter Used in the MAX160/AD7574

Table 5. Truth Table, Static Ram Mode

INPUTS		OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7–DB0	
L	H	H	HI-Z	Write Cycle (Start Convert)
L	↓	H	HI-Z to DATA	Read Cycle (Data Read)
L	↑	H	DATA to HI-Z	Reset Converter
H	X (Note 1)	X	HI-Z	Not Selected
L	H	L	HI-Z	No Effect (Converter Busy)
L	↓	L	HI-Z	No Effect (Converter Busy)
L	↑	L	HI-Z	Not Allowed, Conversion Error

Note 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the state of $\overline{CS}$ or $\overline{BUSY}$.

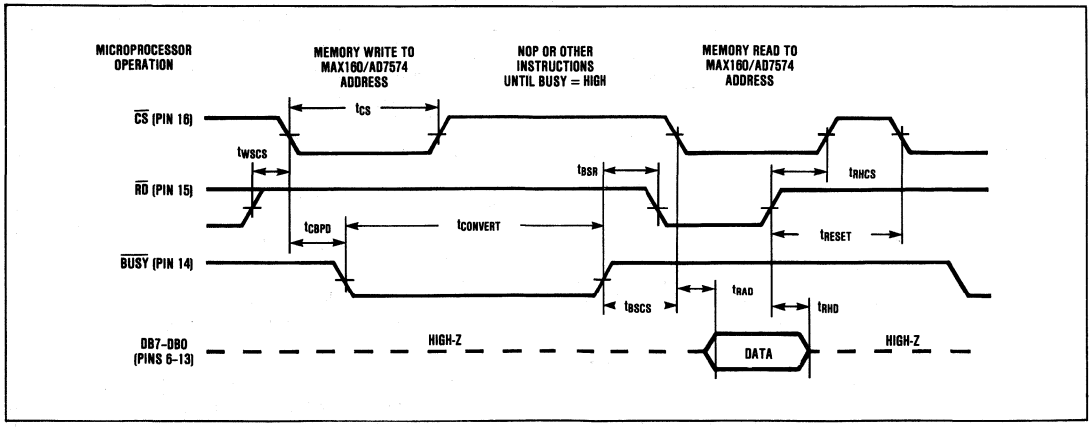


Figure 5. Static RAM Mode Timing Diagram

μP Compatible 8 Bit A/D Converter

Table 6. Truth Table, Rom Mode

INPUTS		OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	⌐	H	HI-Z to DATA	Data Read
L	⌐	⌐	DATA to HI-Z	Reset and Start New Conversion
L	⌐	L	HI-Z	No Effect (Converter Busy)
L	⌐	L	HI-Z	Not Allowed, Conversion Error

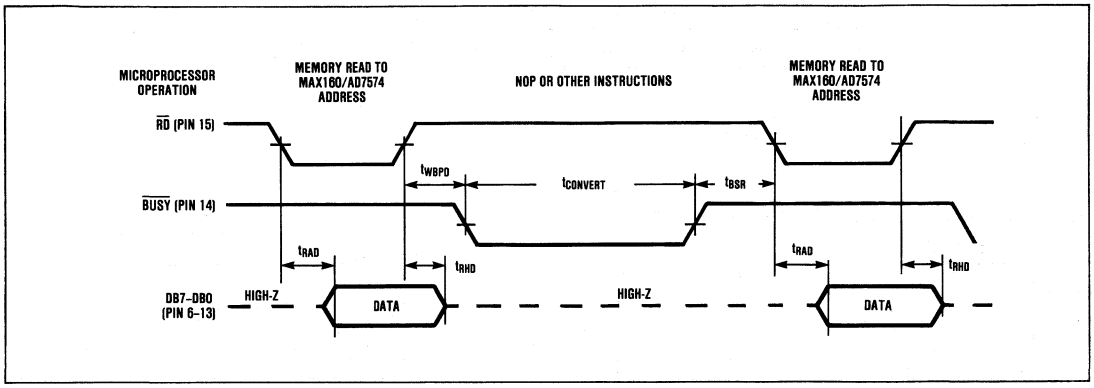


Figure 6. ROM Mode Timing Diagram ($\overline{CS}$ Held Low)

Table 7. Truth Table, Slow Memory Mode

INPUTS	OUTPUTS		MAX160/AD7574 OPERATION
$\overline{CS}$ & $\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
H	H	HI-Z	Not Selected
⌐	H → L	HI-Z	Start Conversion
L	L	HI-Z	Conversion in Progress. μP in WAIT State
L	⌐	HI-Z to DATA	Conversion Complete. μP READS Data
⌐	H	DATA to HI-Z	Converter Reset and Deselected
H	H	HI-Z	Not Selected

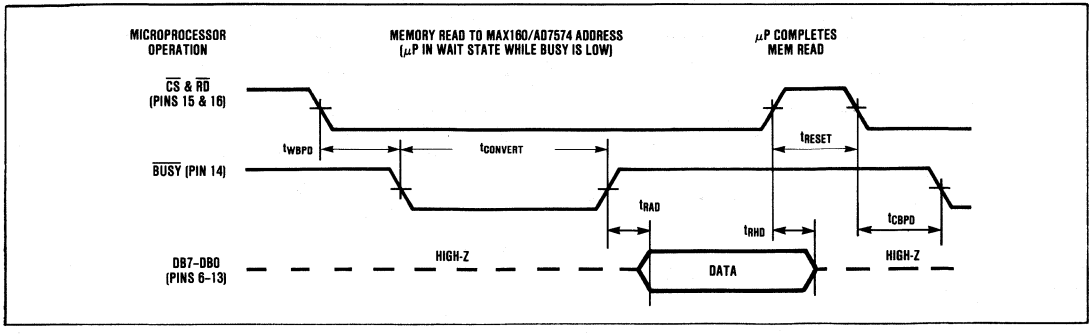


Figure 7. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)

Digital Interface

The MAX160/AD7574 has three interface modes which are determined by the timing of the CS and RD inputs.

Static RAM Interface Mode

Table 5 and Figure 5 show the truth table and timing requirements for interfacing the MAX160/AD7574 as a static RAM.

A conversion is started by executing a memory WRITE instruction to the MAX160/AD7574 address. Once a conversion is in progress, subsequent WRITE operations have no effect. Data is read by executing a memory READ operation to the A/D's address.

$\overline{BUSY}$ must be high before a READ is attempted. In other words, the elapsed time between WRITE and READ must be greater than the conversion time. Once $\overline{BUSY}$ is HIGH (end of conversion) the data READ can be performed. The data readout is destructive, since the MAX160/AD7574 is internally reset when $\overline{RD}$ goes high. Note that $\overline{CS}$ remaining LOW longer than the hold time (t_{RHCS}) will initiate a new conversion.

ROM Interface Mode

Table 6 and Figure 6 show the truth table and timing requirements for interfacing the MAX160/AD7574 as Read Only Memory.

In this mode the $\overline{CS}$ input is not used and is held low. The $\overline{RD}$ input is derived from the decoded device address. A data READ is initiated by executing a memory READ instruction to the MAX160/AD7574 address location. A conversion automatically starts when $\overline{RD}$ returns HIGH. Similar to the RAM mode, attempting a READ before $\overline{BUSY}$ goes HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is poorly defined in time since the conversion is performed at the end of a previous READ operation. This problem can be overcome by performing two READ operations back to back and only using the data from the second read.

Slow-Memory Interface Mode

Table 7 and Figure 7 show the truth table and timing requirements for interfacing the MAX160/AD7574 as slow memory. This mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX160/AD7574 conversion time.

In this mode $\overline{CS}$ and $\overline{RD}$ are tied together. The decoded device address is used to drive CS/RD. The $\overline{BUSY}$ output is connected to the processor's READY input. A conversion is initiated by executing a memory READ to the MAX160/AD7574 address. $\overline{BUSY}$ then goes LOW and forces the processor into a WAIT state. At the end of the conversion, $\overline{BUSY}$ returns high and the data is available at the data outputs.

The major advantage of the slow memory mode is that it allows the processor to start and end a conversion and read the result with a single READ instruction.

Do not attempt a memory WRITE in this mode, since a three-state bus conflict will arise.

Interface Application Hints

Timing and Control

Failure to observe the timing restrictions of Figures 5-7 may cause the MAX160/AD7574 to change interface modes. For example, in the RAM mode, if $\overline{CS}$ is held low for too long, the converter moves into the ROM mode since a new conversion starts.

Logic Deglitching in μP Applications

Unspecified states in the address bus can cause glitches at the MAX160/AD7574 $\overline{CS}$ or $\overline{RD}$ inputs. Such glitches can cause undesired conversion starts, resets or data reads. The best method for avoiding these problems is to gate the address decode with $\overline{WR}$ or $\overline{RD}$ when in the RAM or ROM modes. In the slow memory mode use latched address inputs.

Initialization After Power-Up

To initialize the MAX160/AD7574 at power-up, perform a memory READ to its address location and ignore the data.

Clock

Internal Oscillator

The MAX160/AD7574 has in internal asynchronous clock oscillator which starts when a convert command is received and stops at the end of a conversion.

The oscillator requires an external resistor and capacitor connected as shown in Figure 8. The internal oscillator has good initial accuracy and stability over temperature and supply voltage. See Typical Operating Characteristics for typical conversion times versus R_{CLK} with C_{CLK} set at 100pF.

To prevent false triggering of the internal clock, R_{CLK} and C_{CLK} must be placed close to the CLK pin and coupling from the $\overline{CS}$ and $\overline{RD}$ inputs must be minimized.

µP Compatible 8 Bit A/D Converter

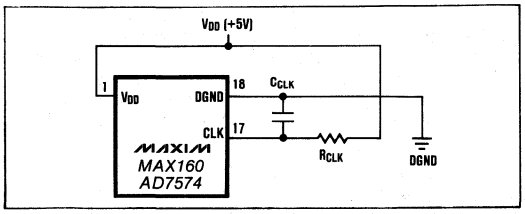


Figure 8. Connecting R_{CLK} and CLK to CLK Oscillator

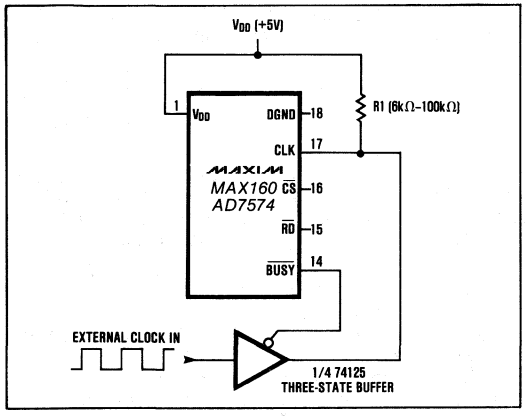


Figure 9. External Clock Operation (Static RAM and Slow Memory Mode)

Operation With External Clock

For applications where synchronous operation is required or the conversion time must be accurately controlled, an external clock can be used.

Figure 9 shows how an external clock is connected. The BUSY output is connected to the three-state enable input of a 74125 buffer. A 500kHz clock provides a conversion time of 15µs.

The external clock should be used only in the static-RAM or slow-memory modes and *not* in the ROM mode. Timing constraints for the external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

2. A data READ can be performed at any time after BUSY = HIGH.

SLOW MEMORY MODE

1. When starting a conversion, $\overline{CS}$ and $\overline{RD}$ should go low on a positive clock edge to provide optimum settling time for the MSB.

Analog Considerations

Application Hints

Input Loading at V_{REF}, A_{IN}, and B_{OFS}

To prevent input loading effects due to the finite input resistance of these pins, low impedance driving sources must be used (i.e. op-amp buffers, or low output impedance references).

Ratiometric Operation

Ratiometric operation is inherent for the multiplying DAC scheme used on the MAX160/AD7574. However, the user must recognize that comparator limitations such as offset voltage, input noise and gain degrade the transfer function at reference voltages less than -10V.

Offset Correction

Offset error in the transfer function can be trimmed by offsetting the buffer that drives the A_{IN} input. This can be achieved either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's non-inverting input. An example of the latter method can be seen in Figure 12.

Analog and Digital Ground

It is recommended that the AGND and DGND pins be connected locally to prevent noise injection into the A/D converter. In systems where the AGND-DGND connection is not local, clamp diodes should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other.

Unipolar Binary Operation

Figures 10 shows the analog circuit connections and nominal transfer characteristic for unipolar operation. Calibration is as follows:

Offset

If offset trimming is required, it must be done in the signal conditioning circuitry used to drive the A_{IN} input in Figure 10. See also the offset trim example shown in Figure 12.

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R1 (i.e. +39.1 mV at R1).

2. Adjust the offset potentiometer until DB7-DB1 are LOW and DB0 flickers.

Gain (Full Scale)

Offset adjustment must be performed prior to gain adjustment. To trim gain:

1. Apply -9.961V to the input of the buffer that drives R1 (i.e. +9.961V at R1)

2. Adjust trimpot R2 until DB7-DB1 are HIGH and DB0 flickers.

Bipolar (Offset Binary) Operation

Figure 11 illustrates the analog circuitry and transfer function for bipolar operation. The output coding is offset binary. Offset correction can be performed at the buffer amplifier used to drive the signal input terminals of the MAX160/AD7574. See Figure 12 for an example of how offset trimming can be performed. Calibration is as follows:

1. Adjust R6 and R7 for minimum resistance across the potentiometers.

2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R6). Then trim R6 or R7 (whichever is required) until DB7-DB1 are LOW and DB0 flickers.

3. Apply 0V to the buffer amplifier used to drive the signal input terminals. Then trim the offset circuit of the buffer amplifier until the ADC output flickers between 01111111 and 10000000.

4. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R6). Then trim R2 until DB7-DB1 are LOW and DB0 flickers.

5. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R6). If the ADC output code is not 11111110 +/-1 bit, repeat the calibration procedure.

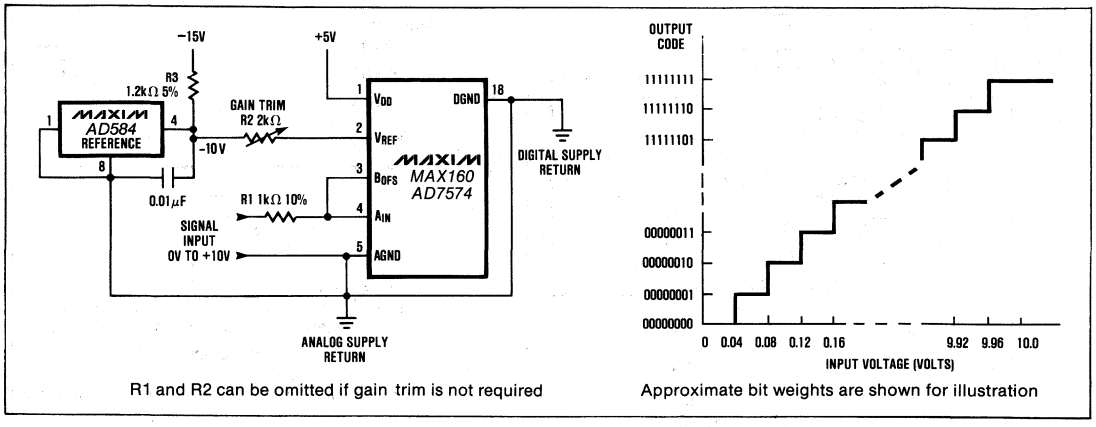


Figure 10. Unipolar (0V to +10V) Operation and Nominal Transfer Characteristic (Output Code is Straight Binary)

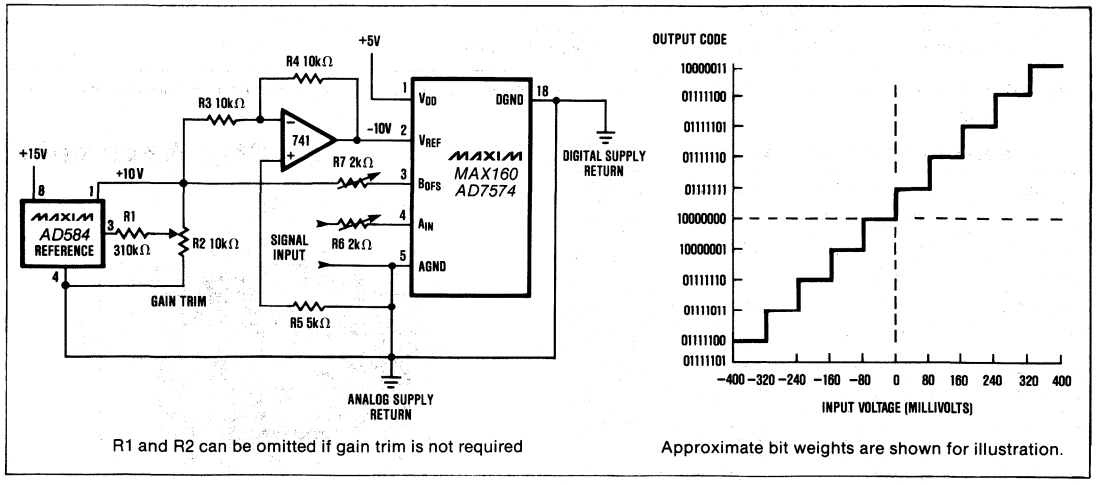


Figure 11. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Offset Binary)

μP Compatible 8 Bit A/D Converter

Bipolar (Complementary Offset Binary) Operation

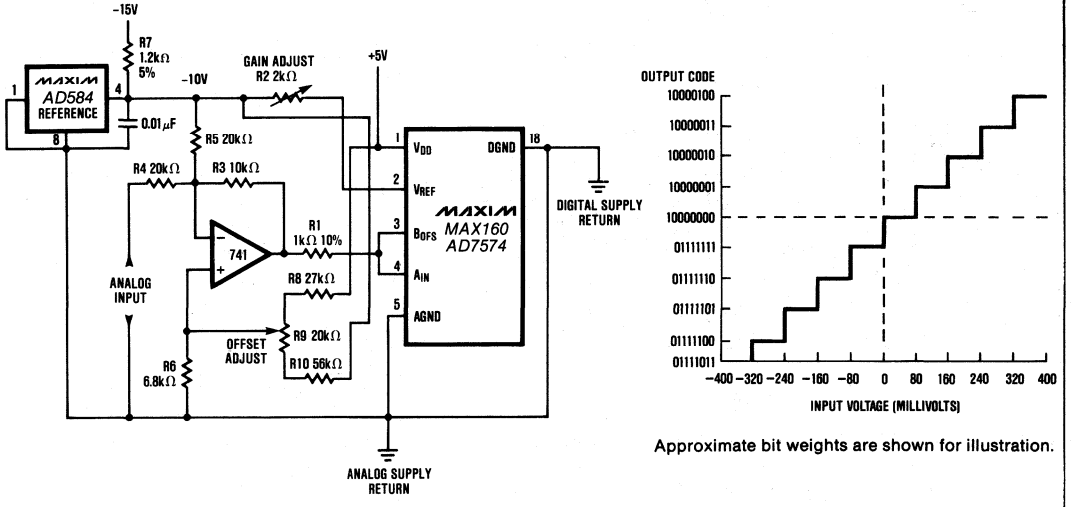
Figure 12 shows the analog connections for offset binary operation. The typical transfer characteristic is also shown. In this bipolar mode, the input signal (-10 to +10V) is conditioned and the A/D basically operates in unipolar mode (0 to +10V). Calibration is as follows (offset adjusted before gain):

Offset

1. Apply 0V to the analog input shown in Figure 12.
2. Adjust R9 until the converter output flickers between codes 01111111 and 10000000.

Gain (Full Scale)

1. Apply -9.922V across the analog input terminals shown in Figure 12.
2. Adjust R2 until DB7-DB1 are HIGH and DB0 flickers between HIGH and LOW.



Note 1: R1 and R2 can be omitted if gain trim is not required.
Note 2: R8, R9 and R10 can be omitted if offset trim is not required.
Note 3: R6||R8||R10 = 5kΩ. If R8, R9 and R10 are not used, make R_6 = 5kΩ.

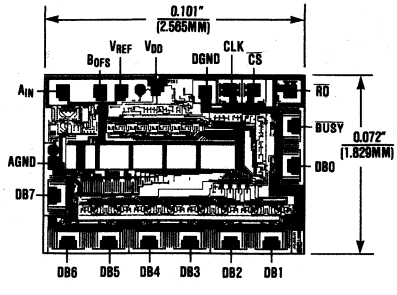
Figure 12. Bipolar (-10V to +10V) Operation and Nominal Transfer Characteristic Around Major Carry (Output Code is Complimentary Offset Binary)

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE†	ERROR
AD7574AQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7574BQ	-25°C to +85°C	CERDIP**	±¾ LSB
AD7574SQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7574TQ	-55°C to +125°C	CERDIP**	±¾ LSB
AD7574AD	-25°C to +85°C	Ceramic	±½ LSB
AD7574BD	-25°C to +85°C	Ceramic	±¾ LSB
AD7574SD	-55°C to +125°C	Ceramic	±½ LSB
AD7574TD	-55°C to +125°C	Ceramic	±¾ LSB

† *All devices — 18 lead packages*
** Maxim reserves the right to ship Ceramic Packages in lieu of *CERDIP packages.*

Chip Topography



MAXIM

CMOS 8-Bit 8-Channel Data Acquisition System

General Description

The MAX161 and AD7581 are CMOS single-chip 8-bit, 8-channel data acquisition systems (DAS). Each chip includes an 8-bit A/D converter, 8-channel multiplexer, 8 x 8 dual port RAM with contention logic, and microprocessor compatible I/O logic. When combined with a voltage reference, a complete data acquisition system is produced that interfaces with the majority of microprocessors.

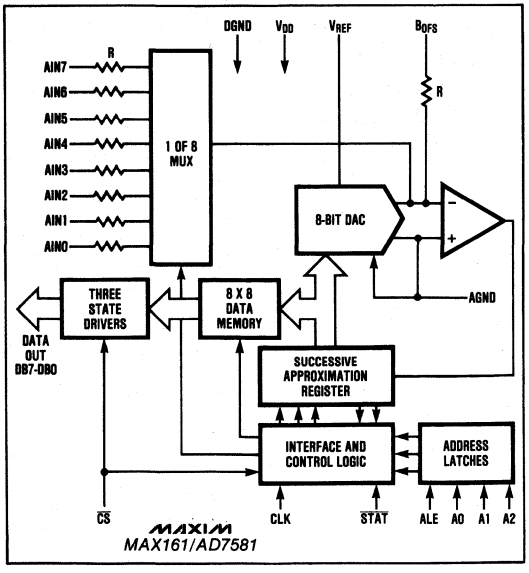
Conversions take place on a continuous, channel sequencing basis using a microprocessor clock or control signal. Data is stored automatically in dual port RAM so that any channel can be read at any time under microprocessor control.

The MAX161 is an enhanced, pin-compatible version of the AD7581. Improvements include faster conversion and interface timing, lower zero error and drift, reduced power dissipation, and availability in military temperature grades. All devices are available in 28 pin DIP and Small Outline (SO) packages.

Applications

Digital Signal Processing
Data Loggers
Automatic Test Equipment
Robotics
Process Control

Functional Diagram



Features

- ♦ **Fast Conversion Time: 20μsec (MAX161)**
- ♦ **No Missing Codes Over Temperature**
- ♦ **On Chip 8 x 8 Dual Port RAM**
- ♦ **Interfaces Directly To Z80/8085/6800**
- ♦ **Ratiometric Capability**
- ♦ **Interleaved DMA Operation**

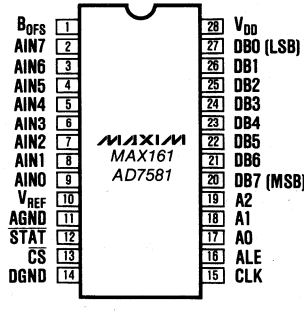
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX161ACPI	0° C to +70° C	Plastic DIP	1 7/8 LSB
MAX161BCPI	0° C to +70° C	Plastic DIP	3/4 LSB
MAX161CCPI	0° C to +70° C	Plastic DIP	1/2 LSB
MAX161ACWI	0° C to +70° C	Small Outline	1 7/8 LSB
MAX161BCWI	0° C to +70° C	Small Outline	3/4 LSB
MAX161CCWI	0° C to +70° C	Small Outline	1/2 LSB
MAX161CC/D	0° C to +70° C	Dice	1 7/8 LSB
MAX161AEPI	-40° C to +85° C	Plastic DIP	1 7/8 LSB
MAX161BEPI	-40° C to +85° C	Plastic DIP	3/4 LSB
MAX161CEPI	-40° C to +85° C	Plastic DIP	1/2 LSB
MAX161AEWI	-40° C to +85° C	Small Outline	1 7/8 LSB
MAX161BEWI	-40° C to +85° C	Small Outline	3/4 LSB
MAX161CEWI	-40° C to +85° C	Small Outline	1/2 LSB
MAX161AMJI	-55° C to +125° C	CERDIP**	1 7/8 LSB
MAX161BMJI	-55° C to +125° C	CERDIP**	3/4 LSB
MAX161CMJI	-55° C to +125° C	CERDIP**	1/2 LSB

** All devices — 28 lead packages*
*** Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*
Ordering Information continued on last page.

Pin Configuration

Top View



CMOS 8-Bit 8-Channel Data Acquisition System

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... +7V
V_{DD} to DGND ..... +7V
AGND to DGND ..... -0.3V, V_{DD}
Digital Input Voltage to DGND
(pins 13,16-19) ..... -0.3V, V_{DD}
Digital Output Voltage to DGND
(pins 12,20-27) ..... -0.3V, V_{DD}
CLK (pin 15) input voltage to DGND ..... -0.3V, V_{DD}
V_{REF} (pin 10) to AGND ..... ±25V
V_{BOFS} (pin 1) to AGND ..... ±17V
AIN (0-7) (pins 9-2) ..... ±17V

Operating Temperature Range
MAX161XC, AD7581J/K/L ..... 0°C to +70°C
AD7581A/B/C ..... -25°C to +85°C
MAX161XE ..... -40°C to +85°C
MAX161XM, AD7581S/T/U ..... -55°C TO +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Package)
Plastic DIP (Derate 12mW/°C above +50°C) 1200mW
Ceramic (Derate 10mW/°C above +50°C) 1000mW
CERDIP (Derate 10mW/°C above +50°C) 1000mW
Small Outline (Derate 12mW/°C above +50°C) 1000mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = -10V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
ACCURACY (at f_{CLK} = 4.0MHz for MAX161, 1.2MHz for AD7581)							
Resolution				8			Bits
Relative Accuracy		MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U			±¾ ±½ ±¼	±1⅞ ±¾ ±½	LSB
Differential Nonlinearity		MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U			±¾ ±½ ±¼	±1⅞ ±⅞ ±¾	LSB
Offset Error (See Figure 5, Note 1)		**Adjustable to zero**	**MAX161A** **MAX161B** **MAX161C**		**±60** **±40** **±20**	**±120** **±60** **±40**	mV
			AD7581J/A/S AD7581K/B/T AD7581L/C/U		±60 ±40 ±20	±200 ±80 ±50	
Gain Error, Worst Channel (See Figure 5, Note 2)		Adjustable to zero	MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U		±3 ±2 ±1	±6 ±4 ±2	LSB
Gain Match Between Channels (See Figure 5)		Adjustable to zero	MAX161A, AD7581J/A/S MAX161B, AD7581K/B/T MAX161C, AD7581L/C/U		2 1 ½	3 2 1	LSB
B_{OFS} Gain Error (Note 3)					±1		LSB
ANALOG INPUTS							
Input Resistance at V_{REF}, B_{OFS}, and AIN7-AIN0	R_{IN}	Pins 1 to 10 (Note 4)		10	20	30	kΩ
V_{REF} (For Specified Performance)	V_{REF}			-10.5		-9.5	V
V_{REF} Range					-5V to -15V		V
Nominal Analog Input Range		+Unipolar Mode (See Figure 5) -Unipolar Mode (See Figure 7) Bipolar Mode (See Figure 9)		0 $-V_{REF}$ $-V_{BOFS}$		$+V_{REF}$ 0 $\lvert V_{REF}\rvert$ $-V_{BOFS}$	V
DIGITAL INPUTS ($\overline{CS}$, ALE, CLK, A0-A2)							
Logic HIGH Threshold	V_{INH}			+2.4	+2.0		V
Logic LOW Threshold	V_{INL}				+1.2	+0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			0.01	1	µA
Input Capacitance	C_{IN}	(Note 5)			4	5	pF

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{REF} = -10V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DIGITAL OUTPUTS (STAT, DB0-DB7)						
Output HIGH Voltage	V_{OH}	I_{SOURCE} = 40μA	4.5	4.8		V
Output LOW Voltage	V_{OL}	I_{SINK} = 1.6mA		0.2	0.6	V
Floating State Leakage	I_{LKG}	DB0-DB7		0.3	10	μA
Floating State Capacitance		DB0-DB7, V_{OUT} = 0V to V_{DD}		5	10	pF
Output Code		See Figure 5 See Figure 7 See Figure 9	Unipolar Binary Complementary Binary Offset Binary			
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		+4.5	+5.0	+5.5	V
Supply Current	I_{DD}	MAX161, AD7581 Static		3	5	mA
		MAX161 Dynamic (f_{CLK} = 4.0MHz)		**3**	**5**	
		AD7581 Dynamic (f_{CLK} = 1.2MHz)		3	8	

Note 1. Typical offset temperature coefficient is **±25μV/°C for the MAX161** and ±150μV/°C for the AD7581.
Note 2. Gain error is measured after offset calibration. Maximum full scale change for any channel from +25°C to T_{MIN} or T_{MAX} is ±2LSBs.
Note 3. Typical change in B_{OFS} gain from +25°C to T_{MIN} or T_{MAX} is ±2LSBs.
Note 4. R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 7 and 9.
Note 5. Guaranteed but not 100% tested.

TIMING CHARACTERISTICS — MAX161 (C_L = 100pF, See Figure 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
ALE Pulse Width	t_H	**50**	**35**		**ns**
Address Valid to Latch Set-Up Time	t_{ALS}	**45**	**30**		**ns**
Address Valid to Latch Hold Time	t_{ALH}	**10**	**0**		**ns**
Address Latch to $\overline{CS}$ Set-Up Time	t_{LCS}	**10**	**0**		**ns**
$\overline{CS}$ to Output Propagation Delay	t_{ACC}		**125**	**200**	**ns**
$\overline{CS}$ Pulse Width	t_{CW}	**250**	**175**		**ns**
$\overline{CS}$ to Output Float Propagation Delay	t_{CF}		**30**	**50**	**ns**
$\overline{CS}$ to Low Impedance Bus	t_{CLZ}		**70**	**100**	**ns**
Clock Frequency (Note 6)	f_{CLK}		**6**	**4.0**	**MHz**

TIMING CHARACTERISTICS — AD7581 (C_L = 100pF, See Figure 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
ALE Pulse Width	t_H	80	50		ns
Address Valid to Latch Set-Up Time	t_{ALS}	70	45		ns
Address Valid to Latch Hold Time	t_{ALH}	20	10		ns
Address Latch to $\overline{CS}$ Set-Up Time	t_{LCS}	20	10		ns
$\overline{CS}$ to Output Propagation Delay	t_{ACC}		200	250	ns
$\overline{CS}$ Pulse Width	t_{CW}	280	250		ns
$\overline{CS}$ to Output Float Propagation Delay	t_{CF}		50	80	ns
$\overline{CS}$ to Low Impedance Bus	t_{CLZ}		100	150	ns
Clock Frequency (Note 6)	f_{CLK}		1.6	1.2	MHz

Note 6. Guaranteed conversion time for stated accuracy of 20μs/channel with 4.0MHz clock for MAX161, and 66.7μs/channel with 1.2MHz clock for the AD7581.

CMOS 8-Bit 8-Channel Data Acquisition System

Detailed Description

Basic Operation

The MAX161 and AD7581 sequentially convert analog signals on 8 input channels into separate 8-bit data words. The data is continually updated in on-chip RAM, with each channel's conversion result assigned to a separate RAM address. Consequently, the conversion process is user transparent in that output data is read directly from RAM. The device can run directly from a microprocessor clock (6800 type systems) or control signal (ALE in 8085 type systems). A functional diagram of the MAX161 and AD7581 is shown on the front page.

A/D Conversion

Internally, the conversion process is divided into 10 phases, each 8 clock periods long. In the first phase, the input multiplexer is decremented and the control logic is reset. STAT (pin 12) goes low for 8 clock cycles at the beginning of this period. (STAT also goes low for 72 clock periods after channel 1 is converted). The successive approximation A/D conversion then takes place during phases 2 through 9. Finally, data is loaded into RAM during phase 10.

A single channel conversion takes 80 input clock periods while a complete scan through all channels requires 640 clock periods. Internal start-up logic initializes the converter within 800 clock periods after power is applied.

Digital Interface

Channel Selection

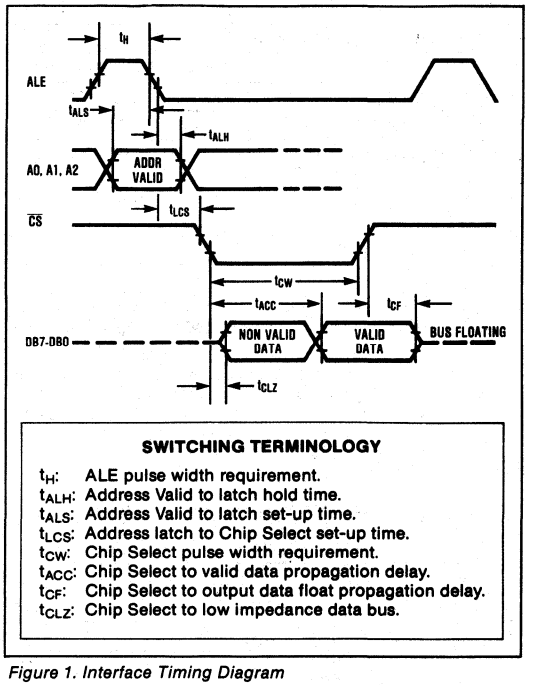
Table 1 shows the truth table for channel selection. RAM locations are addressed by AO-A2. In systems with a multiplexed address/data bus, the address is latched by ALE (pin 16). Alternatively, when address and data busses are separate, the address latches can be made transparent by tying ALE HIGH.

Table 1:
Channel Selection Truth Table

A2	A1	A0	ALE	CHANNEL DATA TO BE READ
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Timing And Control

Control timing for the MAX161 and AD7581 is shown in Figure 1. When CS (pin 13) is HIGH, the three-state data drivers are in their high impedance state. The drivers switch to the active state when CS goes LOW. Output data is valid after time t_{ACC}.



SWITCHING TERMINOLOGY

- t_H: ALE pulse width requirement.
- t_{ALH}: Address Valid to latch hold time.
- t_{ALS}: Address Valid to latch set-up time.
- t_{LCS}: Address latch to Chip Select set-up time.
- t_{CW}: Chip Select pulse width requirement.
- t_{ACC}: Chip Select to valid data propagation delay.
- t_{CF}: Chip Select to output data float propagation delay.
- t_{CLZ}: Chip Select to low impedance data bus.

Figure 1. Interface Timing Diagram

Data Read Operation

The MAX161 and AD7581 continuously scan and convert analog input signals without regard to the channel being selected for data output. The on-chip RAM and contention logic allow data to be read asynchronously with respect to the conversion process. The output data (RAM contents) is simply the most recent conversion result for the selected channel.

Automatic Interleaved DMA is provided by internal logic to ensure that memory updates do not take place when the memory is being addressed by a microprocessor. RAM is normally updated on a rising clock edge, 6 clock periods prior to STAT going LOW, provided CS is HIGH (i.e. data is not being read). If CS is LOW (read operation in progress), then the memory update is delayed by 3 clock periods. By delaying the update, data will not be written in RAM during a READ as long as CS is kept shorter than 3 clock periods. The possibility of a "contention" error with an asynchronous READ is therefore eliminated if CS is less than 3 clock periods long. Although asynchronous reading errors are eliminiated with this feature, it in no way restricts compatibility with other manufacturers' AD7581s.

Channel Identification

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To do this, the channel that is currently converting must be identified. $\overline{STAT}$ provides an identifying signal by staying low for an extended time (72 vs. 8 clock periods) when channel 0 is active (see Figure 2). Note that input channels are scanned in reverse order, i.e. AIN7,6...1,0.

A simple circuit for channel identification using $\overline{STAT}$ is shown in Figure 3. The time constant, RC, is chosen such that X2 ignores the short $\overline{STAT}$ pulses but responds to the wider (72 clock periods) pulse width occuring during channel 0 conversion. With a 1μs clock period, use 0.022μF for C and 1.8kΩ for R. An alternate means of channel identification uses the microprocessor to periodically interrogate the $\overline{STAT}$ output. A simple routine is shown in Figure 4.

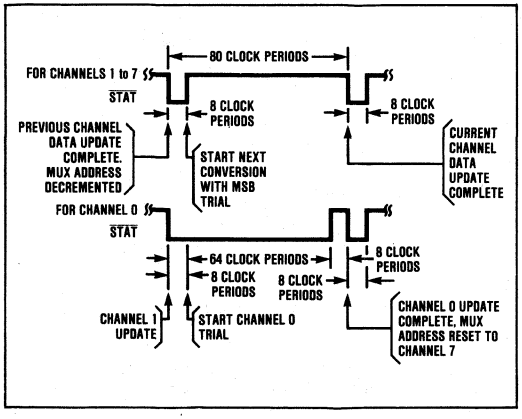


Figure 2. $\overline{STAT}$ Timing Diagram

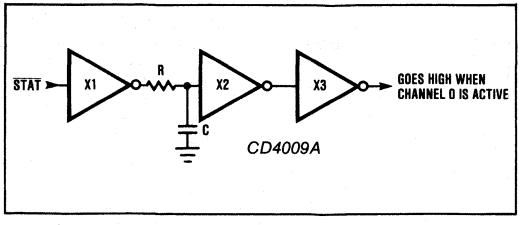


Figure 3. Hardware Channel Identification

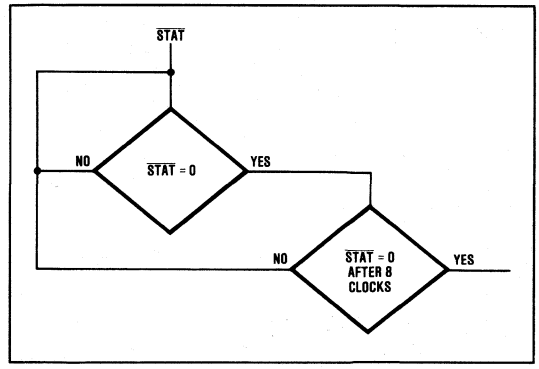


Figure 4. Software Channel Identification

Operating Circuits

For the following circuits, the offset and gain adjustments shown in Figures 5, 7 and 9 are often not needed (The offset and gain error of the MAX161C are 1LSB and 2LSB respectively). In those cases, A1 and R1–R12 can be omitted. Note that in all cases where full scale is adjusted, offset must be trimmed first.

Unipolar Binary Operation

Figures 5 and 6 show the analog circuit connections and the resulting transfer characteristic for basic unipolar operation (0 to +10V input). A -10V reference is connected to pin 10 through resistor R9 and a clock is connected to pin 15. Calibration is as follows:

Offset

Offset (zero error) is trimmed using the bipolar offset pin, B_{OFS}. Resistors R10–R12 form a voltage divider buffered by A1 which drives B_{OFS}. A0–A2 are taken LOW and latched using ALE so that channel 0 is continuously monitored. With AIN0 = +19.5mV (i.e. 1/2 LSB for 10V full scale) adjust R11 until DB7–DB1 are LOW and DB0(LSB) flickers. The offset of all channels is identical so one adjustment takes care of all eight inputs.

Full Scale

Apply +9.941V (F.S.-3/2LSB) to all inputs (AIN0–AIN7), then select one channel using A0–A2, and latch the address with ALE. Adjust trimmer RN of the selected input so that DB7–DB1 are HIGH and DB0 (LSB) flickers. Repeat for other channels.

CMOS 8-Bit 8-Channel Data Acquisition System

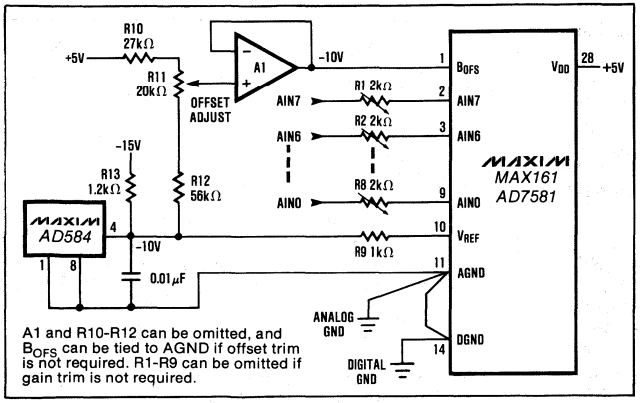


Figure 5. Unipolar (0 to +10V) Operation

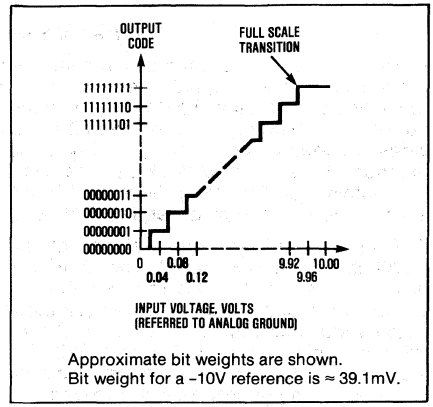


Figure 6. Unipolar (0 to +10V) Transfer Characteristic

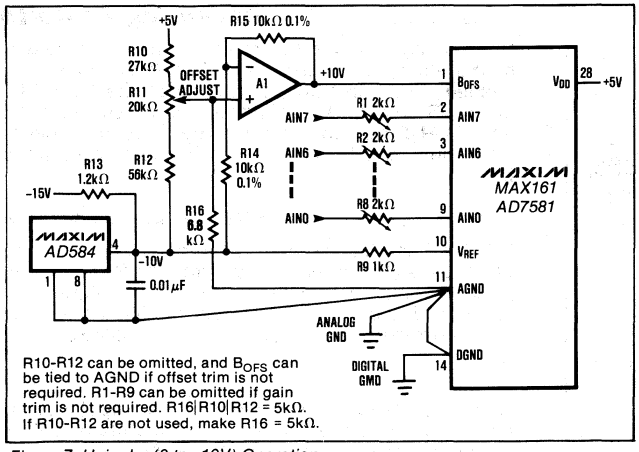


Figure 7. Unipolar (0 to -10V) Operation

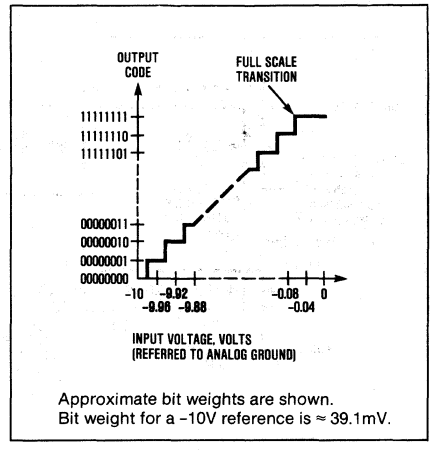


Figure 8. Unipolar (0 to -10V) Transfer Characteristic

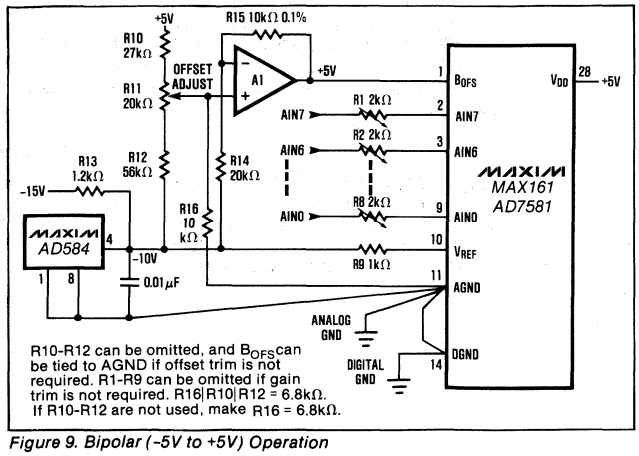


Figure 9. Bipolar (-5V to +5V) Operation

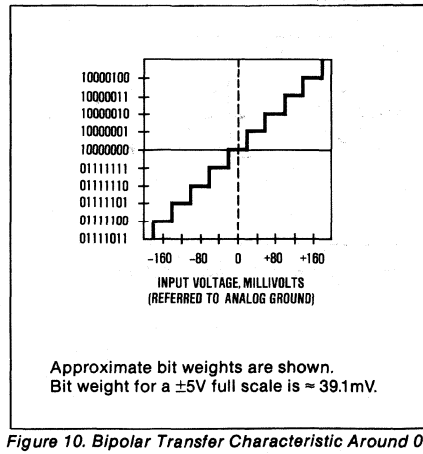


Figure 10. Bipolar Transfer Characteristic Around 0V

MAXIM

Unipolar (Complimentary Binary) Operation

Figures 7 and 8 show the analog circuit connections and typical transfer characteristic for unipolar (0 to -10V input) complementary binary operation. Calibration is as follows:

Offset

A0-A2 are taken LOW and latched using ALE, activating channel 0. The offset voltage is identical for all channels so only one trim is needed. With AIN0 = -9.98V (i.e. -F.S.+1/2LSB), adjust R11 so that DB7-DB1 are LOW and DB0 (LSB) flickers.

Full Scale

Apply -58.6mV (3/2 LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB7-DB1 are HIGH and the DB0 (LSB) flickers. Repeat for other channels.

Bipolar (Offset Binary) Operation

Figures 9 and 10 show the analog circuit connections and typical transfer characteristic for ±5V bipolar operation. Calibration is as follows:

Offset

A0-A2 are taken LOW and latched using ALE, selecting channel 0. The offset error is identical for all channels so only one trim is needed. With AIN0 = -4.980V (i.e. -F.S.+1/2LSB), adjust R11 so that DB1-DB7 are LOW and DB0 (LSB) flickers.

Full Scale

Apply +4.941V (+F.S.-3/2LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB1-DB7 are HIGH and DB0 (LSB) flickers. Apply -19.5mV to each gain trimmed channel. If the output code does not flicker between 01111111 and 1000000, repeat the calibration procedure.

Application Hints

Analog and Digital Ground

AGND and DGND should be connected together at the device to prevent the possibility of injecting noise into the A/D converter. In systems where the AGND-DGND connection is not local, connect clamp diodes (1N914 or equivalent) between the AGND and DGND pins.

VDD (pin 28) should be bypassed to AGND using a 10µF electrolytic and 0.1 µF ceramic capacitor. Lead lengths should be kept as short as possible.

Logic Deglitching In µP Applications

Unspecified states on the address bus (due to different rise and fall times) can cause glitches at the $\overline{CS}$ pin, initiating unwanted reads. These glitches can be avoided by gating the address decoding logic with $\overline{RD}$ (8085A) or VMA (6800) as shown in Figures 11 and 12.

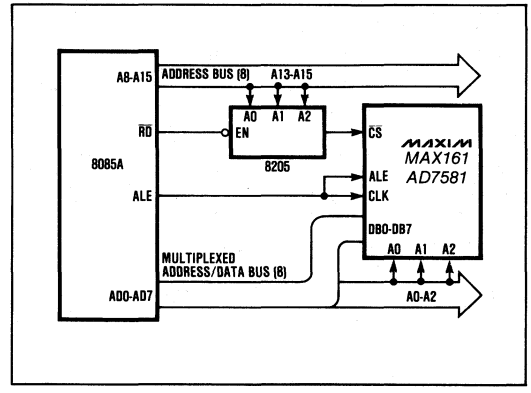


Figure 11. 8085A Interface

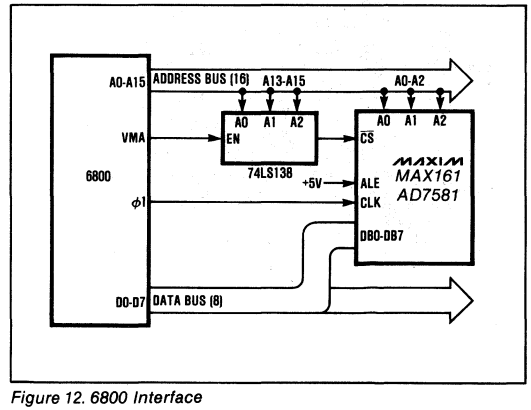


Figure 12. 6800 Interface

CMOS 8-Bit 8-Channel Data Acquisition System

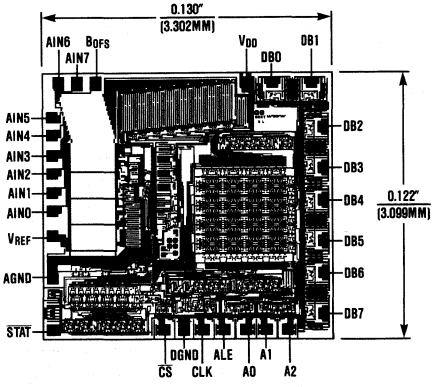
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7581JN	0°C to +70°C	Plastic DIP	1 7/8 LSB
AD7581KN	0°C to +70°C	Plastic DIP	3/4 LSB
AD7581LN	0°C to +70°C	Plastic DIP	1/2 LSB
AD7581JCWI	0°C to +70°C	Small Outline	1 7/8 LSB
AD7581KCWI	0°C to +70°C	Small Outline	3/4 LSB
AD7581LCWI	0°C to +70°C	Small Outline	1/2 LSB
AD7581JC/D	0°C to +70°C	Dice	1 7/8 LSB
AD7581AD	-25°C to +85°C	Ceramic	1 7/8 LSB
AD7581BD	-25°C to +85°C	Ceramic	3/4 LSB
AD7581CD	-25°C to +85°C	Ceramic	1/2 LSB
AD7581AQ	-25°C to +85°C	CERDIP**	1 7/8 LSB
AD7581BQ	-25°C to +85°C	CERDIP**	3/4 LSB
AD7581CQ	-25°C to +85°C	CERDIP**	1/2 LSB
AD7581SQ	-55°C to +125°C	CERDIP**	1 7/8 LSB
AD7581TQ	-55°C to +125°C	CERDIP**	3/4 LSB
AD7581UQ	-55°C to +125°C	CERDIP**	1/2 LSB

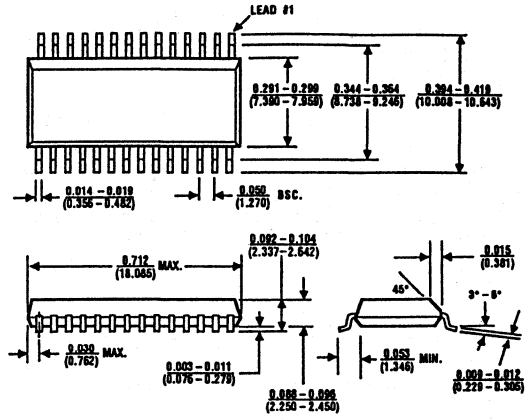
* *All devices — 28 lead packages*

** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*

Chip Topography



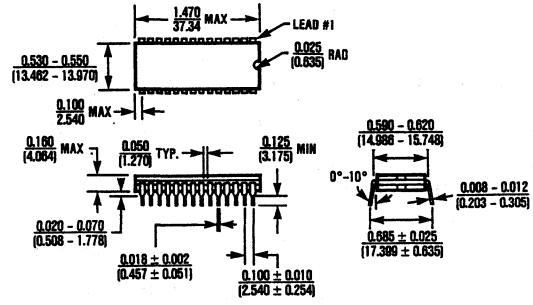
Package Information



28 Lead Small Outline, Wide (WI)

θ_{JA} = 80°C/W

θ_{JC} = 45°C/W



28 Lead CERDIP (JI)

θ_{JA} = 55°C/W

θ_{JC} = 20°C/W

Complete High-Speed CMOS 12-Bit ADC

General Description

The MAX162 and AD7572 are complete 12-Bit analog-to-digital converters (ADC's) that combine high speed, low power consumption, and an on-chip voltage reference. The conversion times are 3μs (MAX162) and 5 and 12μs (AD7572). The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX162/AD7572 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

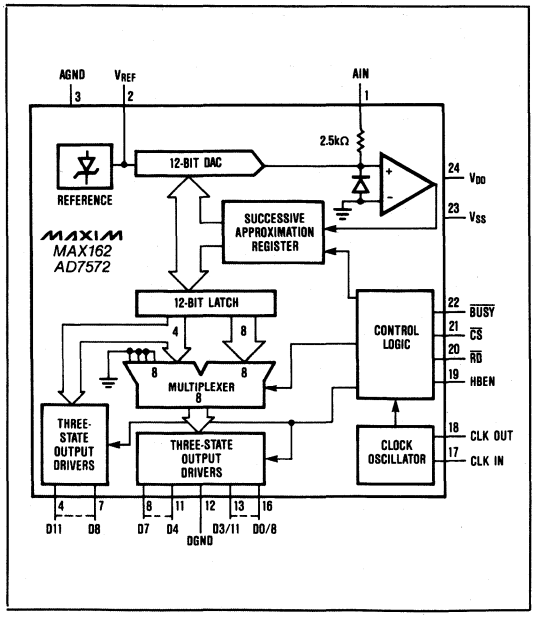
Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Functional Diagram



Features

- 12-Bit Resolution and Linearity
- 3μs (MAX162), 5μs and 12μs (AD7572) Conversion Times
- No missing Codes
- On-Chip Voltage Reference
- 90ns Access Time
- 215mW Max Power Consumption
- 24-Lead Narrow DIP Package

Ordering Information

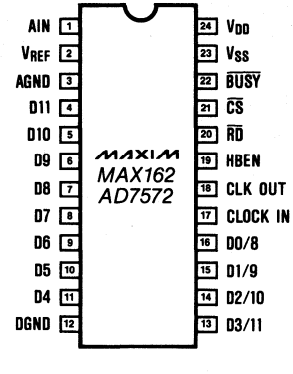
PART	TEMP. RANGE	PACKAGE*	ERROR
3μs CONVERSION TIME			
MAX162ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX162BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX162BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CC/D	0°C to +70°C	Dice**	±1 LSB
MAX162AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX162BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162CING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX162BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX162CMRG	-55°C to +125°C	CERDIP	±1 LSB

* *All devices — 24 lead packages*

** *Consult factory for dice specifications*

Ordering Information continued on last page.

Pin Configuration



Complete High-Speed CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX162XC, AD7572JN, KN, LN,
JCWG, KCWG, LCWG ..... 0°C to +70°C
MAX162XI, AD7572AQ, BQ, CQ ..... -25°C to +85°C
MAX162XM, AD7572SQ, TQ, UQ .... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for AD7572XX05 and 1MHz for AD7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX162A, AD7572L/C/U MAX162B/C, AD7572K/B/T/J/A/S				±1/2 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX162C, AD7572J/A/S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±8	LSB
		MAX162B, AD7572K/B/T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±3 ±6	
		MAX162A, AD7572L/C/U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
Full Scale Error (Note 2)		MAX162C, AD7572J/A/S	T_A = 25°C			±15	LSB
		MAX162B, AD7572K/B/T	T_A = 25°C			±10	
		MAX162A, AD7572L/C/U	T_A = 25°C			±10	
Full Scale Tempco (Notes 3, 4)		MAX162C, AD7572J/A/S MAX162B/A, AD7572K/B/T, AD7572L/C/U				±45 ±25	ppm/°C
ANALOG INPUT							
Input Voltage Range		For Bipolar Input see Figures 19-21		0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)		MAX162C, AD7572J/A/S MAX162B/A, AD7572K/B/T, AD7572L/C/U			40 20		ppm/°C
Output Current Sink Capability		(Note 6)				500	µA
POWER SUPPLY REJECTION							
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V			±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V MAX162/AD7572 MAX162	V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB LSB

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ± 5%, V_{SS} = -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for AD7572XX05 and 1MHz for AD7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	μA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200μA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	μA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF
CONVERSION TIME							
MAX162	t_{CONV}	f_{CLK} = 4MHz	Synchronous (13 clock cycles) Asynchronous (12 to 13 clock cycles)	 3.0		3.25 3.25	μs
AD7572XX05	t_{CONV}	f_{CLK} = 2.5MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 4.8		5 5.2	μs
AD7572XX12	t_{CONV}	f_{CLK} = 1MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	 12		12.5 13	μs
POWER REQUIREMENTS							
V_{DD}		±5% for Specified Performance		4.75	5	5.25	V
V_{SS} (Note 8)		±5% MAX162 ±5% AD7572			-12 or -15 -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V			145	215	mW

Note 1: Typical change over temp is ±1 LSB
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: V_{SS} = -12V ±5% for the MAX162 only. Functional operation is guaranteed by testing offset error and full scale error.

Complete High-Speed CMOS 12-Bit ADC

TIMING CHARACTERISTICS (Note 9)

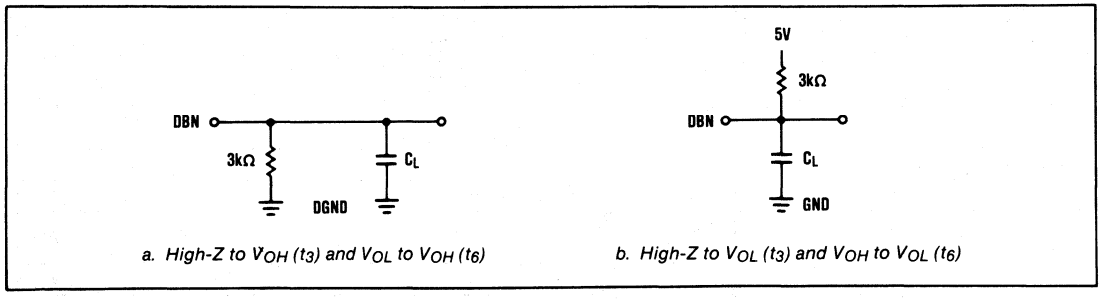
(V_{DD} = +5V, V_{SS} = -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX162C/I AD7572J/K/L AD7572A/B/C		MAX162M AD7572S/T/U		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

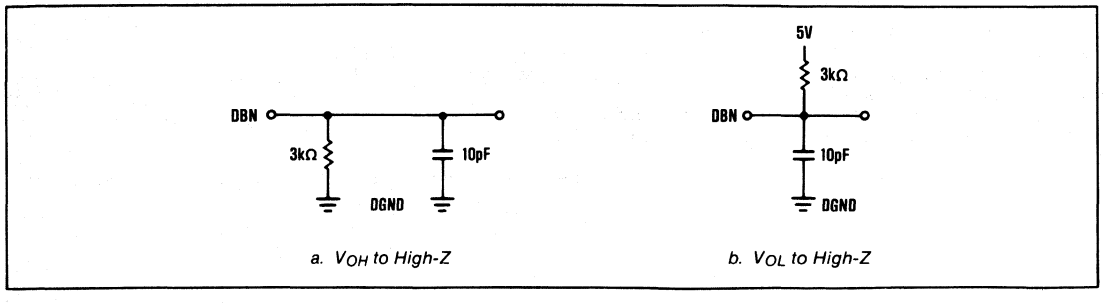
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

Complete High-Speed CMOS 12-Bit ADC

Pin Description

PIN	NAME	FUNCTION
1	AIN	Analog Input, 0 to +5V unipolar input
2	V_{REF}	-5.25V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLKIN	Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. An inverted CLKIN signal appears at this pin.

PIN	NAME	FUNCTION
19	HBEN	High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.
22	$\overline{BUSY}$	The BUSY Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V for AD7572 and -15V or -12V for MAX162.
24	V_{DD}	Positive Supply, +5V.

Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note:
* D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

Converter Operation

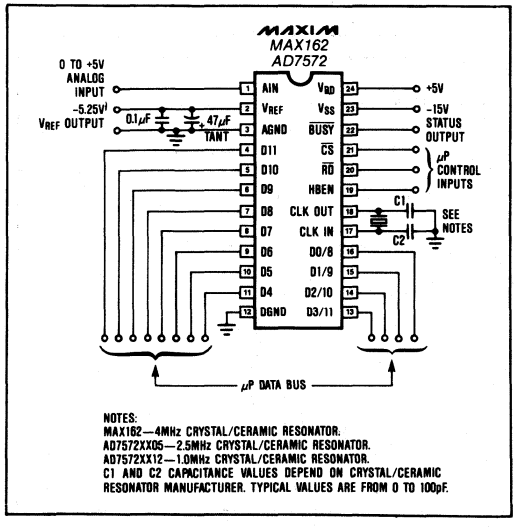


Figure 3. MAX162/AD7572 Operational Diagram

The MAX162 and AD7572 use a successive approximation technique to convert an unknown analog input to a 12 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 3 shows the MAX162/AD7572 in its simplest operational configuration.

Figure 4 shows the MAX162/AD7572 analog equivalent circuit. The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero crossing detector and its output is fed back to the SAR input.

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN digital inputs. A conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN is low. The $\overline{BUSY}$ output goes low as soon as the conversion starts. $\overline{BUSY}$ may be used to control an external sample-and-hold when wide bandwidth input signals are being measured.

Complete High-Speed CMOS 12-Bit ADC

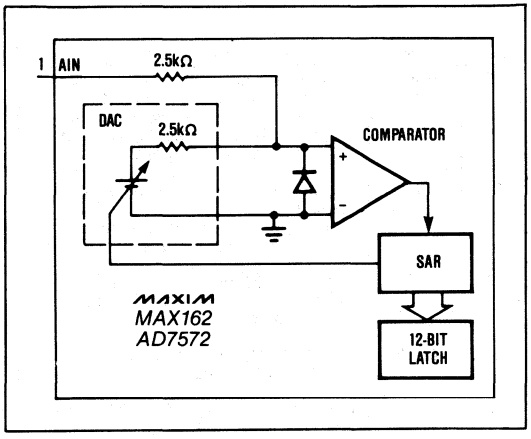


Figure 4. MAX162/AD7572 Analog Equivalent Circuit

The SAR is set to half scale as soon as the $\overline{CS}$ and $\overline{RD}$ inputs go low. This reset is asynchronous with the clock input. The analog input is then compared to one half of the full scale voltage. About 30ns after the second falling edge of CLKIN (or rising edge of CLKOUT), the output of the comparator is latched into the SAR MSB bit (see Figure 5). The bit is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (bit 11) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. Following a falling CLKIN signal, the $\overline{BUSY}$ output goes high and the SAR result is latched into the three-state output buffers.

Clock Operation

Clock Oscillator

Figure 6 shows the MAX162/AD7572 clock circuitry. The capacitive load on the CLKOUT pin must be minimized for low power dissipation and to avoid digital coupling of the CLKOUT buffer currents to the comparator. If an external clock source is being used to drive CLKIN, CLKOUT should be left open. The external clock source must have a 50% duty cycle. If the internal oscillator is being used, a crystal/ceramic resonator should be connected between CLKOUT and CLKIN as shown in Figure 6.

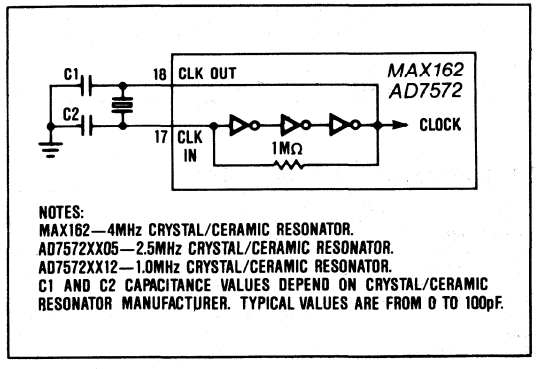


Figure 6. MAX162/AD7572 Internal Clock Circuit

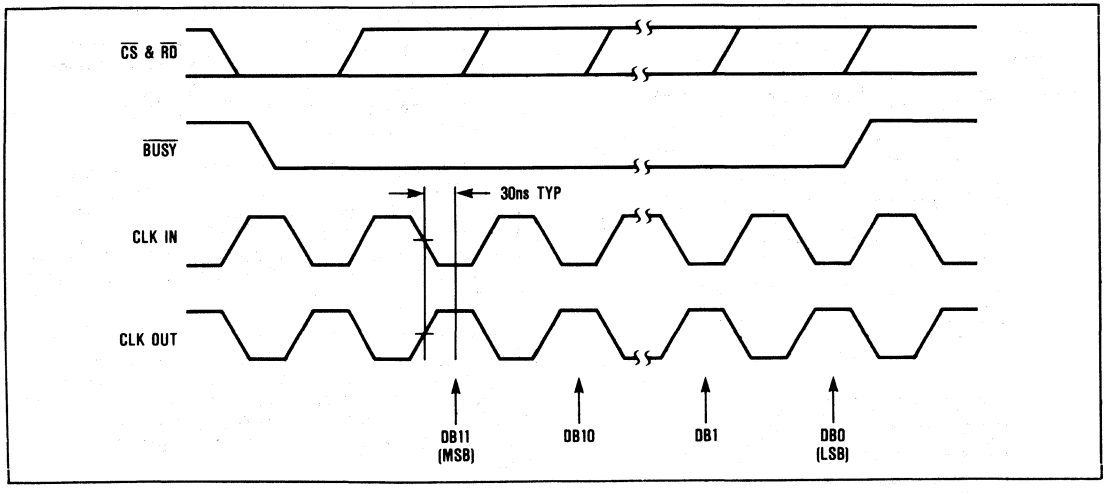


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN.

Control Input Synchronization

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). To ensure a fixed conversion time use the following guidelines for synchronization:

MAX162

For the MAX162 the $\overline{RD}$ input should go low at the falling edge of CLKIN. In this case the conversion lasts 13 clock cycles and the conversion time is 3.25μs when f_{CLK} = 4MHz. If the CLKIN and $\overline{RD}$ falling edges are skewed, the skew must not be more than 50ns to ensure the 13 period conversion time (See Figure 7). The MSB is tried at the second clock falling edge, leaving two clock cycles for the external sample-and-hold to settle from hold transients.

AD7572

The AD7572 $\overline{RD}$ input can go low at the rising edge of CLKIN. In this case the conversion lasts 12.5 clock cycles and the conversion time is 5μs when f_{CLK} = 2.5MHz and 12.5μs when f_{CLK} = 1MHz. The delay from the falling edge of $\overline{RD}$ to the falling edge of CLKIN must not be less than 180ns to ensure the 12.5 clock cycle conversion time (See Figure 8). This leaves the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional half clock cycle of settling can be allowed for driving the sample-and-hold by having $\overline{RD}$ go low at the falling edge of CLKIN, similar to the MAX162. This results in a 13 cycle conversion time (5.2μs when f_{CLK} = 2.5MHz, 13μs when f_{CLK} = 1MHz).

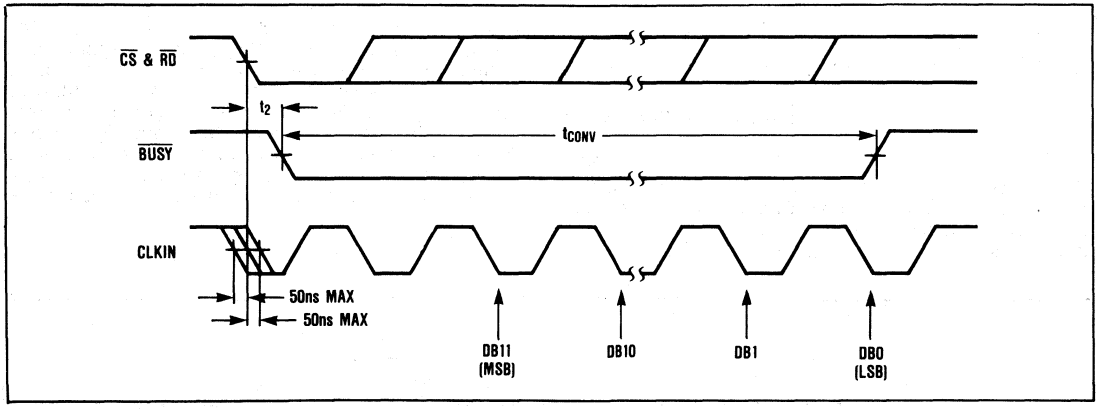


Figure 7. MAX162 $\overline{RD}$ and CLKIN For Synchronous Operation

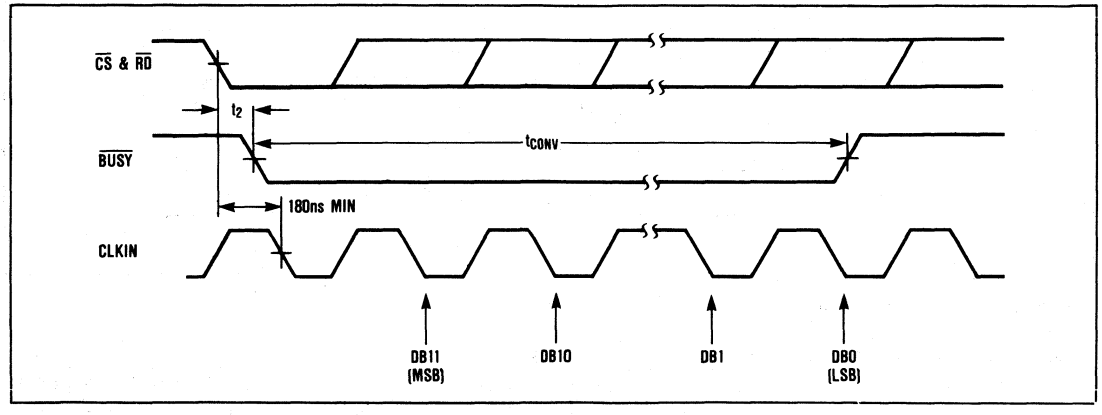


Figure 8. AD7572 $\overline{RD}$ and CLKIN For Synchronous Operation

Complete High-Speed CMOS 12-Bit ADC

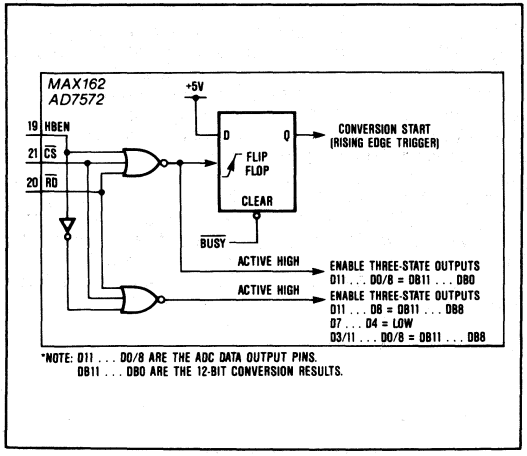


Figure 9. Logic Equivalent for $\overline{RD}$, $\overline{CS}$ and HBEN Inputs

Digital Interface

Output Data Format

The 12 output data bits can either be presented full parallel or in two 8 bit words. To obtain parallel output for 16 bit processors, HBEN should be kept low and the output data D11-D0 will be right justified.

For a two byte data read, outputs D7-D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented with the leading 4 bits being low for D7-D0/8.

Note that the 4 MSB's always appear at digital outputs D11-D8 whenever the digital drivers are enabled, regardless of the state of HBEN.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs; HBEN, CS and RD. Figure 9 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion. Once a conversion is in progress, it cannot be re-started. The BUSY output is low during the entire conversion cycle.

There are two modes of operation as outlined in the timing diagrams of Figures 10-13. Slow memory mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX162/AD7572 conversion time. ROM mode is for processors that cannot be forced into a wait state. In both operational modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation is required to access the conversion result.

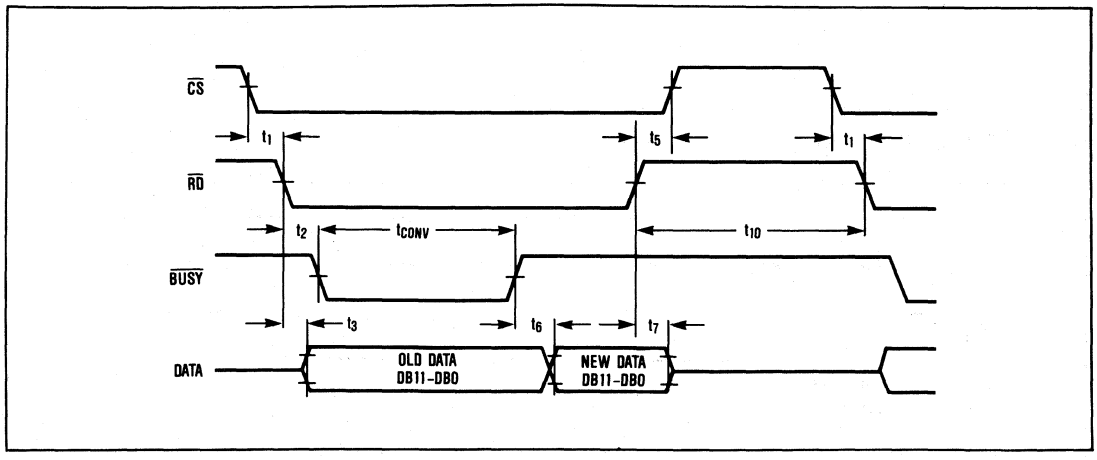


Figure 10. Slow Memory Mode, Parallel Read Timing Diagram

Table 1. Slow Memory Mode, Parallel Read Data Bus Status

MAX162/AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

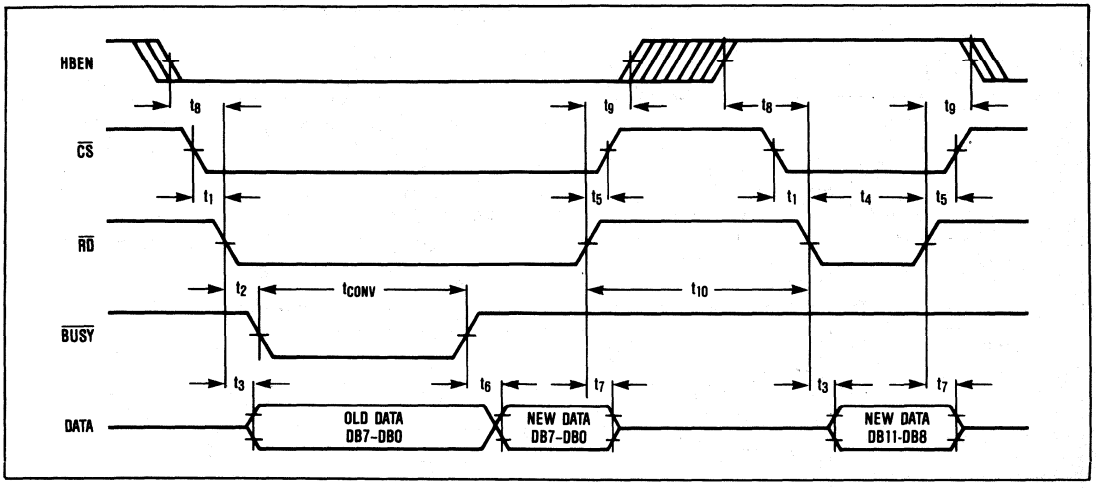


Figure 11. Slow Memory Mode, Two Byte Read Timing Diagram

Table 2. Slow Memory Mode, Two Byte Read Data Bus Status

MAX162/AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

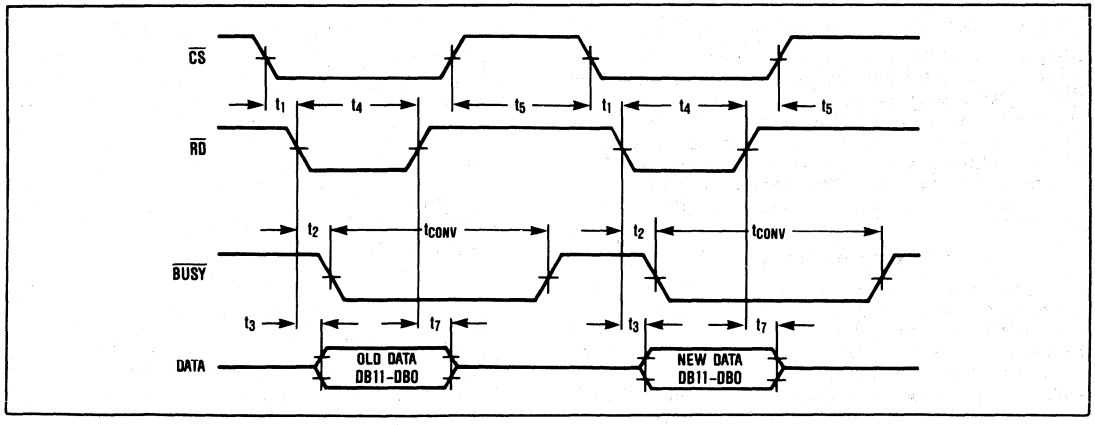


Figure 12. ROM Mode, Parallel Read Timing Diagram

Table 3. ROM Mode, Parallel Read Data Bus Status

MAX162/AD7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Complete High-Speed CMOS 12-Bit ADC

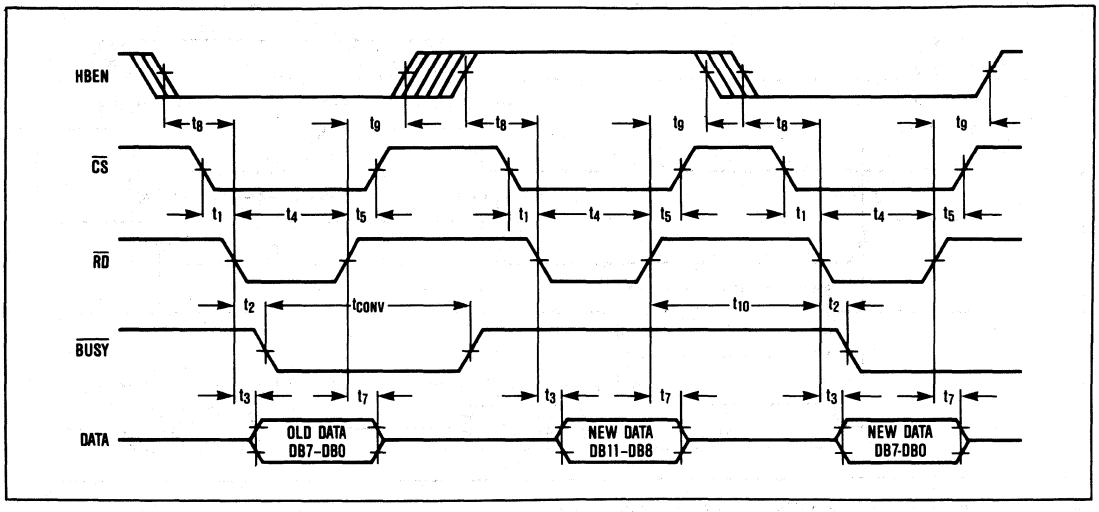


Figure 13. ROM Mode, Two Byte Read Timing Diagram

Table 4. ROM Mode, Two Byte Read Data Bus Status

MAX162/AD7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 10 and Table 1 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. CS and RD going low starts the conversion and BUSY goes low indicating that the conversion is in progress. Data from the previous conversion appears at the digital outputs. At the end of the conversion, BUSY returns high and the output latches are updated to place the digital conversion result on data outputs D11-D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only outputs D7-D0/8 are used. Starting the conversion and reading the 8 LSB's is identical to the Slow Memory Mode, Parallel Read. See Figure 11 and Table 2. A second READ operation with HBEN high places the 4 MSB's with 4 leading zeros on the data outputs D7-D0/8. The high byte read does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM mode avoids placing the processor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion appears at the data outputs D11-D0/8 (see Figure 12 and Table 3). This data may be disregarded if not needed. A second READ operation will access the results of the first operation and also start a new conversion. The delay between successive READ operations must be longer than the conversion time for the MAX162/AD7572.

ROM Mode, Two Byte Read

As in the Slow Memory Mode, only data outputs D7-D0/8 should be used for two byte reads. Figure 13 and Table 4 show the operation in this mode. A conversion is started with a READ operation with HBEN low. The data outputs present the 8 LSB's from the previous conversion and this data can be disregarded if not required. Two more READ operations are needed to access the conversion result. The first READ must be with HBEN high, where the 4 MSB's with 4 leading zero's are accessed. The second READ is with HBEN low, which reads in the 8 LSB's and starts a new conversion.

Interface Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, LSBs of error can be caused due to coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

ROM Mode

Considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a decision to keep or drop a bit. To avoid this problem, RD and CS should be active for less than one clock cycle. In other words, the RD and CS low pulse should be shorter than 250ns for the MAX162, 400ns for the AD7572XX05 and 1μs for the AD7572XX12. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN, since the comparator output is always latched at falling edges of CLKIN.

Analog Considerations

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX162/AD7572. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX162/AD7572 package.

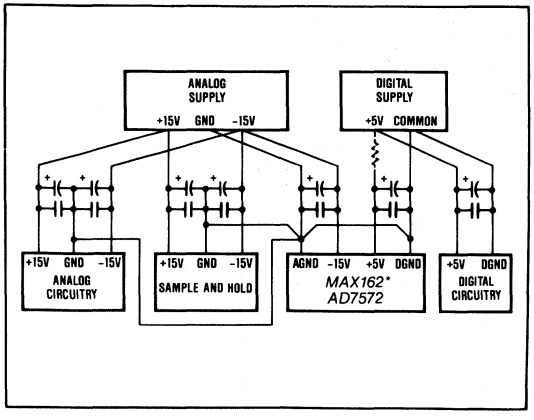


Figure 14. Power Supply Grounding Practice

Grounding

Figure 14 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 3 (AGND) of the MAX162/AD7572 separate from the logic ground. All other analog grounds and pin 12 (DGND) of the MAX162/AD7572 should be connected to this STAR ground and no other digital grounds should be connected to this STAR point. The ground return to the power supply from this STAR ground should be low impedance for noise free operation of the ADC.

Power Supply Bypassing

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1μF and 10μF by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10-20 ohms) resistor can be connected as shown in Figure 14 to filter external noise.

Internal Reference

The MAX162/AD7572 has an internal buried zener reference which provides the DAC reference voltage. The reference voltage is -5.25V ±1% and has a low temperature coefficient. The reference output is available at pin 2, and should be bypassed to analog ground (pin 3) with a 47μF tantalum capacitor in parallel with 0.1μF capacitor to minimize noise and provide low impedance at high frequencies. This by-pass capacitor must not be less than 4.7μF. The internal reference output buffer can sink upto 500μA.

Driving The Analog Input

The input signal leads to AGND and AIN should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion (4MHz for MAX162 and 2.5 or 1MHz for the AD7572). The output impedance of the driving amplifier is equal to its open loop output impedance divided by the loop gain at the frequency of interest.

AD7572 The AD7572 maximum clock rate of 2.5MHz makes it possible to drive it with amplifiers like the OP-42, AD711 or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

MAX162 The MAX162 with a maximum 4MHz clock rate might cause settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a OP-42, AD711 or OP-27 can be used to improve high frequency output impedance.

Complete High-Speed CMOS 12-Bit ADC

MAX162/AD7572 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX162. For higher bandwidth signals a sample-and-hold should be used.

The $\overline{BUSY}$ output from the MAX162/AD7572 may be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the $\overline{BUSY}$ signal goes low, the switching transients at the output of the sample-and-hold caused by the DAC switching may result in code dependent errors due to the aperture delay of the sample-and-hold. A NAND gate may be used to ensure that the sample-and-hold switches to the hold mode BEFORE any disturbances as shown in Figures 15 & 16. The NAND gate solution works only if the width of the $\overline{RD}$ pulse is wider than the $\overline{RD}$ to $\overline{BUSY}$ delay in the MAX162/AD7572. If this is not the case, use a flip flop which is set by the falling edge of $\overline{RD}$ and reset by the rising edge of $\overline{BUSY}$.

For synchronous $\overline{RD}$ and CLKIN as described above, the hold settling time allowed for the sample-and-hold is 500ns, 600ns and 1.5μs for the MAX162, AD7572XX05 and AD7572XX12 respectively.

To achieve the maximum sampling rate, the MAX162/AD7572 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

AD7572 Figure 15 shows an AD585 sample-and-hold to AD7572 interface. The AD7572 RD input and $\overline{BUSY}$ output are used to put the AD585 in hold mode when a conversion is in progress. In this example the analog input range is ±2.5V but other voltage ranges can be configured differently as explained later.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3μs sample-and-hold acquisition time.

Although this circuit works quite well for the 1MHz clock rate, at the 2.5MHz clock rate a faster sample-and-hold amplifier such as the HA-5320 is recommended.

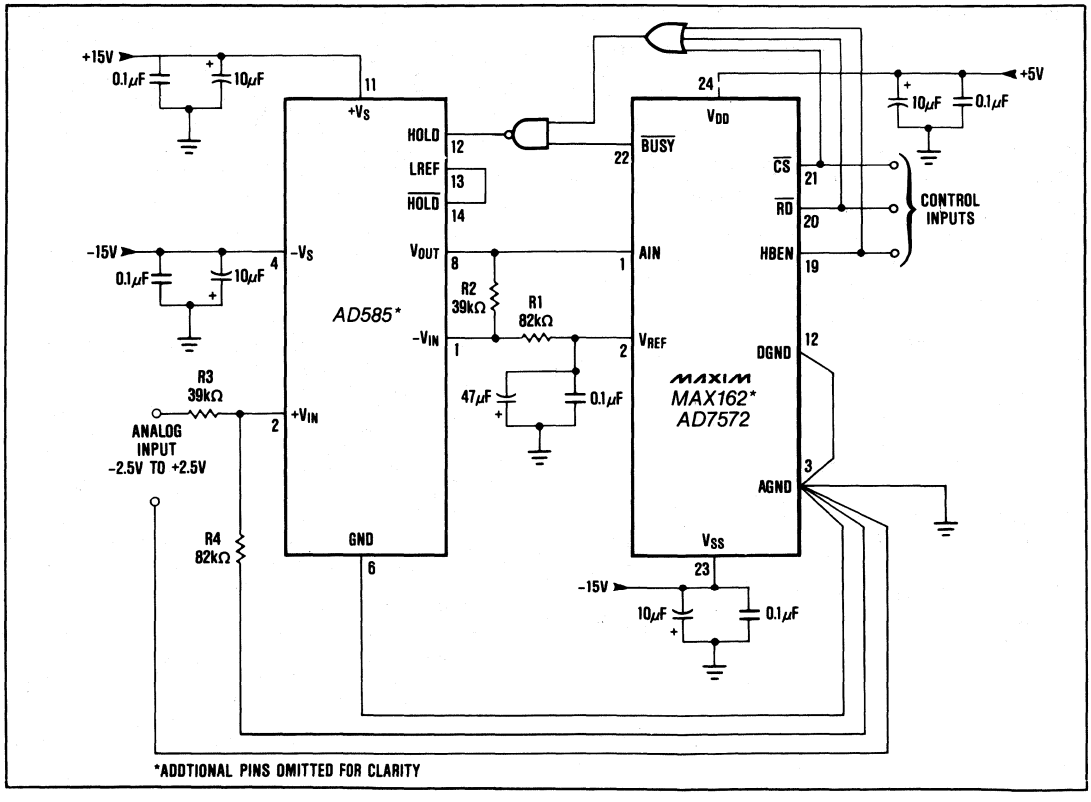


Figure 15. AD7572—AD585 Sample-and-Hold Interface

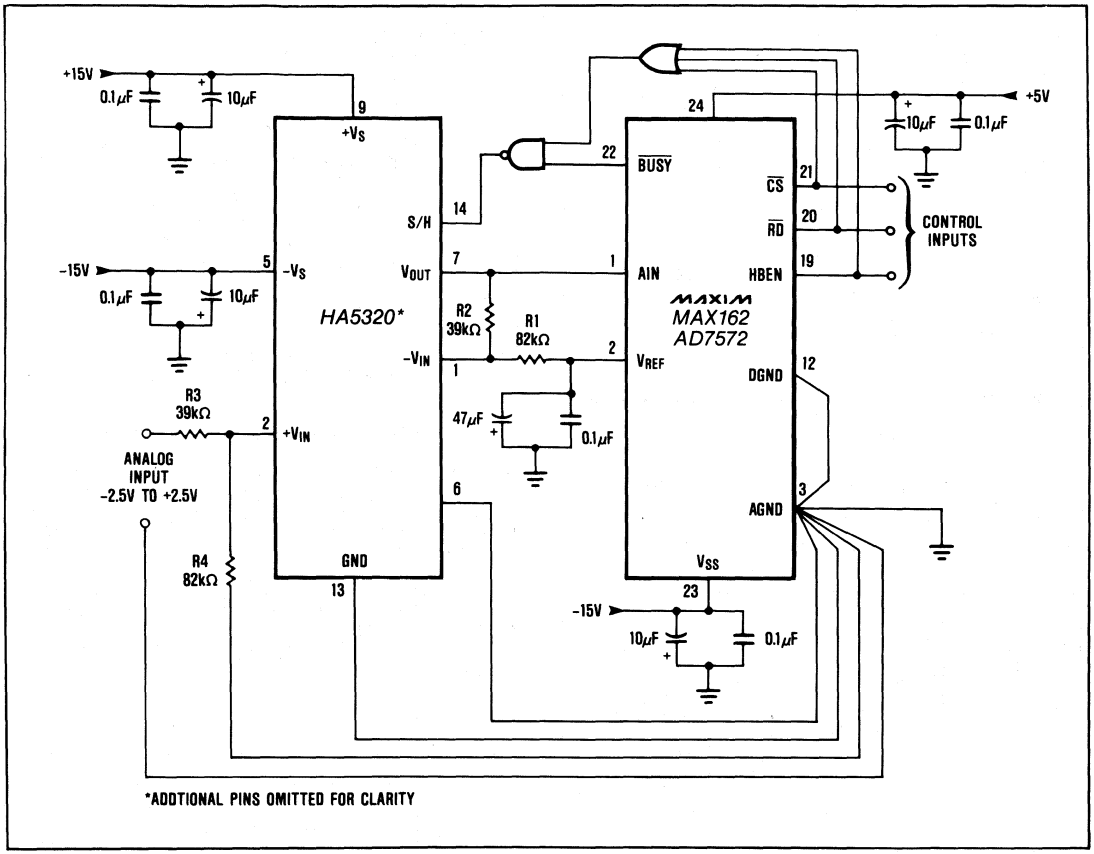


Figure 16. MAX162/AD7572—HA5320 Sample-and-Hold Interface

MAX162 Figure 16 shows the MAX162 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock which allows for a 1.5μs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Unipolar Input Operation

Figure 17 shows the nominal input/output transfer function of the MAX162/AD7572. Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 18. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS-3/2LSB (4.99817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 5 and 6.

Complete High-Speed CMOS 12-Bit ADC

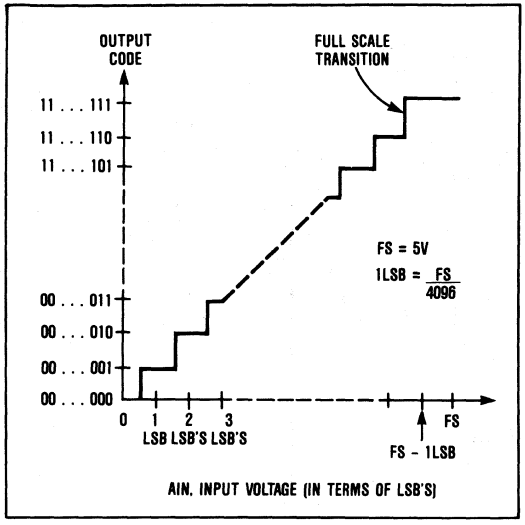


Figure 17. MAX162/AD7572 Transfer Function

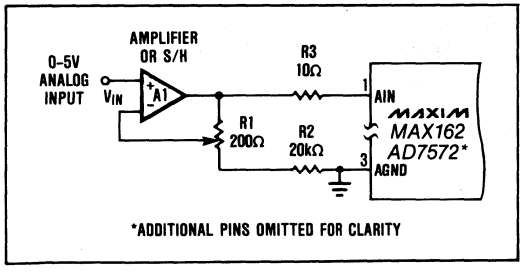


Figure 18. Full-Scale Adjustment

Figure 19 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 20 shows the ideal transfer function for this mode.

Figure 21 shows the bipolar operation in the inverting mode, where the output coding is complementary offset binary. Figure 20 shows the ideal transfer function for the circuit in Figure 21.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

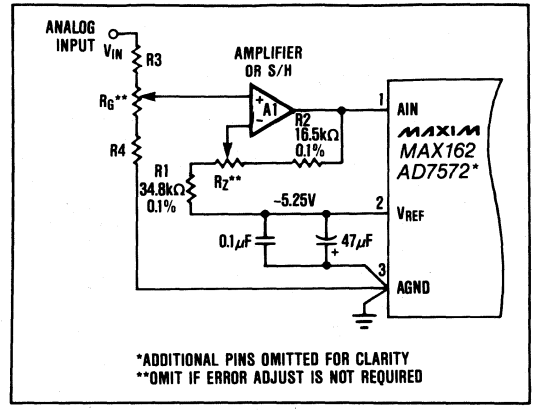


Figure 19. MAX162/AD7572 Non-inverting Bipolar Operation

Table 5. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 19

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

Notes:
* R3 and R4 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

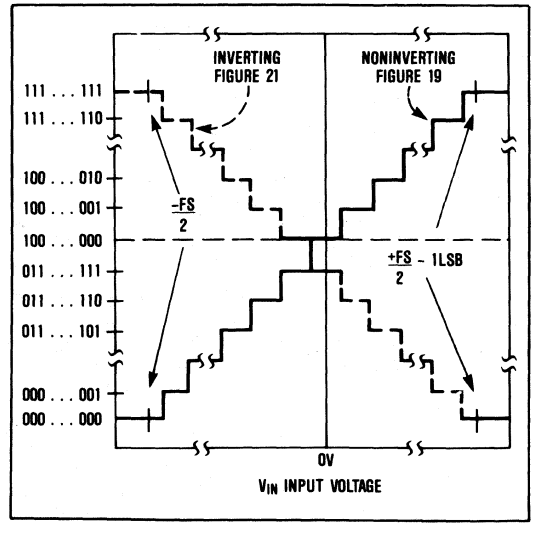


Figure 20. Ideal Input/Output Transfer Characteristic for the Bipolar circuits in Figures 19 and 21.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see tables 5 and 6) and adjust R_Z until the output code flickers between the following codes:

For Non-inverting (Figure 19) 1000 0000 0000
1000 0000 0001

For inverting (Figure 21) 0111 1111 1111
0111 1111 1110

Apply FS-3/2LSB (see tables 5 and 6) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 19) 1111 1111 1110
1111 1111 1111

For inverting (Figure 21) 0000 0000 0001
0000 0000 0000

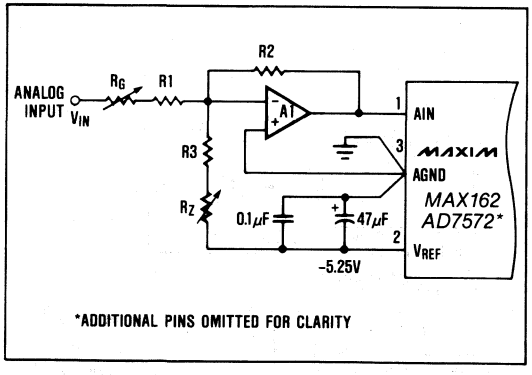


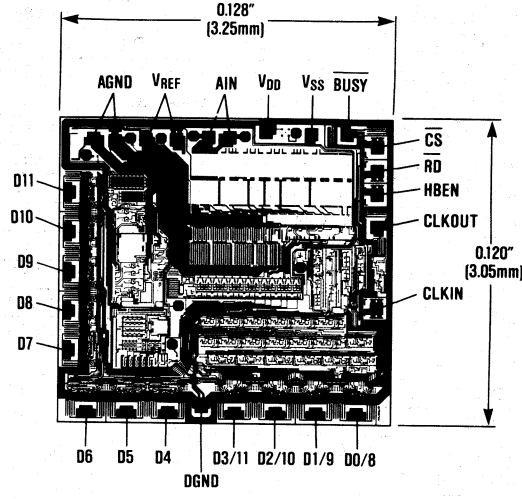
Figure 21. MAX162/AD7572 Inverting Bipolar Operation

Table 6. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 21

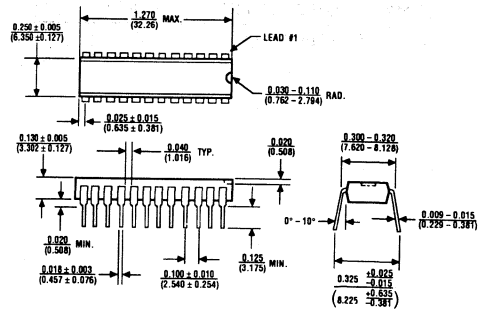
V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

Notes:
* R1, R2, and R3 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

Chip Topography



Package Information



24 Lead Plastic Narrow DIP (NG)
θ_{JA} = 120°C/W
θ_{JC} = 60°C/W

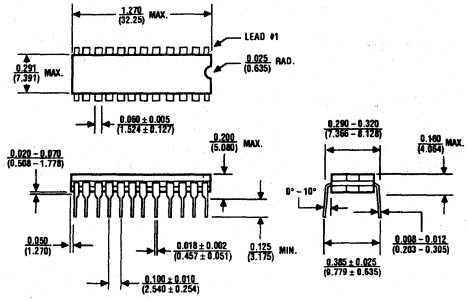
Complete High-Speed CMOS 12-Bit ADC

Ordering Information (continued)

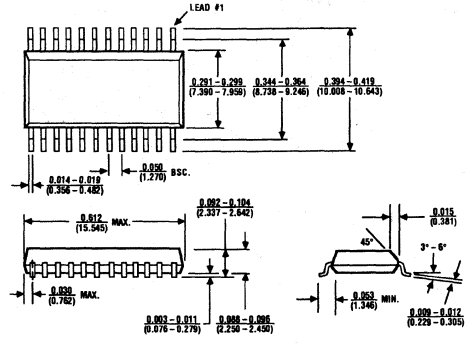
PART	TEMP. RANGE	PACKAGE*	ERROR
5μs CONVERSION TIME			
AD7572JN05	0°C to +70°C	Plastic DIP	±1 LSB
AD7572KN05	0°C to +70°C	Plastic DIP	±1 LSB
AD7572LN05	0°C to +70°C	Plastic DIP	±½ LSB
AD7572JCWG05	0°C to +70°C	Wide S.O.	±1 LSB
AD7572KCWG05	0°C to +70°C	Wide S.O.	±1 LSB
AD7572LCWG05	0°C to +70°C	Wide S.O.	±½ LSB
AD7572AQ05	-25°C to +85°C	CERDIP	±1 LSB
AD7572BQ05	-25°C to +85°C	CERDIP	±1 LSB
AD7572CQ05	-25°C to +85°C	CERDIP	±½ LSB
AD7572SQ05	-55°C to +125°C	CERDIP	±1 LSB
AD7572TQ05	-55°C to +125°C	CERDIP	±1 LSB
AD7572UQ05	-55°C to +125°C	CERDIP	±½ LSB
12μs CONVERSION TIME			
AD7572JN12	0°C to +70°C	Plastic DIP	±1 LSB
AD7572KN12	0°C to +70°C	Plastic DIP	±1 LSB
AD7572LN12	0°C to +70°C	Plastic DIP	±½ LSB
AD7572JCWG12	0°C to +70°C	Wide S.O.	±1 LSB
AD7572KCWG12	0°C to +70°C	Wide S.O.	±1 LSB
AD7572LCWG12	0°C to +70°C	Wide S.O.	±½ LSB
AD7572AQ12	-25°C to +85°C	CERDIP	±1 LSB
AD7572BQ12	-25°C to +85°C	CERDIP	±1 LSB
AD7572CQ12	-25°C to +85°C	CERDIP	±½ LSB
AD7572SQ12	-55°C to +125°C	CERDIP	±1 LSB
AD7572TQ12	-55°C to +125°C	CERDIP	±1 LSB
AD7572UQ12	-55°C to +125°C	CERDIP	±½ LSB

** All devices — 24 lead packages*

Package Information (continued)



24 Lead Narrow CERDIP (RG)
θ_{JA} = 80°C/W
θ_{JC} = 40°C/W



24 Lead Small Outline, Wide (WG)
θ_{JA} = 85°C/W
θ_{JC} = 45° C/W

MAXIM

Complete 10μs CMOS 12-Bit ADC

General Description

The MAX172 is a complete 12-Bit analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 10μs. The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX172 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

- **12-Bit Resolution and Linearity**
- **10μs Conversion Time**
- **No Missing Codes**
- **On-Chip Voltage Reference**
- **90ns Access Time**
- **215mW Max Power Consumption**
- **24-Lead Narrow DIP Package**
- **Pin-for-Pin AD7572 Replacement**

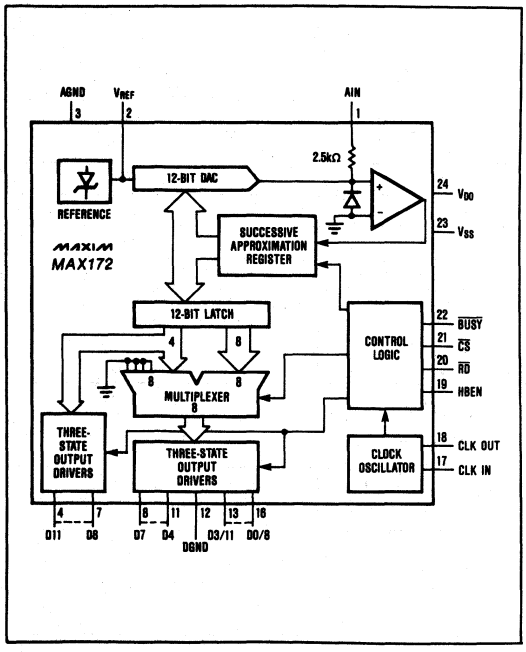
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX172ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX172BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX172ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX172BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX172CC/D	0°C to +70°C	Dice**	±1 LSB
MAX172AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX172BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX172AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX172BMRG	-55°C to +125°C	CERDIP	±1 LSB

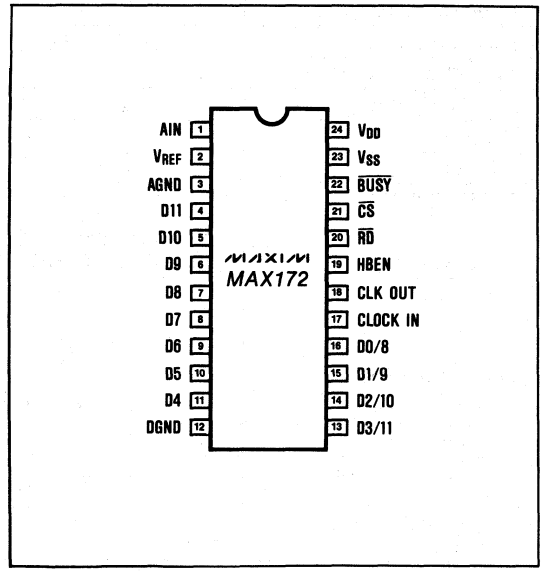
* *All devices — 24 lead packages*

** *Consult factory for dice specifications*

Functional Diagram



Pin Configuration



Complete 10μs CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX172XC ..... 0°C to +70°C
MAX172XI ..... -25°C to +85°C
MAX172XM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX172A MAX172B				±1/2 ±1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Offset Error (Note 1)		MAX172B	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±8	LSB
		MAX172A	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
Full Scale Error (Note 2)		MAX172B	T_A = 25°C			±15	LSB
		MAX172A	T_A = 25°C			±10	
Full Scale Tempco (Notes 3, 4)						±45	ppm/°C
ANALOG INPUT							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)					40		ppm/°C
Output Current Sink Capability		(Note 6)				500	μA
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	μA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200μA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	μA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION TIME						
MAX172	t_{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	9.6		10 10.4	μs
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V		±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V, V_{SS} = -5% to +5%		±1/8		LSB
POWER REQUIREMENTS						
V_{DD}		±5% for Specified Performance		5		V
V_{SS} (Note 8)		±5% for Specified Performance		-12 or -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1 LSB.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB.
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: Functional operation at V_{SS} = -12V ± 5% is guaranteed by testing offset error and full scale error.

TIMING CHARACTERISTICS (Note 9)

(V_{DD} = +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

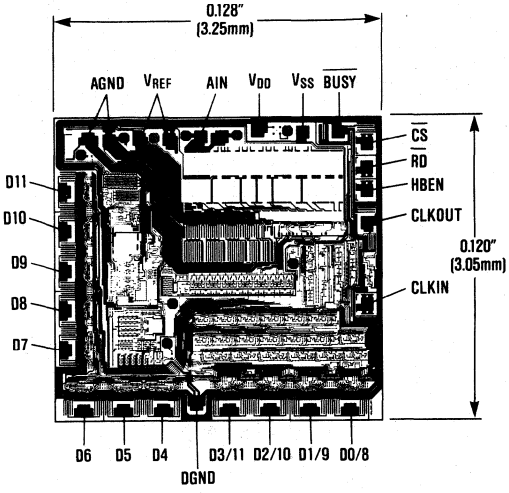
PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX172C/I		MAX172M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

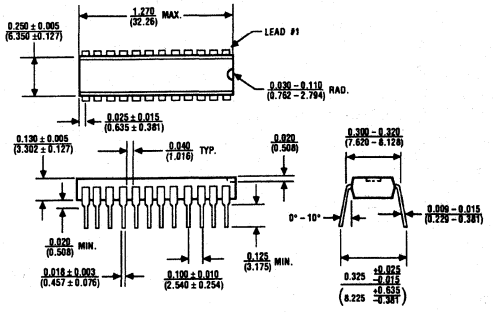
For additional information on using the MAX172 please refer to MAX162 data sheet.

Complete 10μs CMOS 12-Bit ADC

Chip Topography

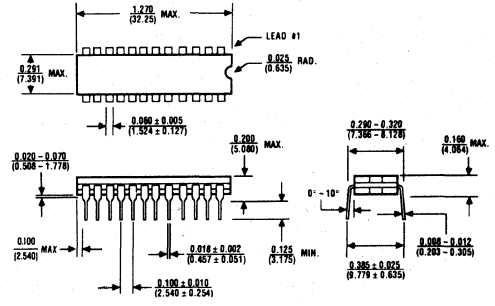


Package Information



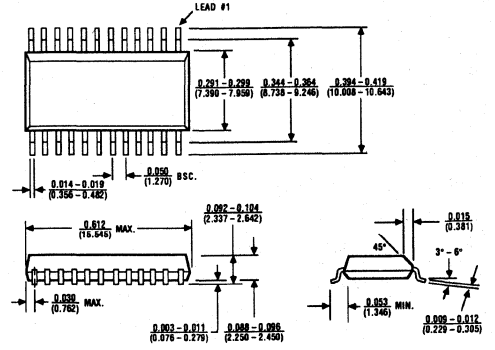
24 Lead Plastic Narrow DIP (NG)

θ_{JA} = 120°C/W
θ_{JC} = 60°C/W



24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W
θ_{JC} = 40°C/W



24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W
θ_{JC} = 45° C/W

MAXIM

High Speed 12 Bit A/D Converter

General Description

The AD578 is a 12-bit successive approximation analog-to-digital converter complete with internal clock and reference. The combination of bipolar and CMOS technology optimizes accuracy, speed, and power in a convenient 32 pin ceramic DIP. Maximum conversion time is 3μS (L version) however the device may be operated at faster speeds with reduced resolution by short cycling.

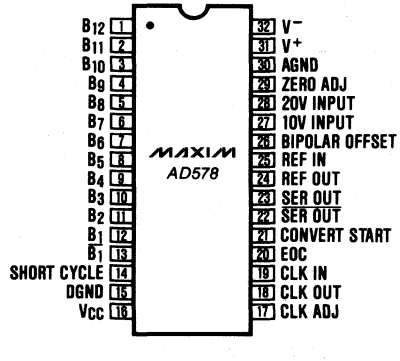
Multiple input ranges are accommodated in both unipolar and bipolar modes using internal resistors. These resistors also track those in the reference for low gain drift with temperature. All data bits are available in both parallel and serial form using either the internal or an external clock.

Applications

High Speed Data Acquisition Systems
Transient Recorders
Multichannel Data Loggers
Digital Signal Processing

Pin Configuration

Top View



Features

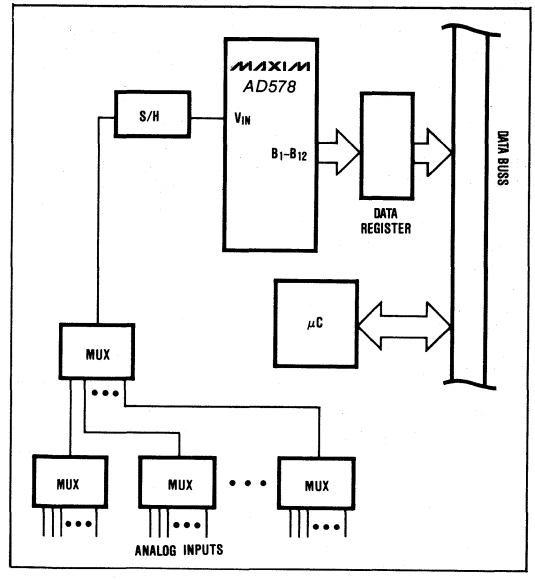
- Pin-for-Pin Second Source
- Fast Conversion: 3μs (AD578L)
- Internal +10V Reference
- Low Gain TC: 30ppm/°C Max
- Linearity Error: 0.012% Max
- No Missing Codes Over Temperature
- Parallel and Serial Outputs
- Adjustable Internal Clock
- Short Cycle Capability

Ordering Information

PART	TEMP. RANGE	PACKAGE
AD578JN	0°C to +70°C	32 Lead Ceramic DIP
AD578KN	0°C to +70°C	32 Lead Ceramic DIP
AD578LN	0°C to +70°C	32 Lead Ceramic DIP
AD578SN	-55°C to +125°C	32 Lead Ceramic DIP
AD578TN	-55°C to +125°C	32 Lead Ceramic DIP

For ±12V Supplies, Order AD578ZXX
(For Hermetic Seal (D) Please Contact Factory.)

Typical Operating Circuit



High Speed 12 Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, V^+ (pin 31 to GND) ..... +18V
Negative Supply Voltage, V^- (pin 32 to GND) ..... -18V
Digital Supply Voltage, V_{CC} (pin 16 to GND) ..... +7V
Digital Input Voltage
(pins 14, 17, 19, 21) ..... GND - 0.5V ≤ V_{IN} ≤ V_{CC} + 0.5V
Analog GND to Digital GND ..... ±0.5V

Analog Inputs (pins 25, 26, 27) ..... ±12V
(pins 28, 29) ..... ±24V
Ref Out ..... Indefinite Short to AGND
Momentary Short to V^+
Power Dissipation ..... 2W @ 100°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = -15V, V_{CC} = +5V, T_A = +25°C, unless noted—Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset (Note 1)	Unipolar, T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±3	±10	ppm/°C
	AD578S		±3	±15	ppm/°C
	Bipolar (Note 1, 2), T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±8	±20	ppm/°C
	AD578S		±8	±25	ppm/°C
Gain Error (Note 1, 3)	T_A = 25°C		±0.1	±0.25	%FSR
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J,T		±15	±30	ppm/°C
	AD578S		±15	±50	ppm/°C
Linearity	T_A = 25°C			½	LSB
	$T_{MIN} \le T_A \le T_{MAX}$; AD578L,K,J		¾		
	AD578S,T			¾	
Differential Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$		no missing codes		
Differential Linearity Drift	$T_{MIN} \le T_A \le T_{MAX}$		±2		ppm/°C
Reference Voltage Accuracy	$V_{nominal}$ = 10.000V		±10	±100	mV
Reference Voltage Drift	$T_{MIN} \le T_A \le T_{MAX}$		±10	±30	ppm/°C
Reference Output Current		±1			mA
Power Supply Rejection Ratio (Note 5)	V^+ = +13.5 to +16.5V			0.005	%/%ΔV
	V^- = -13.5 to -16.5V			0.005	
	V_{CC} = +4.5 to +5.5V			0.005	
Conversion Speed	AD578L	3.0			µs
	AD578K,T	4.5			
	AD578J,S	6.0			
Input Impedance	0V to +10V range		5		kΩ
	0V to +20V range		10		
	-5V to +5V range		5		
	-10V to +10V range		10		
Power Supply Range (Note 5)	V^+	13.5		16.5	V
	V^-	-13.5		-16.5	
	V_{CC}	4.75		5.25	
Power Supply Current	V^+		11	15	mA
	V^-		21	35	
	V_{CC}		45	80	
Power Dissipation			0.7	1.15	W
Operating Temperature Range	AD578L,K,J	0		+70	°C
	AD578S,T	-55		+125	
Logic Output Drive	B_1-B_{12}, $\overline{B_1}$, CLOCK OUT		2		LS TTL Loads
	SER OUT, SER OUT		2		
	EOC		8		
Logic Input Load	CLOCK IN, CONVERT START		1		
Parallel Output Code	Unipolar	Binary			
	Bipolar	Offset Binary/Two's Complement			
Serial Output Code	Unipolar	Binary/Complementary Binary			
	Bipolar	Offset Binary/Complementary Offset Binary			

Note 1: Adjustable to zero.
Note 2: 50Ω, 1% resistor between pins 24 and 26.
Note 3: 50Ω, 1% resistor between pins 24 and 25.
Note 4: AD578ZXX models, V^+ = +12V, V^- + -12V
Note 5: 'Z' models, V+ = 11.6V to 12.6V,
V^- = -11.6V to -12.6V

High Speed 12 Bit A/D Converter

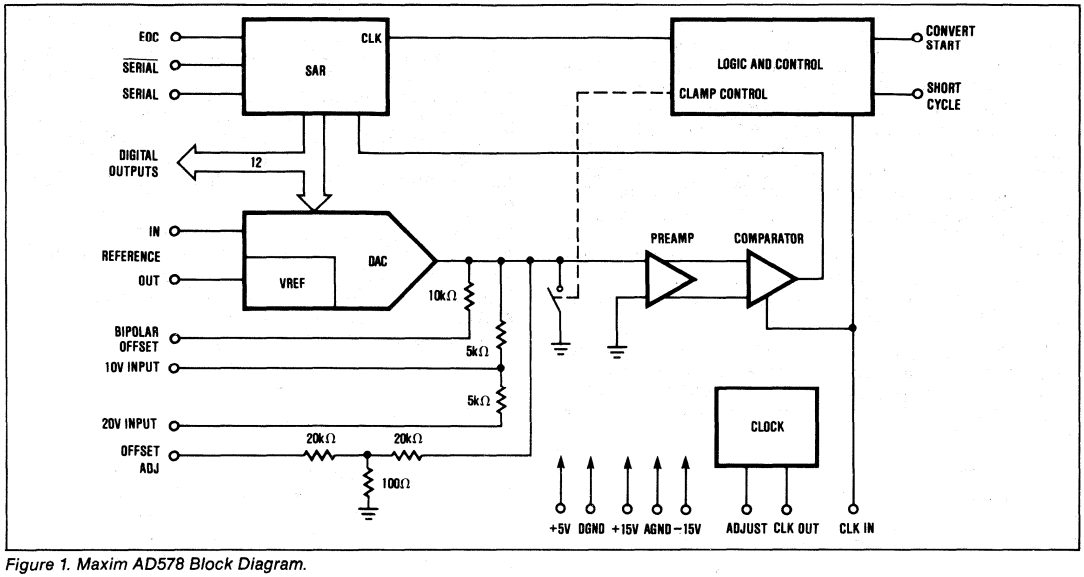


Figure 1. Maxim AD578 Block Diagram.

Detailed Description

The AD578 is a 12-bit successive approximation A/D converter in which the analog input is compared to the output of a high speed D/A converter (Figure 1). The D/A is binarily stepped until its output matches the analog input. The digital code from the successive approximation register (SAR) appears on the outputs as the binary value of the input voltage. The conversion processs consists of twelve successive tests, starting with the D/A set to half Full Scale (FS). The comparator determines whether the D/A output is higher or lower than the analog input and either sets or resets Bit 1 (MSB). On the next test, the D/A is incremented up or down ¼ FS, based on the last decision, and is again compared to the input. The result is stored as BIT 2. Each comparator decision is clocked into the SAR for the remaining bits until all twelve have been tested.

A positive going pulse on Convert Start resets the D/A Converter to ½ FS and sets the End-Of-Convert (EOC) high indicating that a conversion is in progress (Figure 7). The internal clock is enabled and the conversion begins on the trailing edge of the Start Convert (S) pulse. After the last bit has been tested, EOC goes LOW indicating that the output data is valid.

Calibration Procedure

For a large number of AD578 applications no user calibration is needed. The performance limits for an uncalibrated device are given in the Electrical Characteristics section. If more precision is required then offset and gain adjustments can be made as follows.

Table 1. Calibration Chart

	ANALOG INPUT VOLTAGE				OUTPUT CODE(1)	
	0 TO +10V	0 TO +20V	-5 TO +5V	-10 TO +10V	MSB	LSB
+FS -1LSB	+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1	1 1 1 1 1 1 1 1
+FS -1½LSB	+9.9964	+19.9927	+4.9964	+9.9927	1 1 1 1	1 1 1 1 1 1 1@
Mid Scale +½LSB	+5.0012	+10.0024	+0.0012	+0.0024	1 0 0 0	0 0 0 0 0 0 0@
Mid Scale	+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0	0 0 0 0 0 0 0 0
-FS +½LSB	+0.0012	+0.0024	-4.9988	-9.9976	0 0 0 0	0 0 0 0 0 0 0@
-FS	+0.0000	+0.0000	-5.0000	-10.0000	0 0 0 0	0 0 0 0 0 0 0 0

Note 1: The symbol "@" indicates a 0 or 1 with equal probability.

High Speed 12 Bit A/D Converter

Keeping in mind that the offset must always be adjusted before the gain, set the system into a mode of continuous conversions with a high repetition rate (>1kHz) while monitoring the output data lines using an oscilloscope, logic analyzer triggered on EOC, or LED's driven by latched data outputs clocked by EOC. Using a DVM, set the input voltage ½ LSB above -Full Scale (-FS) for the appropriate range (Table 1). Adjust the offset potentiometer (Figure 2) so that the LSB (B_{12}) alternates between a "0" and "1" with a 50% duty cycle with all the other bits OFF. Using LED's, the LSB will appear at half intensity. The gain is similarly set by applying a voltage of +FS -1½LSB (Table 1) and adjusting the LSB for the same 50% ON condition with the exception that all the other bits are ON.

In bipolar mode, it is often desired to calibrate the bipolar zero condition at mid scale rather than the -FS offset. In this case set the input to MID SCALE +½LSB and adjust the LSB for 50% duty cycle with all bits off except B_1 (MSB).

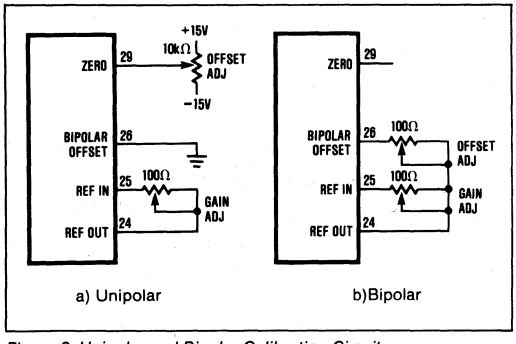


Figure 2. Unipolar and Bipolar Calibration Circuit.

Clock Adjust

The internal clock on all grades is set for a nominal 5.8μs with tolerance of about +0.2μs with no external components connected to pin 17. To obtain 3.0μs for the L grade, connect an 825Ω resistor as shown in Figure 5(a). For K and T grades, use a 3.3kΩ resistor for 4.5μs. For J and S grades, it is recommended that no adjustment be made unless exactly 6.0μs is required.

For faster conversion speeds, connect a resistor chosen from Figure 3 between pins 17 and 18. For slower conversions, connect a capacitor, Figure 4, from pin 17 to GND. A combination of both resistor and capacitor maybe used particularly for fine adjustment of slow clock settings (Figure 5).

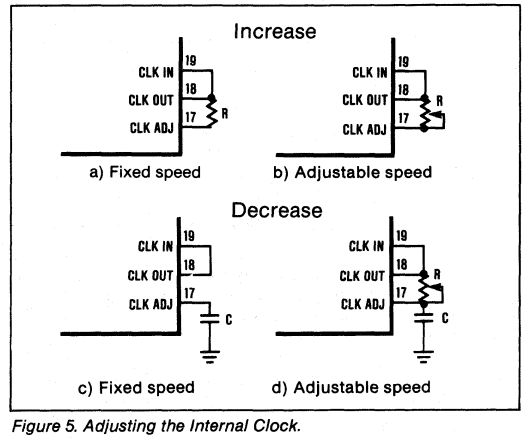


Figure 5. Adjusting the Internal Clock.

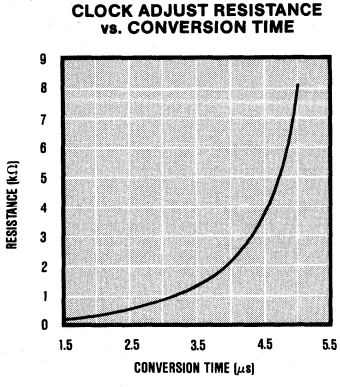


Figure 3. Speed vs. Resistance.

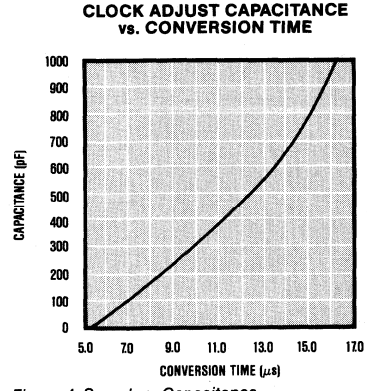


Figure 4. Speed vs. Capacitance.

High Speed 12 Bit A/D Converter

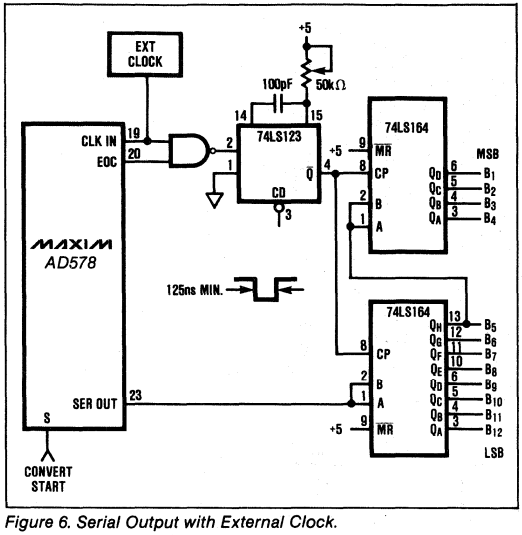
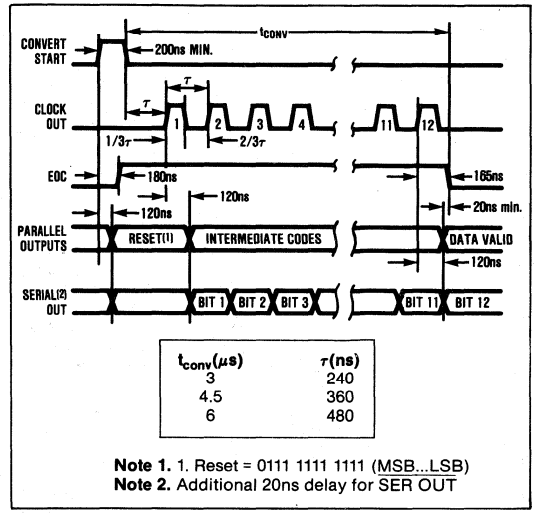


Figure 6. Serial Output with External Clock.



t_{conv}(μs)	τ(ns)
3	240
4.5	360
6	480

Note 1. 1. Reset = 0111 1111 1111 (MSB...LSB)
Note 2. Additional 20ns delay for SER OUT

Figure 7. Timing Diagram.

Short Cycle

For conversions of less than 12 bits, SHORT CYCLE, pin 14, must be connected to the next higher bit than the desired resolution. For example, connecting pin 14 to pin 2 will result in 10 bit conversions. When using an external clock, EOC must also be used to inhibit the CLK IN.

External Clock

The external clock can be used for synchronous applications, such as clocking the serial output data into a serial-to-parallel shift register (Figure 6). The clock should have a duty cycle between 30% and 70%. The main advantage of serial transmission is the reduction in the number of output lines from 12 to 1, which is particularly useful when using optical couplers or sending data over long distances.

Application Hints

Layout

The Analog and Digital Grounds should be directly connected together as close as possible to the package and then tied to a quiet analog ground with no switching transients taking place during the conversion. A ground plane works best, but is not necessary if large traces are used. It is advisable to filter the supplies with 10μF electrolytic capacitors on the PC board along with 0.1μF bypassing capacitors as close to the supply pins on the AD578 as possible. Above all, separate the analog circuit connections, pins 24 through 32, away from the digital section. If a digital signal must cross an analog connection, make sure it crosses at a ninety degree angle on different sides of the board if at all possible.

If using only the 20V input range, leave the 10V input (pin 27) completely unconnected since capacitance on this high impedance point can degrade dynamic performance. When relays or switches are used, mount them as close to the input pins as possible.

Although not necessary to achieve rated specifications, it is recommended that a 10μF electrolytic capacitor be connected on REF OUT to GND for improved noise on the code transitions.

Interfacing

The digital outputs of the AD578 should be latched since they are constantly changing during the conversion. Edge triggered, rather than transparent latches are preferred, such as the 74LS574 (Figure 8), to prevent changing data lines feeding back into the analog portions of the A/D converter. Capacitive loading above 30pF as well as connections more than a few inches long should be avoided on the digital outputs of the A/D.

Input Signal Conditioning

The analog input should be driven by a wide bandwidth, low output impedance op amp or a fast sample-hold. Although V_{IN} may not change during the conversion, the load current of the A/D abruptly changes with each clock cycle due to successive DAC codes (Figure 1). The amplifier must recover to the original value in time for the rest of the circuit to settle before the comparator can make a decision. An op amp which can settle to 0.01% in 50 to 100ns for a 0.5mA change in load current with no thermal tail and low offset voltage drift is recommended.

High Speed 12 Bit A/D Converter

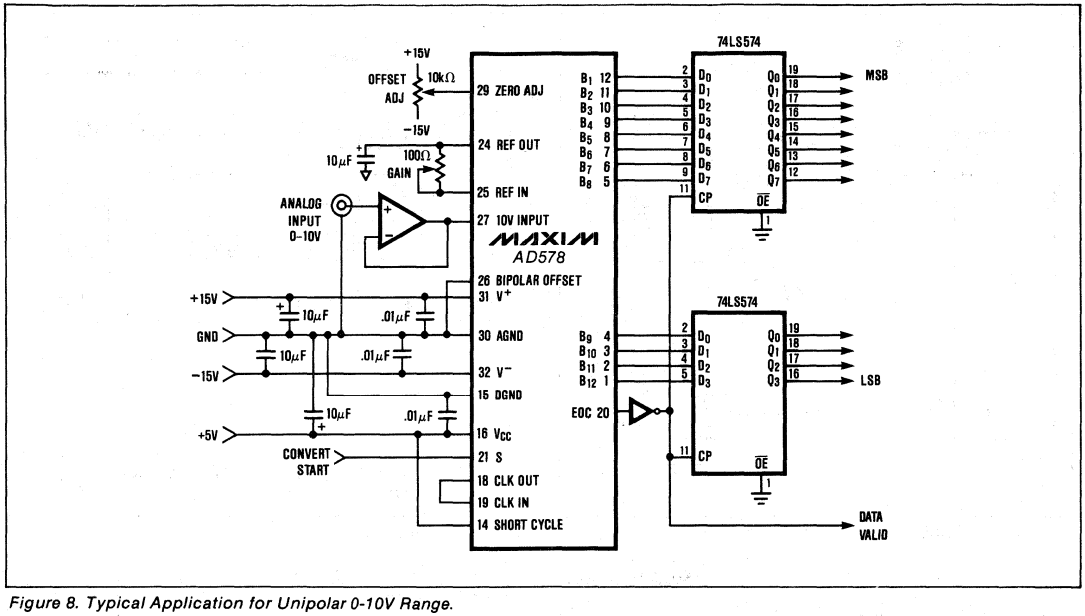
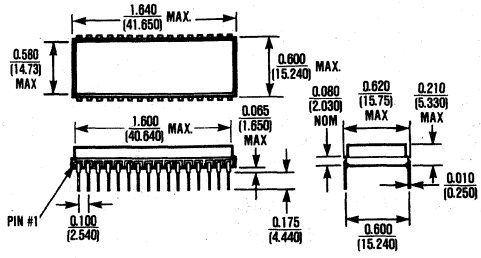


Figure 8. Typical Application for Unipolar 0-10V Range.

Package Information



32 Lead Ceramic Sidebraze

θ_{JA} = 7°C/W

θ_{JC} = 30°C/W

CMOS High Speed A/D Converter with Track/Hold Function

General Description

The ADC0820 is a high speed, microprocessor compatible, 8 bit analog-to-digital converter which uses a half-flash technique to achieve a conversion time of 1.4 μs. The converter has a 0V to +5V analog input range and uses a single +5V supply.

A built-in track-and-hold function is included, eliminating the need for an external track-and-hold for input slew rates up to 100mV/μs.

The A/D easily interfaces with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. Data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system I/O port. An over-flow output is also provided for cascading devices to achieve higher resolution.

Maxim's ADC0820 is pin-compatible with National Semiconductor's ADC0820 and provides improved specifications. It is packaged in 20-pin DIP and Small Outline packages.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Loops
Audio Systems

Features

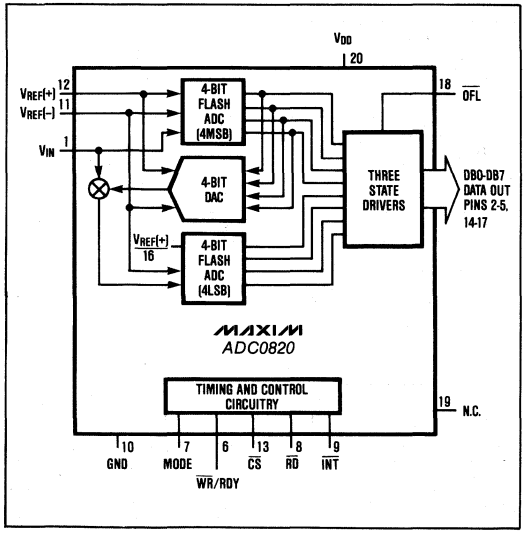
- **Fast Conversion Time: 1.4μs Max.**
- **Built-in Track-and-Hold Function**
- **No Missing Codes**
- **No User Adjustments Required**
- **Single +5V Supply**
- **No External Clock**
- **Easy Interface To Microprocessors**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
ADC0820BCN	0° C to +70° C	Plastic	±½ LSB
ADC0820CCN	0° C to +70° C	Plastic	±1 LSB
ADC0820CC/D	0° C to +70° C	Dice	±1 LSB
ADC0820CCM	0° C to +70° C	Small Outline	±1 LSB
ADC0820BCJ	-40° C to +85° C	CERDIP	±½ LSB
ADC0820CCJ	-40° C to +85° C	CERDIP	±1 LSB
ADC0820BJ	-55° C to +125° C	CERDIP	±½ LSB
ADC0820CJ	-55° C to +125° C	CERDIP	±1 LSB

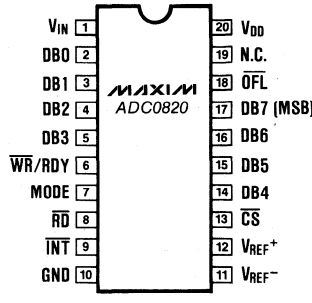
** All devices — 20 lead packages.*

Functional Block Diagram



Pin Configuration

Top View



CMOS High Speed A/D Converter with Track/Hold Function

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins
(Pins 1-9, 11-19) ..... GND - 0.3V, V_{DD} +0.3V
Output current (Pin 19) 30mA
Power Dissipation (Any Package) to +75°C 450mW
Derate Above +25°C by ..... 6mW/°C

Operating Temperature Ranges
ADC0820CCN/BCN/CCM ..... 0°C to +70°C
ADC0820BCJ/CCJ ..... -40°C to +85°C
ADC08020BJ/CJ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		ADC0820B ADC0820C			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
REFERENCE INPUT						
Reference Resistance		T_A = +25°C T_A = T_{MIN} to T_{MAX}	1.4 1.25	2.2	4.0 4.0	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD} + 0.1	V
V_{REF}^- Input Voltage Range			GND - 0.1		V_{REF}^+	V
ANALOG INPUT						
Analog Input Voltage Range	V_{INR}		GND - 0.1		V_{DD} + 0.1	V
Analog Input Capacitance	C_{VIN}			45		pF
Analog Input Current	I_{VIN}	V_{IN} = 0V to +5V; T_A = +25°C, T_{MIN} to T_{MAX}			±0.3 ±3	μA
Slew Rate, Tracking (Note 2)	SR			0.2	0.1	V/μs
LOGIC INPUTS						
Input HIGH Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE	2.0 3.5			V
Input LOW Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$ MODE			0.8 1.5	V
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$; T_A = +25°C, T_{MIN} to T_{MAX}			0.1 1	μA
		$\overline{WR}$; T_A = +25°C, T_{MIN} to T_{MAX}			0.3 3	
		MODE; T_A = +25°C, T_{MIN} to T_{MAX}		50	150 200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE; T_A = 25°C, T_{MIN} to T_{MAX}			-0.3 -1	μA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, MODE		5	8	pF
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$ V_{DD} = +4.75V, I_{OUT} = -360μA V_{DD} = +4.75V, I_{OUT} = -10μA	4.0 4.5			V
Output LOW Voltage	V_{OL}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY V_{DD} = +4.75V, I_{OUT} = 1.6mA			0.4	V
Three-state Output Current		DB0-DB7, RDY; T_A = +25°C, T_{MIN} to T_{MAX}	-0.3 -3		+0.3 +3	μA
Output Capacitance (Note 3)	C_{OUT}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		5	8	pF
Output Source Current	I_{SRC}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0		-25	-10	mA
Output Sink Current	I_{SINK}	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = V_{DD}		40	15	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, RD-MODE, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY						
Supply Voltage	V_{DD}	±5% for Specified Performance		5		V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0 T_A = +25°C T_{MIN} to T_{MAX}		5	10 15	mA
Power Dissipation		$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = 0		25		mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. See Note 2, 4.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			ADC0820BCX ADC0820CCX		ADC0820BJ ADC0820CJ		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 3kΩ		35	70		90		100	ns
Conversion Time (RD Mode)	t_{CRD}	(Note 7)		1.2	1.6		2.0		2.5	μs
Data Access Time (RD Mode) (See Figure 1)	t_{ACC0}	(Note 5)		t_{CRD} + 10	t_{CRD} + 35		t_{CRD} + 50		t_{CRD} + 70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		60	125		175		225	ns
Data Hold Time	t_{DH}	(Note 6)		40	90		120		150	ns
Delay Time Between Conversions	t_P		500			600		600		ns
Write Pulse Width	t_{WR}		600		50,000	600	50,000	600	50,000	ns
Conversion Time (WR-RD Mode)	t_{CWR-RD}		1.4			1.56		1.62		μs
Delay between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		600			700		700		ns
Data Access Time (WR-RD Mode) (See Figure 3)	t_{ACC1}	t_{RD} < t_{INTL}		110	220		280		350	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}			100	200		260		320	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}			600	1000		1400		1700	ns
Data Access Time (WR-RD Mode) (See Figure 2)	t_{ACC2}	t_{RD} > t_{INTL}, (Note 6)		60	100		130		160	ns
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t_{IHWR}	C_L = 50pF		70	100		130		150	ns
Data Access Time After $\overline{INT}$	t_{ID}			10	50		65		75	ns

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Sample tested at +25°C by Quality Assurance to ensure compliance.
Note 3: Guaranteed by design.
Note 4: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 5: Defined as the time required for an output to cross 0.8V or 2.4 V.
Note 6: Defined as the time required for the data lines to change 0.5V.
Note 7: For faster conversions use WR-RD Mode.

CMOS High Speed A/D Converter with Track/Hold Function

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Analog input; range = GND < V_{IN} < V_{DD}.
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50μA current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.
11	V_{REF}^-	Lower limit of reference span. Sets the zero code voltage. Range: GND to V_{REF}^+.
12	V_{REF}^+	Upper limit of reference span. Sets the Full Scale input voltage. Range: V_{REF}^- to V_{DD}.
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than V_{REF}^+, $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	N.C.	Test Pin (No Connect)
20	V_{DD}	Power supply voltage, +5V.

Digital Interface

RD Mode (Pin 7 Low)

A conversion is started by taking $\overline{RD}$ low and keeping it low until output data appears (Figure 1). Pin 6 ($\overline{WR}$/RDY) is configured as a status output (RDY) in this mode, and is used with microprocessors which can be forced into a WAIT state. The processor starts a conversion, waits, and then reads data with a single READ instruction. RDY, an open collector output, goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion. $\overline{INT}$ goes low at the end of the conversion and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

WR-RD Mode (Pin 7 High)

In the WR-RD mode, pin 6 ($\overline{WR}$/RDY) is the WRITE input for the converter. With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{WR}$. There are several options for reading data:

Using the Internal Delay

The processor waits for $\overline{INT}$ to go low before reading data (Figure 2). $\overline{INT}$ typically goes low 600ns after the rising edge of $\overline{WR}$, indicating that the conversion is complete. With $\overline{CS}$ low, DB0-DB7 are read by pulling $\overline{RD}$ low. $\overline{INT}$ is then reset on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Reading Before Delay

The conversion time is externally controlled with $\overline{RD}$ (Figure 3). The status of $\overline{INT}$ is ignored and $\overline{RD}$ is taken low as soon as 600ns after the rising edge of $\overline{WR}$. This completes the conversion and enables DB0-DB7. $\overline{INT}$ goes low after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$.

Pipelined Operation

"Pipelined" operation is achieved by tying $\overline{WR}$ and $\overline{RD}$ together (Figure 4). With $\overline{CS}$ low, taking $\overline{WR}$ and $\overline{RD}$ low starts a new conversion and, at the same time, reads the result of the previous conversion.

Stand-Alone Operation

In stand-alone operation, $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by pulling $\overline{WR}$ low (Figure 5). Output data is valid approximately 600ns after the rising edge of $\overline{WR}$.

Analog Considerations

Reference Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter set the full-scale and zero input voltages. The voltage at $V_{REF}(-)$ defines the input level which produces an output code of all zeroes, and the voltage at $V_{REF}(+)$ defines the input which produces an output code of all ones (see Figure 6). Figure 7 shows some reference configurations.

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. The lead length of these capacitors should be as short as possible. If the reference inputs (pins 11, 12) are driven by long lines, they also should be bypassed to GND with 0.1 μF capacitors at the reference input pins.

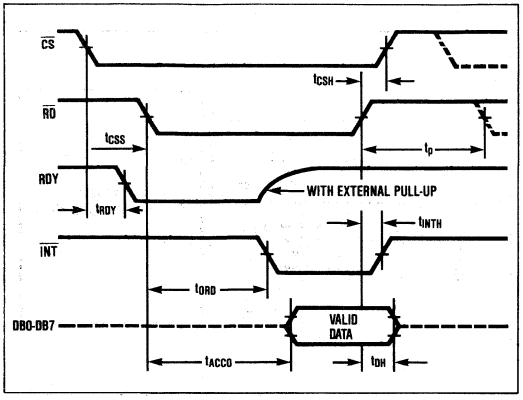


Figure 1. RD Mode Timing

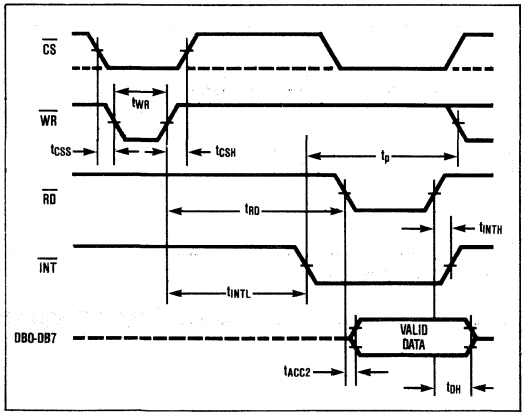


Figure 2. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

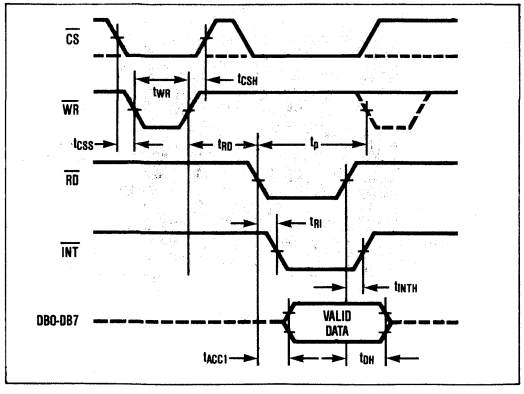


Figure 3. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

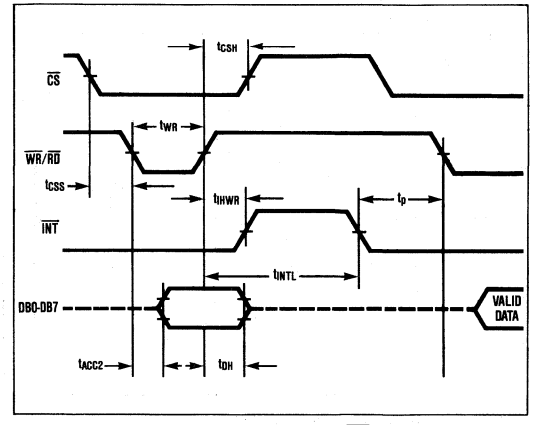


Figure 4. WR-RD Mode Pipe-Lined Timing, $\overline{WR} = \overline{RD}$

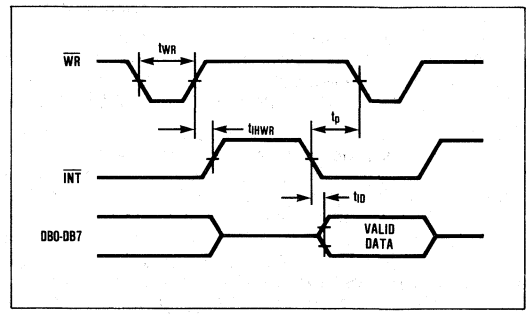


Figure 5. WR-RD Mode Stand-Alone Timing, $\overline{CS} = \overline{RD} = 0$

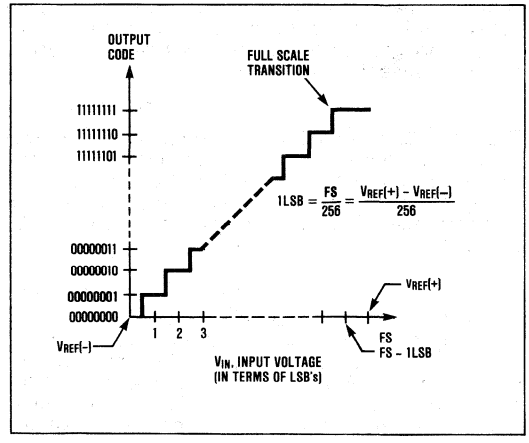


Figure 6. Transfer Function

CMOS High Speed A/D Converter with Track/Hold Function

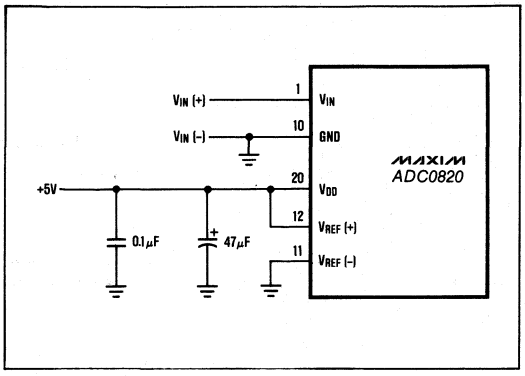


Figure 7a. Power Supply as Reference

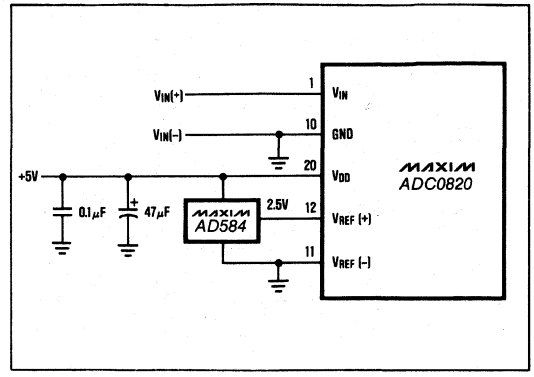


Figure 7b. External Reference 2.5V Full Scale

Input Current

The ADC0820 analog input behaves somewhat differently from conventional A/D converters. The ADC0820 takes varying amounts of current from the input depending on the operating cycle of the A/D.

During the input sampling phase ($\overline{WR}$ = LOW in the (WR-RD Mode) input capacitors must be charged to the input voltage through the resistance of internal analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of stray capacitance (C_S) must be charged. An equivalent RC model of the input is shown in Figure 8. The 45pF input capacitance allows source resistances (R_S) of up to 1kΩ to be used without increased settling time. For larger resistances, the width of the $\overline{WR}$ pulse must be increased from 600ns. In the RD mode, where the sample time is fixed, R_S greater than 1kΩ may cause settling errors. In this case, use the WR-RD mode and greater than 600ns $\overline{RD}$ time, or use a buffer to drive the analog input.

Input Filtering

The ADC0820's sampled data comparators generate input transients at V_{IN}. This does not degrade performance since the A/D only "looks" at the input after these transients occur. It is not necessary to filter these transients with an external capacitor at the V_{IN} terminal.

Inherent Track-and-Hold

The ADC0820 can measure a variety of high speed input signals without the help of an external sample-and-hold. The input is tracked from the time $\overline{WR}$ goes low (in the WR-RD mode) to approximately 100ns after it returns high. Input signals with slew rates typically up to 200mV/μs can be converted without error.

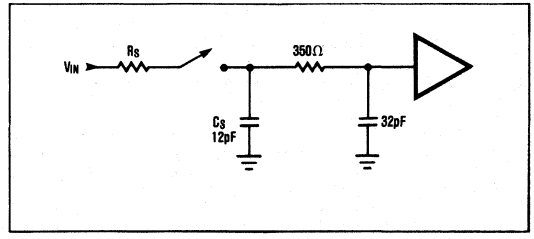
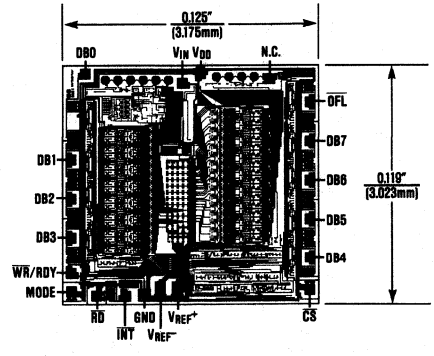


Figure 8. Equivalent Input Model

Chip Topography



MAXIM

3½ Digit A/D Converter

General Description

The Maxim ICL7106 and ICL7107 are monolithic analog to digital converters. They have very high input impedances and require no external display drive circuitry. On-board active components include polarity and digit drivers, segment decoders, voltage reference and a clock circuit. The ICL7106 will directly drive a non-multiplexed liquid crystal display (LCD) whereas the ICL7107 will directly drive a common anode light emitting diode (LED) display.

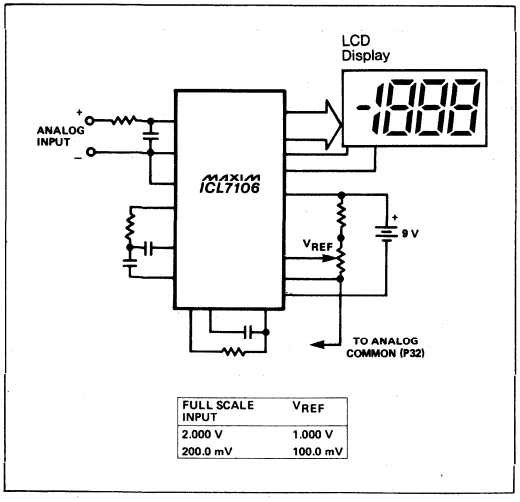
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7106 and ICL7107, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

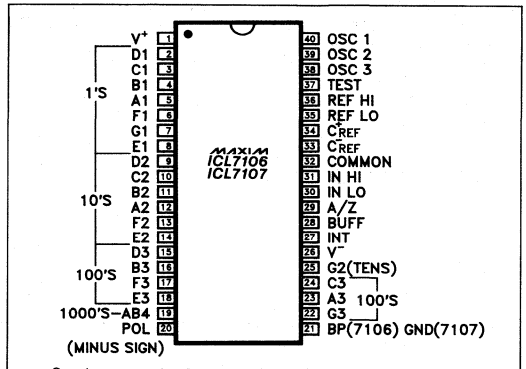
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
  LCD-ICL7106
  LED-ICL7107
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **True Differential Reference and Input**
- **True Polarity Indication for Precision Null Applications**
- **Monolithic CMOS design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7106CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7106CJL	0°C to +70°C	40 Lead CERDIP
ICL7106CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7106C/D	0°C to +70°C	Dice
ICL7107CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7107CJL	0°C to +70°C	40 Lead CERDIP
ICL7107CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7107C/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Cerdip Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	-1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A=25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

3½ Digit A/D Converter

- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 7)**
- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Negligible Hysteresis**
- **Maxim Quality and Reliability**
- **Increased Maximum Rating for Input Current (Note 8)**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 6)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 6)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV				
	T_A = 25°C (Note 6)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ 70°C (Note 10)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 6)		1	10	pA
	0° ≤ T_A ≤ 70°C		**20**	**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0				
	T_A = 25°C		0.6	1.8	mA
	0° ≤ T_A ≤ 70°C			**2**	
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
7106 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7107 Only—Segment Sinking Current (Except Pin 19)	V^+ = 5.0V	5	8.0		mA
(Pin 19 only)	Segment Voltage = 3V	10	16		mA
7106 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 9)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 6: Test condition is V_{IN} applied between pin IH-HI and IN-LO through a 1MΩ series resistor as shown in Figures 1 and 2.

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 9: Number of measurement cycles for display to give accurate reading.

Note 10: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter

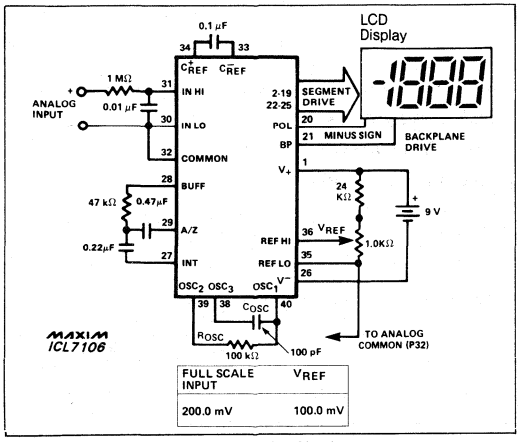


Figure 1. Maxim ICL7106 Typical Operating Circuit

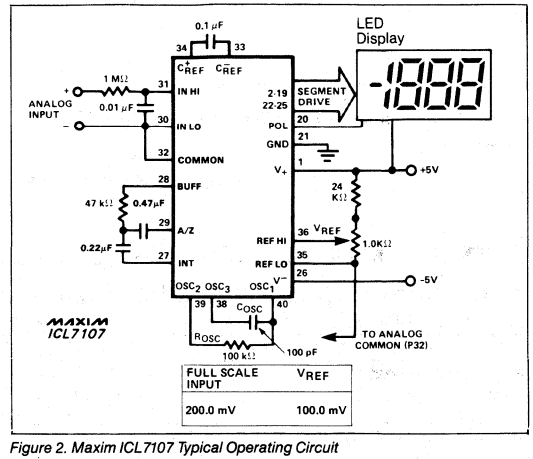


Figure 2. Maxim ICL7107 Typical Operating Circuit

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" overrange conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a rollover voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This happens during de-integration of a positive signal. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifer can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical

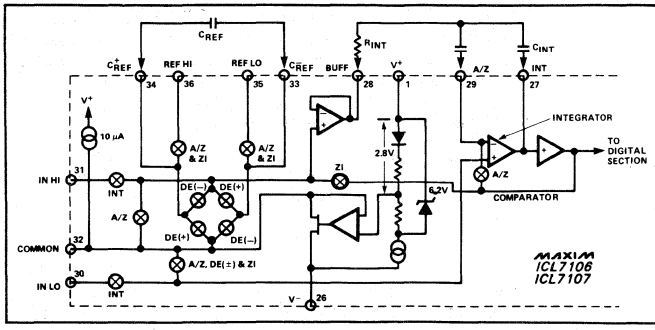


Figure 3. Analog Section of ICL7106/ICL7107

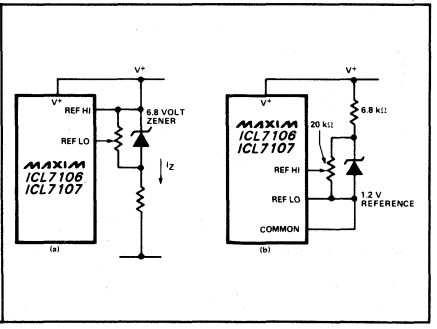


Figure 4. Using an External Reference

applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful when using the ICL7106, or for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The analog common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80ppm/°C, and a low voltage coefficient (.001%).

The internal heating of the ICL7107 by the LED display drivers degrades the stability of Analog Common. The power dissipated by the LED display drivers changes with the displayed count, thereby changing the temperature of the die, which in turn results in a small change in the Analog Common voltage. This combination of variable power dissipation, thermal resistance, and temperature coefficient causes a 25–80µV increase in noise near full scale. Another effect of LED display driver power dissipation can be seen at the transition between a full scale reading and an overload condition. Overload is a low power dissipation condition since the three least significant digits are blanked in overload. On the other hand, a near full scale reading such as 1999 has many segments turned on and is a high power dissipation condition. The difference in power dissipation between overload and full scale may cause a ICL7107 with a negative temperature coefficient reference to cycle between overload and a near full scale display as the die alternately heats and cools. An ICL7107 with a positive TC reference will exhibit hysteresis under these conditions: once put into overload by a voltage just barely more than full scale, the voltage must be reduced by several counts before the ICL7107 will come out of overload.

None of the above problems are encountered when using an external reference. The ICL7106, with its low power dissipation, has none of these problems with either an external reference or when using Analog Common as a reference.

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from analog-common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, REF-LO should be connected to analog common. This will remove the common-mode voltage from the reference system.

Analog Common is internally tied to an N-channel FET that can sink 30mA or more of current. This will hold the Analog Common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 10µA of source current, however, so COMMON may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD if left in this mode for several minutes.

3½ Digit A/D Converter

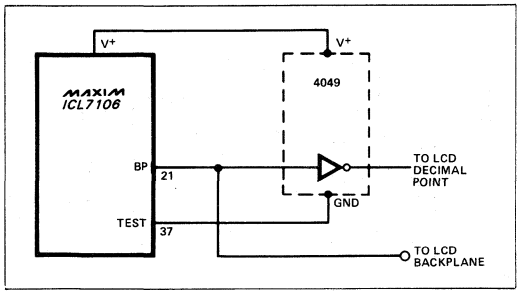


Figure 5A. Fixed Decimal Point Drivers

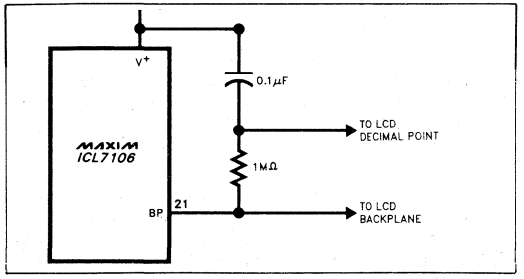


Figure 5B. Fixed Decimal Point Drivers

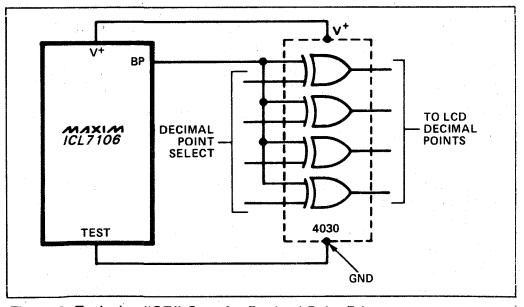


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Digital Section

The digital section for the ICL7106 and ICL7107 is illustrated in Figures 8 and 9. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the segment is ON and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The ICL7107 is identical to the ICL7106 except that the backplane and drivers have been replaced by N-channel segment drivers. The ICL7107 is designed to drive common anode LED's with a typical segment current of 8mA. Pin 19 (thousands digit output) sinks current from two LED segments, and has a 16mA drive capability.

The polarity indication is "on" for negative analog inputs, for both the ICL7106 and ICL7107. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7106 and ICL7107 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 48kHz would be used to obtain three readings per second.

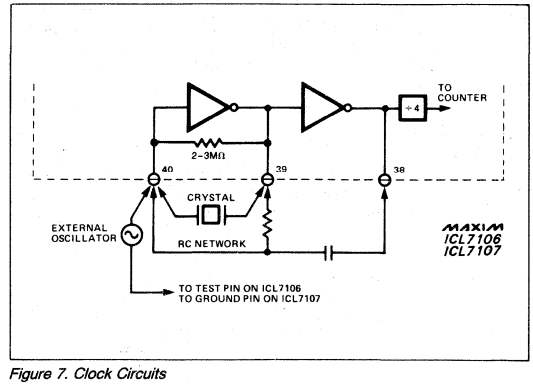


Figure 7. Clock Circuits

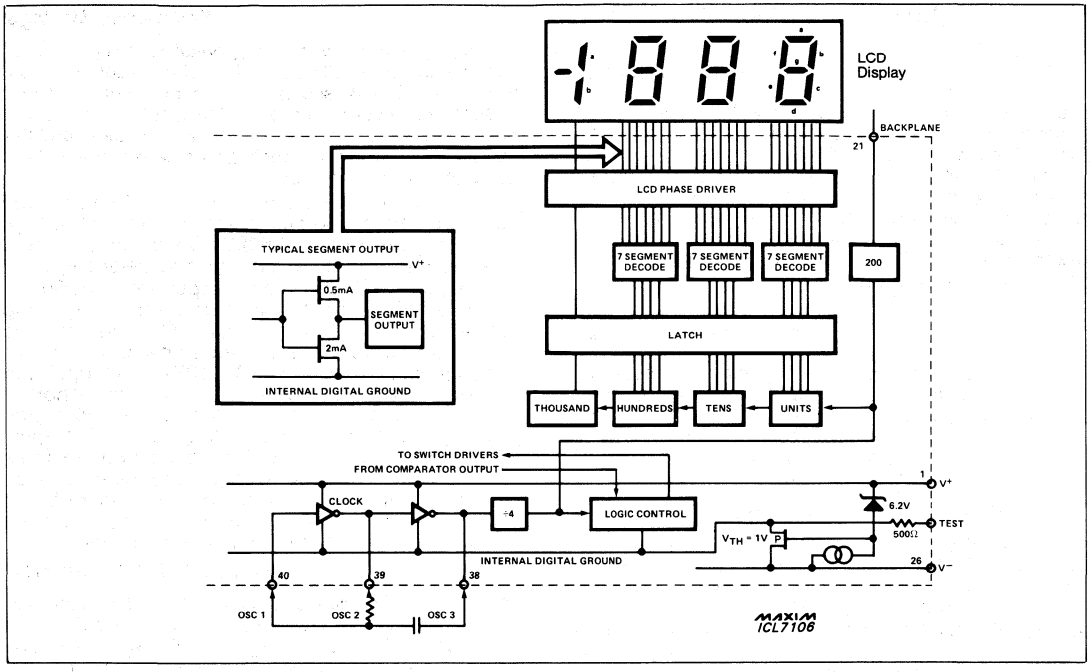


Figure 8. ICL7106 Digital Section

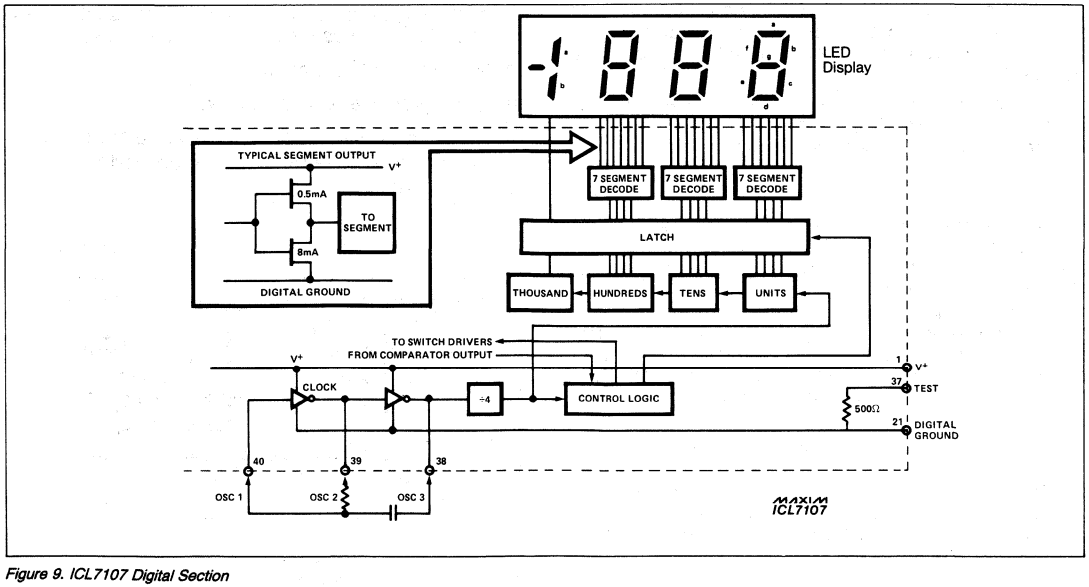


Figure 9. ICL7107 Digital Section

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Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For the 2V scale, a 0.047μF capacitor is adequate. A capacitor size of 0.47μF is recommended for 200mV full scale where low noise operation is very important. Due to the ZI phase of Maxim's ICL7106/7, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems seen in other manufacturers' ICL7106/7 which do not have the ZI phase.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent rollover error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (at approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable for the ICL7106 or ICL7107 when the analog common is used as a reference. A nominal ±3.5 to 4 volt swing is acceptable for the ICL7107 with a ±5V supply and analog common tied to supply ground. The nominal values for C_{INT} is 0.22μF for three readings per second. (48kHz clock). These values should be changed in inverse proportion to maintain the same output swing if different oscillator frequencies are used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100μA of quiescent current. 20μA of drive current can be supplied with negligible non-linearity. This resistor should be large enough to maintain the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 47KΩ resistor is recommended; (2V scale/470KΩ).

Oscillator Components

A 100KΩ resistor is recommended for all ranges of frequency. By using the equation f = 0.45/RC, the capacitor value can be calculated. For 48kHz clock, (3 readings/second), the oscillator capacitor plus stray capacitance should equal 100pF.

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. Suitable values of the capacitor and integrating resistor would be 0.22μF and 120KΩ. This provides for a slightly quieter system and also avoids a divider network on the input. The ICL7107 can accept input signals up to ±3.5V with ±5V supplies. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset reading can be conveniently generated.

ICL7107 Power Supplies

The ICL7107 is designed to operate from ±5V supplies. However, when a negative supply is not available it can be generated from a clock output with two diodes, two capacitors, and an inexpensive IC. Refer to Figure 10. Alternatively a −5V supply can be generated using Maxim's ICL7660 and two capacitors.

A negative supply is not required in selected applications. The conditions to use a single +5V supply are:

- An external reference is used.
- The signal is less than ±1.5V.
- The input signal can be referenced to the center of the common-mode range of the converter.

See Figure 18.

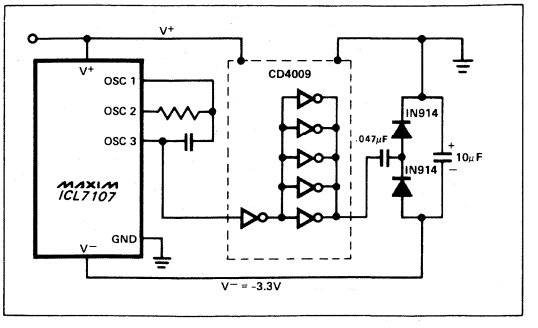


Figure 10. Generating Negative Supply from +5V

Applications Information

Heat is generated within the ICL7107 IC package due to the sinking of LED display current. Fluctuating chip temperature can cause a display to change reading if the internal voltage reference is used. By reducing the power being dissipated such variations can be reduced. The ICL7107 power dissipation is reduced by reducing the LED common anode voltage. The curve tracer illustration showing the relationship between the output current and the output voltage for typical ICL7107 is seen in Figure 11. Note that the typical ICL7107 output is 3.2V (point A), since the typical LED has 1.8V across it (8mA drive current) and its common anode is connected to +5V. Maximum power dissipation is:

$$8.1mA \times 3.2V \times 24 \text{ segments} = 622mW$$

Once the ICL7107 output voltage is above 2V, the LED current is essentially constant as output voltage increases. Point B illustrates that reducing the output voltage by 0.7V results in 7.7mA of LED current, (only 5% reduction). The maximum power dissipation is a reduction of 26% as calculated by:

$$7.7mA \times 2.5V \times 24 \text{ segments} = 462mW$$

As illustrated in Figure 12, reduced power dissipation is easy to obtain. This can be accomplished by placing either a 5.1Ω resistor or a 1 amp diode in series with the display (but not in series with the ICL7107). Point C of Figure 18 illustrates that a resistor will reduce the ICL7107 output voltage when all 24 segments are "On". The output voltage will increase when segments are turned "Off". On the other hand, the diode will result in a relatively steady output voltage, around Point B. The resistor not only reduces the change in power dissipation as the display changes, but also limits the maximum power dissipation. This is due to the fact that as fewer segments are "On", each "On" output drops more voltage and current. The resistor circuit will change about 230mW when changing from the best case of six segments, a "111" display, to worst-case of a "1888" display. If the resistor is removed, the power dissipation change will be 470mW. The resistor, therefore, will reduce the effect of display dissipation on reference voltage drift by about 50%.

As more segments are turned off, the change in LED brightness caused by the resistor is almost unnoticeable. A diode may be used instead of the resistor if it is important to maintain a steady level of display brightness.

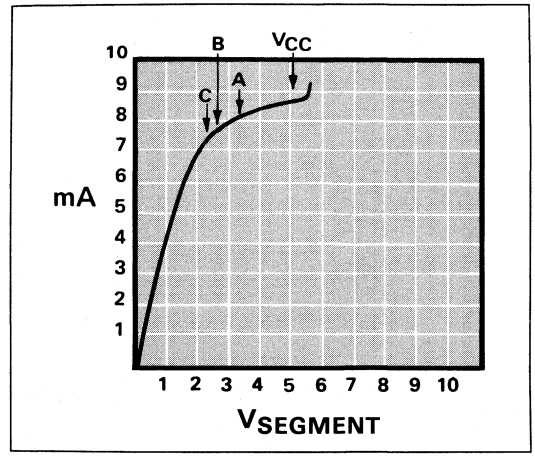


Figure 11. ICL7107 Output Current vs. Output Voltage

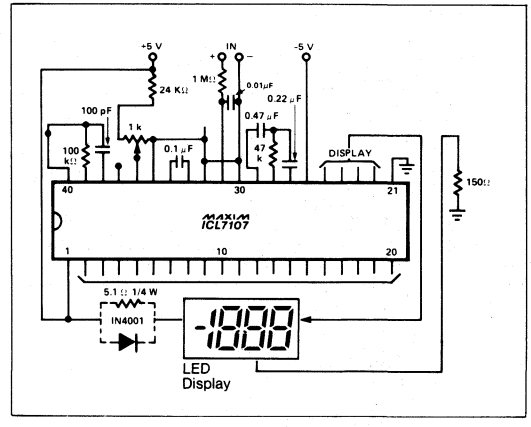


Figure 12. Diode or Resistor Limits Package Power Dissipation

3½ Digit A/D Converter

Typical Applications

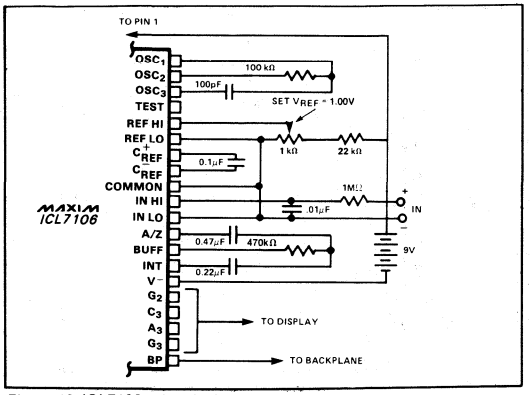


Figure 13. ICL7106 using the Internal Reference. 2V Full Scale; 3 Readings per Second.

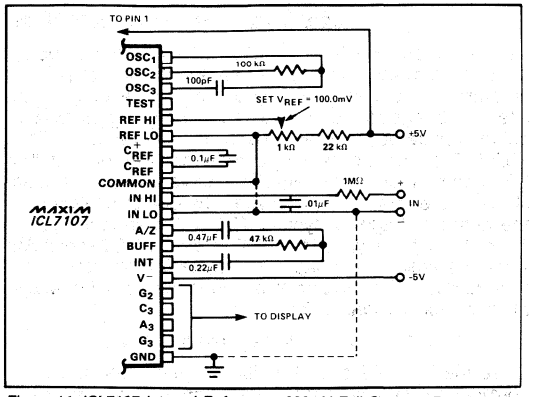


Figure 14. ICL7107 Internal Reference. 200mV Full Scale; 3 Readings per Second, V_{IN} Tied to GND for Single Ended Inputs. (See discussion under "Analog Common".)

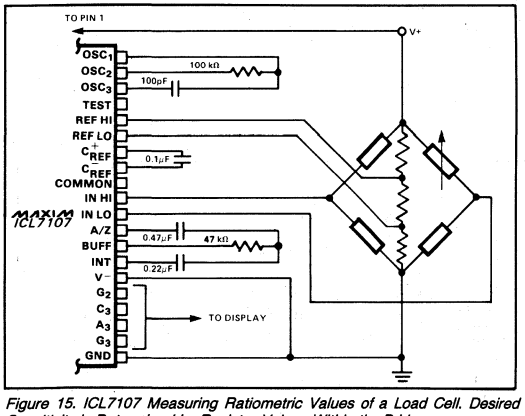


Figure 15. ICL7107 Measuring Ratiometric Values of a Load Cell. Desired Sensitivity is Determined by Resistor Values Within the Bridge.

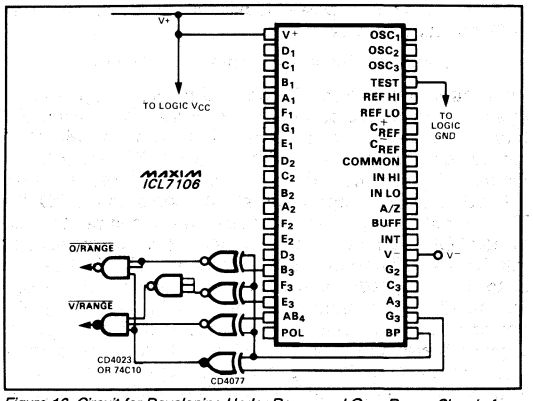


Figure 16. Circuit for Developing Under Range and Over Range Signals from ICL7106 Outputs.

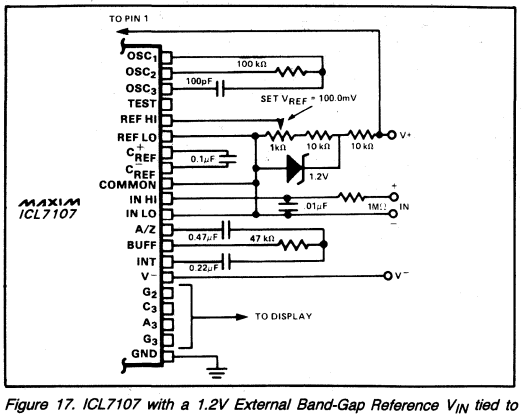


Figure 17. ICL7107 with a 1.2V External Band-Gap Reference V_{IN} tied to common.

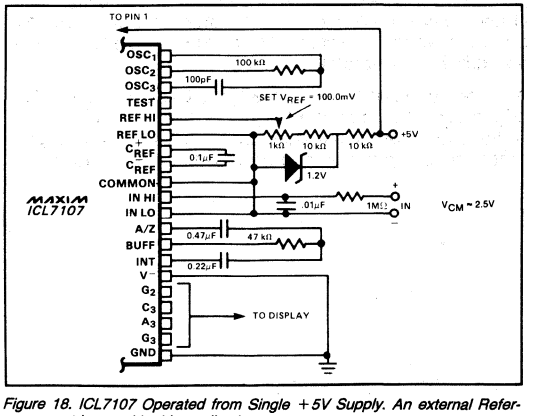


Figure 18. ICL7107 Operated from Single +5V Supply. An external Reference must be used in this application.

Typical Applications

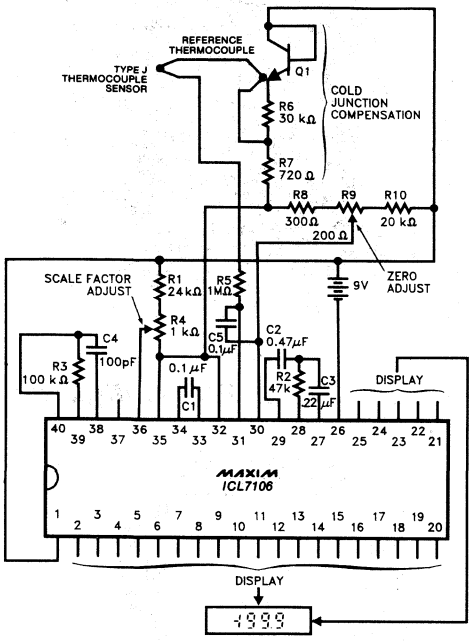


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4μV/°C output of a Type J thermocouple results in 1 count/°C.

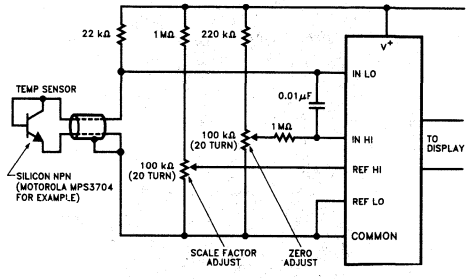


Figure 20. Digital Thermometer

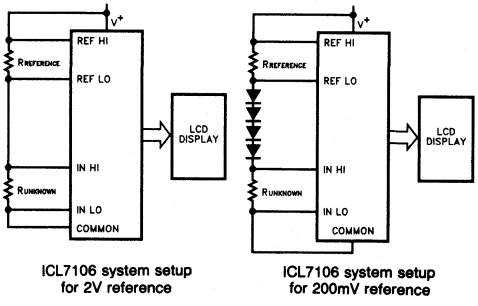
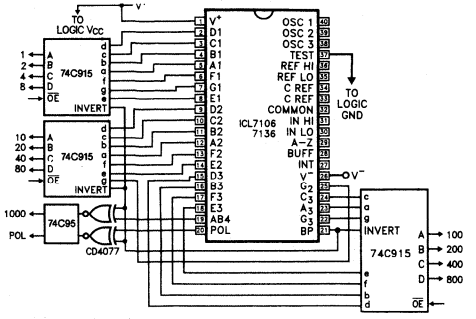
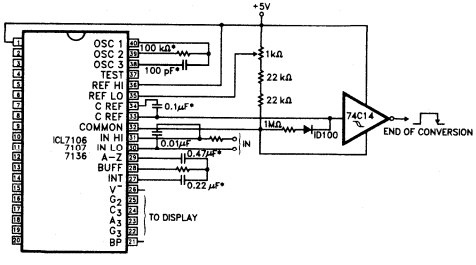


Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers

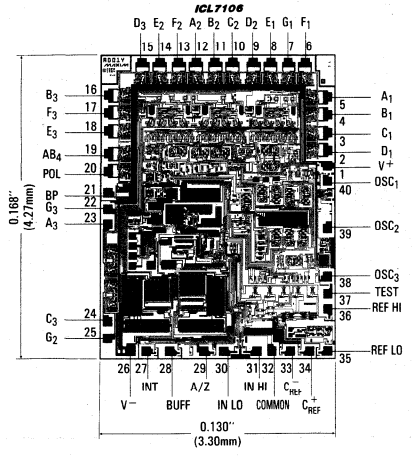


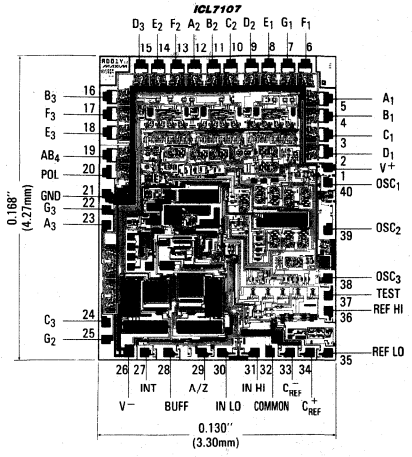
* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

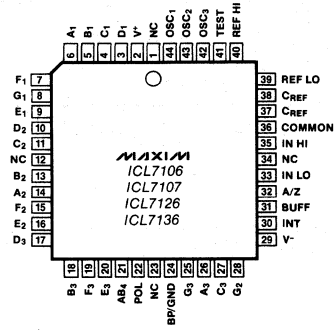
3½ Digit A/D Converter

Chip Topographies





Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

12 Bit A/D Converter With 3-State Binary Outputs

General Description

The ICL7109 is a monolithic 12 bit A/D converter designed for easy interface with microprocessors and UARTs. The 12 bit binary plus polarity and over-range outputs can be directly interfaced to a microprocessor bus. In this mode the ICL7109 is controlled by the microprocessor through the chip select and two byte enable inputs. For remote data logging applications the ICL7109 outputs are easily converted to a UART handshake mode, working with industry standard UARTs to provide serial data transmission.

This device offers high accuracy by lowering rollover error to less than 1 count and zero reading drift to less than 1 μV/°C. In many data acquisition systems the ICL7109 is an attractive, low cost, one-per-channel alternative to analog multiplexing due to its low power consumption and input bias current.

Maxim has added a zero-integrator phase to the ICL7109, eliminating overrange hangover, "crosstalk" and hysteresis effects. Maxim has also increased the current sourcing capabilities of the ICL7109, enabling it to rapidly drive the large capacitances often found on microprocessor busses.

Applications

This device is used in a wide range of data acquisition and control applications. Most applications involve the measurement of analog data:

Pressure	Speed	Voltage
Resistance	Flow	Weight
Temperature	Power	Current

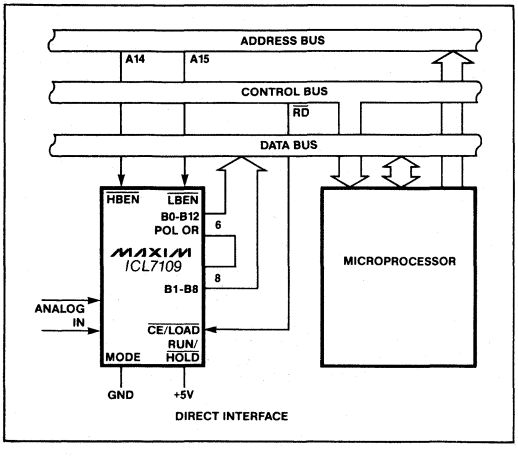
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Zero Integrator Phase for Fast Overload Recovery**
- **Hysteresis and "Crosstalk" Eliminated**
- **Enhanced Bus Driving Capability**
- **Byte Organized Three-state Outputs**
- **UART Handshake Mode for Serial Interfacing**
- **True Differential Input and Reference**
- **Up to 30 Conversions per Second**
- **Significantly Improved ESD Protection**
- **Monolithic, Low Power CMOS Design**

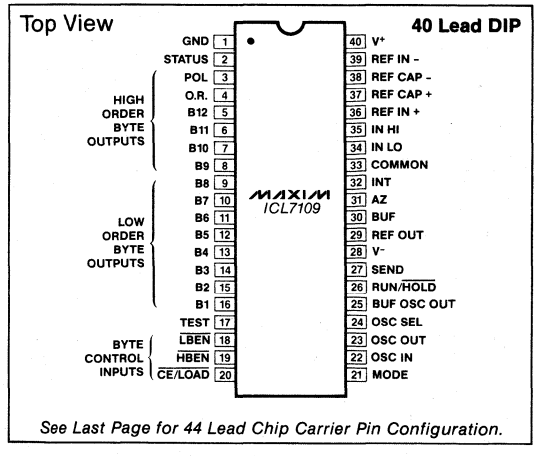
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7109MJL	-55°C to +125°C	40 Lead CERDIP
ICL7109IJL	-20°C to +85°C	40 Lead CERDIP
ICL7109CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7109CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7109C/D	0°C to +70°C	Dice

Typical Operating Circuit



Pin Configuration



See Last Page for 44 Lead Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

12 Bit A/D Converter With 3-State Binary Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) .... GND - 0.3V ≤ V_{IN} ≤ V^+ + 0.3V
Power Dissipation (Note 3)
Cerdip Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Plastic Chip Carrier (Quad) ..... 400mW @ +70°C

Operating Temperature
Cerdip Package (MJL) ..... -55°C ≤ T_A ≤ +125°C
Cerdip Package (CJL) ..... -20°C ≤ T_A ≤ +85°C
Plastic Package (CPL) ..... 0°C ≤ T_A ≤ +70°C
Plastic Chip Carrier
(Quad) Package (Q) ..... 0°C ≤ T_A ≤ 70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		V_{IN} = V_{REF} V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Low, Common	V^- +1.5		V^+ -1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	V_{IN} = 0 All devices 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C ICL7109IDC -25°C ≤ T_A ≤ +85°C ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V^+ -0.5 to V^- +1.0	V^+ -1.0	V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

12 Bit A/D Converter With 3-State Binary Outputs

- **Zero Integrator Phase ensures fast overload recovery**
- **"Crosstalk" and Hysteresis Eliminated**
- **Bus Driving Capability Enhanced**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 4)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Recovery Time				**0**	**1**	**Measurement Cycles**
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 5)	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 2.048V Over full operating temperature range (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	V_{CMR}	Input Hi, Input Low, Common	V^- +1.5		V^+-1.5	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input	I_{ILK}	V_{IN} = 0V All devices, T_A = 25°C ICL7109CPL CQ 0°C ≤ T_A ≤ +70°C ICL7109IJL -20°C ≤ T_A ≤ +85°C ICL7109MJL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} ≈ 408.9mV ≈ 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29 open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C

Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (test circuit per Mil Std 883, Method 3015.1).

Note 5: A 4.096V full scale voltage exceeds the Common Mode Voltage Range of the device. The full scale voltage has therefore been changed to 2.048V.

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

(All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless noted.)

DIGITAL SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	$I_{OUT} = 100\mu A$ Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage	V_{OL}	$I_{OUT} = 1.6mA$		0.2	0.4	V
Output Leakage Current		Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current		Pins 18, 19, 20 $V_{OUT} = V^+ -3V$ MODE input at GND		5		μA
Control I/O Loading		HBEN Pin 19 LBEN Pin 18			50	pF
Input High Voltage	V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage	V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current		Pins 26, 27 $V_{OUT} = V^+ -3V$		5		μV
Input Pull-up Current		Pins 17, 24 $V_{OUT} = V^+ -3V$		25		μA
Input Pull-down Current		Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High O_{OH}	$V_{OUT} = 2.5V$		1		mA
	Low O_{OL}	$V_{OUT} = 2.5V$		1.5		mA
Buffered Oscillator Output Current	High BO_{OH}	$V_{OUT} = 2.5V$		2		mA
	Low BO_{OL}	$V_{OUT} = 2.5V$		5		mA
MODE Input Pulse Width	t_W		50			ns

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

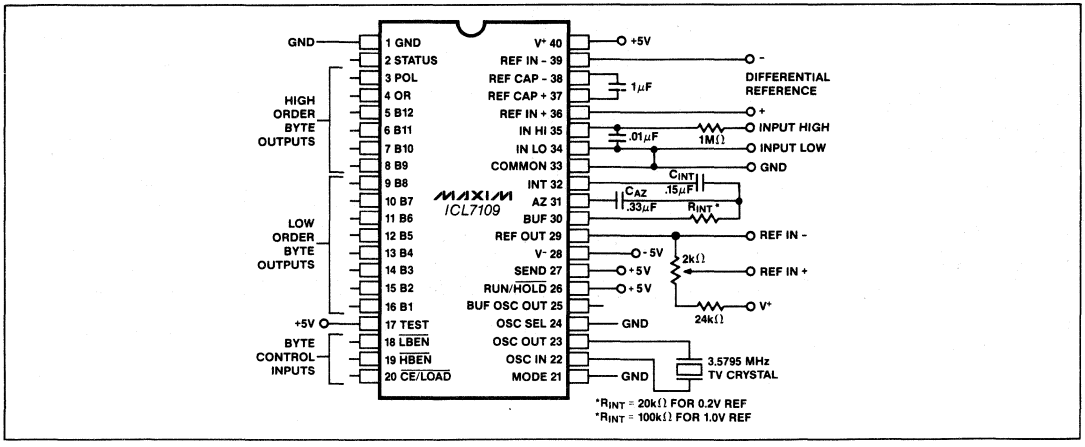


Figure 1. ICL7109 Test Circuit

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		**V_{OH}**	**Pins 2-16, 18-20. I_{OUT} = 1mA I_{OUT} = 100µA**	**3.5 4.0**	**4.3 4.5**		**V V**
Output Low Voltage		V_{OL}	I_{OUT} = -1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	µA
Control I/O Pullup Current			**Pins 18, 19, 20 V_{OUT} = V^+ -3V MODE input at GND**	**2**	**5**	**20**	**µA**
Control I/O Loading			HBEN Pin 19, LBEN Pin 18			50	pF
Input High Voltage		V_{IH}	Pins18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			**Pins 26, 27 V_{OUT} = V^+ -3V**	**2**	**5**	**20**	**µA**
Input Pull-up Current			**Pins 17, 24 V_{OUT} = V^+ -3V**	**5**	**100**	**300**	**µA**
Input Pull-down Current			**Pin 21 V_{OUT} = GND +3V**	**2**	**5**	**20**	**µA**
Oscillator Output Current	**High**	**O_{OH}**	**V_{OUT} = 2.5V**	**1**	**2**		**mA**
	Low	**O_{OL}**	**V_{OUT} = 2.5V**	**1.5**	**3**		**mA**
Buffered Oscillator Output Current	**High**	**BO_{OH}**	**V_{OUT} = 2.5V**	**2**	**4**		**mA**
	Low	**BO_{OL}**	**V_{OUT} = 2.5V**	**5**	**10**		**mA**
MODE Input Pulse Width		t_W	(Note 6)	50			ns
Byte Enable Width		t_{BEA}	(Note 6)	350	100		ns
Data Access Time from Byte Enable		t_{DAB}	(Note 6)		150	350	ns
Data Hold Time from Byte Enable		t_{DHB}	(Note 6)		100	300	ns
Chip Enable Width		t_{CEA}	(Note 6)	400	120		ns
Data Access Time from Chip Enable		t_{DAC}	(Note 6)		175	400	ns
Data Hold Time from Chip Enable		t_{DHC}	(Note 6)		150	400	ns

Note 6: Guaranteed by design; sample tested only.

12 Bit A/D Converter With 3-State Binary Outputs

Table 1. PIN FUNCTIONS

PIN	FUNCTION	TYPE	DESCRIPTION
1	GND		Ground return for digital logic, 0V
2	STATUS	Output	HI = Converter in integrate phase, or deintegrate phase until data is latched LO = Converter in zero-integrator phase, auto-zero phase, or deintegrate phase after data is latched.
3	POL	Three state data output bits	Polarity — HI = Positive input.
4	OR		Overrange — HI = Overranged
5	B12		Bit 12 = Most significant bit
6	B11		Bit 11
7	B10		Bit 10
8	B9		Bit 9
9	B8		Bit 8
10	B7		Bit 7
11	B6		Bit 6
12	B5		Bit 5
13	B4		Bit 4
14	B3		Bit 3
15	B2		Bit 2
16	B1		Bit 1 = Least significant bit.
17	TEST	Input	HI = Normal operation LO = All output bits high. MID = Counter output latches enabled. Connect to +5V if not used.
18	$\overline{LBEN}$	Input Output	Low Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking Low Byte Enable low activates low order byte outputs B1-B8. In handshake mode (when MODE is HI) this pin becomes a low byte flag output.
19	$\overline{HBEN}$	Input Output	High Byte Enable. When MODE is low and $\overline{CE/LOAD}$ is low, taking High Byte Enable low activates high order byte outputs B9-B12, POL & OR. In handshake mode (when MODE is HI) this pin becomes a high byte flag output.
20	$\overline{CE/LOAD}$	Input Output	When MODE is low, taking Chip Enable/Load high disables B1-B12, POL & OR. Taking it low enables B1-B12, POL & OR if $\overline{HBEN}$ and $\overline{LBEN}$ are low. In handshake mode (when MODE is HI) this pin becomes a load strobe output.
21	MODE	Input	LO = Converter in direct output mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as inputs controlling byte outputs directly. HI = Converter in handshake mode. Makes $\overline{LBEN}$, $\overline{HBEN}$ & $\overline{CE/LOAD}$ act as outputs.
22	OSC IN	Input	Oscillator input.
23	OSC OUT	Output	Oscillator output.
24	OSC SEL	Input	Taking Oscillator Select high or leaving it open configures OSC IN, OSC OUT & BUF OSC OUT as an RC oscillator. Clock frequency = BUF OSC OUT frequency. Taking it low configures OSC IN & OSC OUT for crystal oscillators. Clock frequency = BUF OSC OUT frequency ÷ 58.
25	BUF OSC OUT	Output	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input	HI = Continuous conversions every 8192 clock pulses. LO = Converter stops in auto-zero after completing the conversion in progress.
27	SEND	Input	Indicates ability of external device to accept data when converter is in handshake mode. Connect to +5V if not used.
28	V^-		Negative supply. Nominally -5V from GND.
29	REF OUT	Output	Reference voltage output. Nominally 2.8V below V^+.
30	BUFFER	Output	Buffer Amplifier Output.
31	AUTO-ZERO		Inside foil of C_{AZ} connects here.
32	INTEGRATOR	Output	Outside foil of C_{INT} connects here.
33	COMMON		Analog Common.
34	INPUT LO		Low side of differential input.
35	INPUT HI		High side of differential input.
36	REF IN^+		Positive input of differential reference.
37	REF CAP^+		Positive side of reference capacitor.
38	REF CAP^-		Negative side of reference capacitor.
39	REF IN^-		Negative input of differential reference.
40	V^+	Input	Positive supply. Nominally +5V from GND.

Note: All digital levels are positive true.

12 Bit A/D Converter With 3-State Binary Outputs

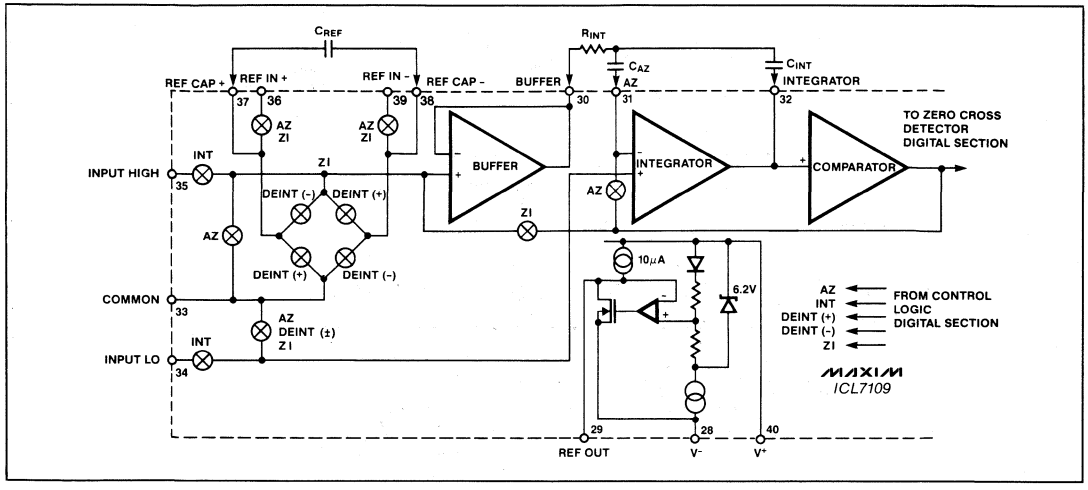


Figure 2. Analog Section

Detailed Description

Analog Section

The equivalent circuit of the Analog Section of the ICL7109 is shown in Figure 2. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle) when the RUN/HOLD input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 3. They are:

1. Auto-Zero (AZ)
2. Signal Integrate (INT)
3. De-integrate (DE)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during Auto-zero. The inputs, In-Hi and In-Lo, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. Lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy. In any event, the offset referred to the input is less than 10 μV.

Signal Integrate Phase

The internal input high (In-Hi) and input low (In-Lo) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between In-Hi and In-Lo for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. The polarity of the integrated signal is determined at the end of this phase.

De-Integrate Phase

The third phase is De-integrate, also known as reference integrate. Input high is internally connected across the previously charged reference capacitor and input low is internally connected to analog Common. The polarity detection circuit connects the reference capacitor with the polarity such that the integrator output returns with a fixed slope to the zero level established in the Auto-Zero phase. The time required for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Zero Integrator Phase

Input low is shorted to analog Common and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return rapidly to zero (See Figure 3). This phase normally lasts between 16 and 32 clock pulses but is extended to 1552 clock pulses after an overrange conversion.

This phase will remove any residual charge left on the integrator capacitor after an overload reading. This Zero Integrator phase virtually eliminates the problem of interaction or "crosstalk" between the various channels of a Maxim ICL7109 based multiple channel data acquisition system. Without the zero integrator phase, an overload on one channel would leave charge on the integrator capacitor, which would then be transferred to the autozero capacitor during the autozero cycle, resulting in an erroneous reading for the next channel that is measured after the channel with the overload.

12 Bit A/D Converter With 3-State Binary Outputs

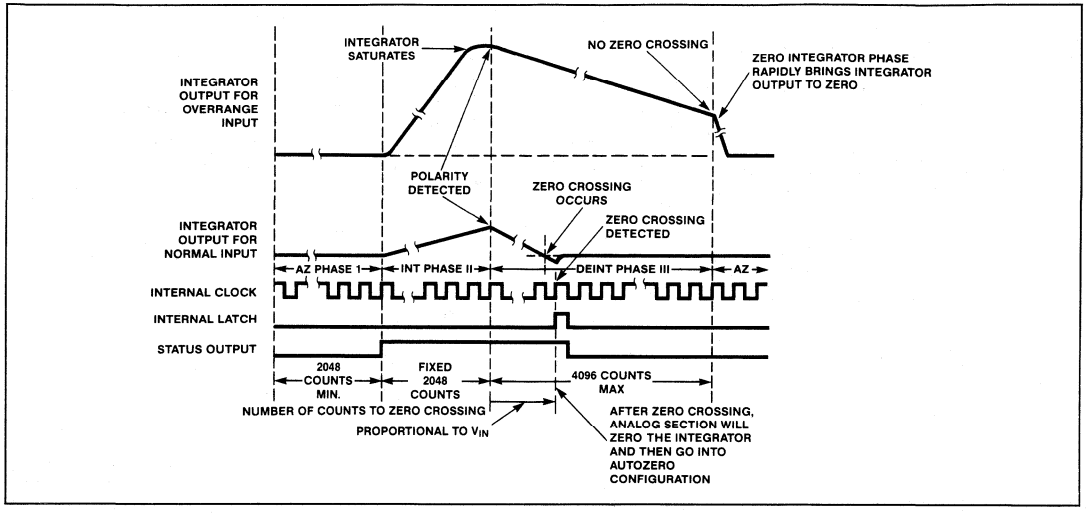


Figure 3. Conversion Timing (RUN/$\overline{HOLD}$ Pin High)

Differential Input

Differential input voltages anywhere within the common-mode range of the input amplifier can be accepted (specifically from 1.5V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB typical in this range. For optimum performance the input voltage at In-Lo and In-Hi should not come within 2 volts of either the positive or negative supply. Care must be exercised to ensure that the integrator output does not saturate, since the integrator also swings with the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator positive. The integrator output swing can be reduced to less than the recommended 4V full-scale swing with little loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

The ICL7109 has been optimized for operation with analog common near digital ground. This allows for a 4V full scale integrator swing positive or negative which maximizes performance of the analog section with ±5V power supplies.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Roll over error defines this difference in reference for positive or negative input voltages. This error can be held to less than one half count for worst-case condition by using an optimum reference capacitor. (See component value selection.)

By having the reference common mode voltage near or at analog COMMON, the roll-over error from these sources is minimized.

Component Value Selection

Care must be exercised in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate for optimum performance of the analog section. The optimum values must be selected for each application.

Integrating Resistor

Both the integrator and buffer amplifier have a class A output stage with a quiescent current of 100 μA, which can supply 20 μA with negligible non-linearity. The integrating resistor should be small enough that undue leakage requirements are not placed on the PC board, but large enough to keep the output current less than 40 μA. For 2.048 volt full scale, 100kΩ is optimum and similarly a 20kΩ is optimum for a 409.6mV scale. For other full scale voltages, R_{INT} should be selected by the relation

$$R_{INT} = \frac{\text{full scale voltage (mV)}}{20\ \mu A}\ k\Omega$$

Integrating Capacitor

C_{INT} (the integrating capacitor) should be selected for maximum integrator output voltage swing without saturation of the integrator (at 0.3 volt from either supply). A ±3.5 to ±4 volt integrator output swing is ideal for the ICL7109 with a ±5 volt supplies and analog common connected to GND. Nominal values for C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively, for 7½ conversions per second (61.44kHz clock frequency). These values should be changed to maintain the integrator output voltage swing, if different clock frequencies are used. The value of C_{INT} is generally given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing (V)}}\ \mu F$$

To prevent roll-over and linearity errors a low dielectric absorption capacitor is required. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon™ capacitors are recommended for the military temperature range. Polypropylene and Teflon™ capacitors should give less than 0.5 count of error due to dielectric absorption even though their absorption characteristics vary somewhat from unit to unit.

Auto-Zero Capacitor

The Maxim ICL7109 has a zero integrator phase which ensures that any charge left on the integrator after an overrange reading is removed before the autozero phase is started. This zero integrator phase allows the use of larger values of autozero capacitors than allowed with other manufacturer's ICL7109s. Normally, the optimum value of the autozero capacitor is between 2 and 4 times the value of the integrator capacitor. The typical value of the autozero capacitor is 0.33 μF. Lower values of C_{AZ} increase the noise in the autozero loop; very large values will take a longer time to charge to the proper value after power-up.

The outer foil of C_{AZ} should be connected to the R_{INT}, C_{INT} summing junction and the inner foil to pin 31 for optimal rejection of stray pickup. Similarly, the inner foil of C_{INT} should be connected to the RC summing junction, and the outer foil of C_{INT} should be connected to pin 32. Above 85°C, Teflon™, or equivalent capacitors are recommended for their low leakage characteristics.

Reference Capacitor

Good results can be achieved in most applications with a 1 μF capacitor. A larger value is required to prevent roll-over error where a 409.6mV scale is used and a large common mode voltage exists (i.e., the reference low is not at analog common). The roll-over error can generally be held to one half count by 10 μF in this case. Above 85°C, Teflon™, or equivalent capacitors are again recommended for their low leakage characteristics.

Reference Voltage

An analog input of $V_{IN} = 2 \times V_{REF}$ generates a full scale output of 4096 counts. For a normalized scale, a reference of 204.8mV should be used for a 409.6mV full scale (100 μV per LSB), and 1.024V reference should be used for a 2.048V full scale (500 μV per LSB). There will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output in many applications where the A/D is sensing the output of a transducer. In a weighing system, for example, the designer could possibly want a full scale reading when the voltage from the transducer is 0.682V. The input voltage should be measured directly and a reference voltage of 0.341V should be used instead of dividing the input down to 409.6mV. 34kΩ and 0.15 μF are suitable values for the integrating resistor and capacitor. A divider on the input is thus avoided. When a zero reading is desired for non-zero input, another advantage of this system is realized. Examples might include temperature and weight measurements with an offset or tare. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. It may be more efficient, however, to perform this type of scaling or tare subtraction digitally using software in processor-based systems using the ICL7109.

Reference Sources

A major factor in the overall absolute accuracy of the converter is the stability of the reference voltage. The resolution of the ICL7109 at 12 bits is 244 ppm or one part in 4096. Therefore, a temperature difference of 3°C will introduce a one-bit error if the reference has a temperature coefficient of 80 ppm/°C (like the onboard reference). Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made, an external high quality reference should be used.

To generate a suitable reference voltage, the ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider. This output will sink up to about 20mA without a significant output variation. A pullup bias device which sources about 10 μA is also provided. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80 ppm/°C typical. REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+, and REF OUT (Pin 29) should be connected to REF^- (pin 39) when using the onboard reference. Shown in the test circuit is the circuit for a 204.8mV reference. The fixed resistor should be removed for a 1V reference, and a 25kΩ precision

12 Bit A/D Converter With 3-State Binary Outputs

potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink sufficient current to destroy the device. By placing a 1kΩ resistor in series with pin 39, this can be avoided.

Detailed Description

Digital Section

The digital section (Figure 4) includes: 1) the clock oscillator and divider circuit; 2) a 12-bit binary counter with output latches and TTL-compatible three-state output drivers; 3) control logic; and 4) UART handshake logic.

Note: The term "clock cycles" as used in the following discussion relates to the internal clock, which is the oscillator output ÷ 58 when OSC SEL is low.

Three-State Outputs

The ICL7109 has 14 three-state outputs: 12 data bits, 1 polarity bit, and 1 overrange bit. These bits are enabled either by the $\overline{CE}$/LOAD, $\overline{LBEN}$ and $\overline{HBEN}$ control signals (see Table 2), or by entering the Handshake mode.

$\overline{CE}$/LOAD, $\overline{LBEN}$, and $\overline{HBEN}$

These three control pins can function as either inputs or outputs. In the Direct interface mode (see "Interfacing" below), these three pins are Chip Enable and Byte Enable inputs. In the Handshake mode these three pins become outputs that load data into the UART. These pins will be outputs while a handshake transfer is in progress or at any time that the Mode input is high.

Run/$\overline{Hold}$ Input

When the Run/$\overline{Hold}$ input is tied high, the ICL7109 continuously performs A/D conversions with a fixed length of 8192 clock cycles per conversion. When Run/$\overline{Hold}$ is taken low, the ICL7109 will complete the conversion in progress, then wait in the autozero phase. After the minimum autozero time has been completed, a high-going pulse on Run/$\overline{Hold}$ of at least 200 nanoseconds is required to start a new conversion; but any pulses during a conversion or up to 2048 clock cycles after Status goes low will be ignored. If the ICL7109 is holding at the end of the autozero phase, a new conversion will start and Status will go high within 7 clock cycles after Run/$\overline{Hold}$ goes high.

In addition to starting and stopping conversions, the Run/$\overline{Hold}$ pin can also be used to minimize conversion time. If Run/Hold is high, each conversion takes a full 8192 clock cycles, with the De-integrate phase taking 4096 clock cycles independent of input voltage. On the other hand, if Run/$\overline{Hold}$ is low at any time after Status goes low, the ICL7109 immediately jumps to the Auto-Zero phase rather than taking a full 4096 clock cycles for De-integrate. A simple way to ensure minimum conversion time is to drive the Run/$\overline{Hold}$ input with the Buffered Oscillator Output. When this is done, the conversion time is dependent on the input voltage: 4096 clock cycles for a zero voltage input, rising to 8192 clock cycles for full scale or overrange inputs.

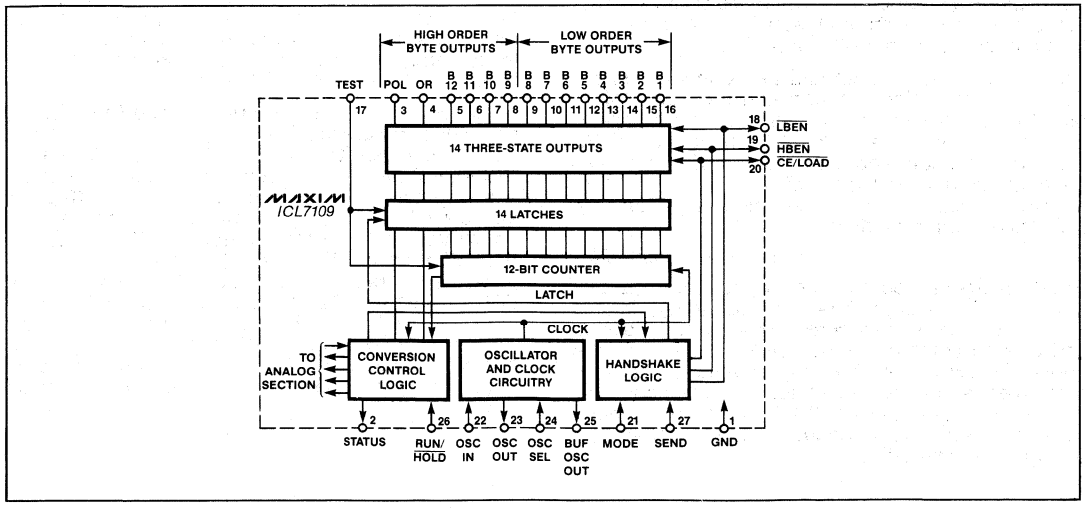


Figure 4. Digital Section

12 Bit A/D Converter With 3-State Binary Outputs

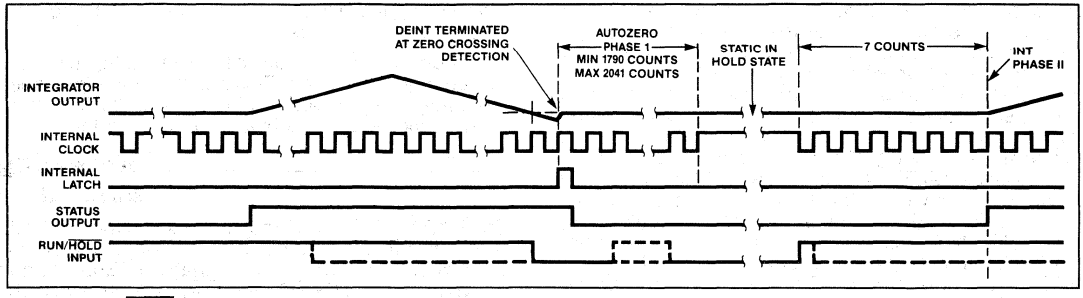


Figure 5. RUN/HOLD Operation

Mode Input

The Mode input is used to control the converter output mode. The converter is in its Direct output mode, where the output data is directly accessible under the control of the chip and byte enable inputs when the Mode pin is low or left open. (To ensure a low level when the pin is left open, this input is provided with an internal pulldown resistor.) When the Mode input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "Direct" mode. The converter will output data in the handshake mode at the end of every conversion cycle when the Mode input remains high. (See "Handshake Mode" section for more details.)

Send Input

The Send Input is a handshake control input used during handshake transfers. The use of Send to control a handshake interface is discussed in the "Interfacing" section, below.

The Maxim ICL7109 contains an improved power-up reset circuit that ensures that the ICL7109 powers up in the Direct mode if the Mode input is low, but other manufacturer's ICL7109s may power up in the Handshake mode even if the Mode input is held low. Although the Send input on the Maxim ICL7109 can be tied either high or low if only the Direct mode is used, other manufacturer's ICL7109s require that the Send input be tied high so that the ICL7109 will return to the Direct mode in 7 clock cycles if the Handshake mode is inadvertently entered on power-up.

Oscillator

The ICL7109 has a versatile three terminal oscillator that may be operated as a crystal or RC oscillator. It also may be overdriven by an external clock source. To optimize it for crystal or RC operation, the Oscillator Select input changes the internal configuration of the oscillator. The oscillator is configured for RC operation when the Oscillator Select input is high or left open (the input is provided with an internal pullup resistor), and the internal clock will be of the same phase and frequency as the signal at the Buffered Oscillator Output. (See Figure 6 for the resistor and capacitor connections.) Oscillation will occur in the circuit at a frequency given by f = 0.45/RC. The oscillator resistor should be 100kΩ. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection, but the capacitor value should not be less than 50pF.

A feedback device and input and output capacitors are added to the oscillator when the Oscillator Select input is low. With no external components, the oscillator will function with most crystals in the 1 to 5MHz range. (See Figure 7.) A fixed ÷ 58 circuit is inserted between the Buffered Oscillator Output and the internal clock by taking the Oscillator Select input low. This division ratio provides 33.18ms integration time, by using a 3.58MHz TV crystal.

$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58\text{MHz}} = 33.18\text{ms}$$

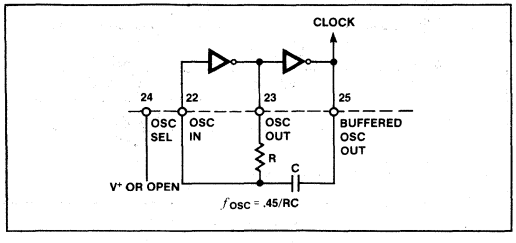


Figure 6. RC Oscillator

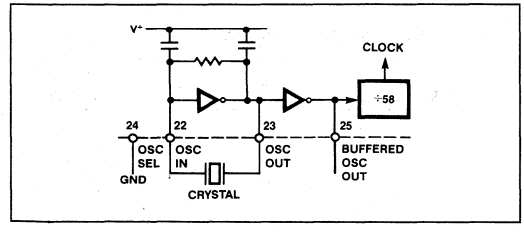


Figure 7. Crystal Oscillator

12 Bit A/D Converter With 3-State Binary Outputs

This time is quite close to 33.33ms or two 60Hz periods. The error is lower than one percent, which will yield better than 40dB of 60Hz rejection. If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the Oscillator Input, and the Oscillator Output should be left open. When Oscillator Select is left open, the internal clock will be of the same duty cycle, frequency and phase as the input signal. The clock will be the input frequency divided by 58 when Oscillator Select is at Ground. The divide by 58 circuit will operate reliably up to about 5MHz (Oscillator Select low), while the converter itself will operate at clock rates up to 2 MHz (Oscillator Select high). This implies a conversion rate of 244 conversions/sec. To operate the converter at these rates the auto-zero and integrating capacitors must be scaled using the guidelines in the Component Selection section. As the conversion rate increases, the accuracy of the converter is compromised, primarily due to noise and the delay of the comparator. If the clock period is less than the comparator delay (typically 1-3 μsec.), the low order bits become meaningless. At 2 MHz, typical readings with the inputs shorted may be 4-10 counts, rendering the 4 LSBs meaningless.

Note: At 15 conversions per second, the integration time of 2048 clock pulses equals one complete period of 60 Hz. This is therefore the maximum conversion rate that will provide 60 Hz noise rejection.

Status Output

At the end of a conversion cycle the Status output goes low, one-half clock period after new data from the conversion has been stored in the output latches. Status goes high at the beginning of Signal Integrate (Phase II). Figure 3 shows the timing details. This signal may be utilized as a flag indicating "data valid" for monitoring the status of the converter or to drive interrupts since data never changes while Status is low.

Test Input

The counter output latches are enabled when the Test input is taken to a level halfway between V^+ and Ground, allowing the counter contents to be examined. When the Test input is grounded, the internal clock is disabled and the counter outputs are all forced into the high state. The counter outputs will be clocked to the low state when the input returns to the 1/2 (V^+ -Ground) voltage (or to V^+) and one clock is applied. This facilitates testing of the counter and the output drivers.

Although the Test pin has an internal pullup, it should be tied high if not used. This ensures that high speed transitions on adjacent pins (particularly LBEN) do not inadvertently activate the test mode.

Table 2. DIRECT MODE TRUTH TABLE

$\overline{CE/LOAD}$	$\overline{LBEN}$	$\overline{HBEN}$	B1-B8	B9-B12, POL,OR
1	X	X	Hi-Z	Hi-Z
0	1	1	Hi-Z	Hi-Z
0	0	1	Data Out	Hi-Z
0	1	0	Hi-Z	Data Out
0	0	0	Data Out	Data Out

Interfacing

Direct Mode

The ICL7109 is in the Direct mode when the Mode pin is low. In this mode the output interface is a simple parallel interface with a Chip Enable ($\overline{CE/Load}$) and two byte enables ($\overline{HBEN}$ and $\overline{LBEN}$). As shown in the truth table of Table 2, the least significant 8 bits of data are enabled when both $\overline{CE/Load}$ and $\overline{LBEN}$ are low. The upper 4 bits of data, polarity, and overrange are enabled whenever $\overline{CE/Load}$ and $\overline{HBEN}$ are low. The Maxim version of the ICL7109 has significantly enhanced current sourcing capability, which enables it to rapidly drive the large capacitances often found on microcomputer busses.

In Figure 12, an approach to interfacing several ICL7109s to a bus is shown. This is achieved by using the $\overline{CE/Load}$ inputs (decoded from an address possibly) to select the desired converter, and tying the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together.

The ICL7109 can also be controlled through I/O peripheral ports, as shown in Figures 14, 15 and 16. Figures 13 through 16 are some practical circuits utilizing the parallel three-state output capabilities of the ICL7109. Shown in Figure 16 is a straightforward interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the ICL7109 data outputs are active at all times. The 8155 I/O ports may be utilized in the same way. Although a read performed while the data latches are undergoing updates will lead to scrambled data, this interface can be used in a read-

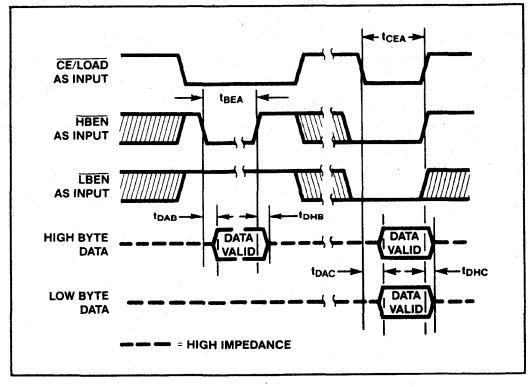


Figure 8. Direct Mode Output Timing

anytime mode. One way of solving this problem is to read the Status output as well. If it is high, read the data a second time after a delay of more than 1/2 converter clock period. If Status is still high, the first reading is correct. If Status is now low, the second reading is correct. On the other hand, the problem of timing is completely avoided by using a read-after-update sequence. (See Figure 14.) Data can be accessed by the high to low transition of the Status output driving an interrupt to the microprocessor. Figure 14 also demonstrates the Run/Hold input being used to initiate conversions under software control.

Figure 15 shows a similar interface to 650X or 680X systems. The transition of the Status output from high to low generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the Run/$\overline{\text{Hold}}$ pin through Control Register B. This application permits software-controlled initiation of conversions.

Direct interfacing to most microprocessor busses is allowed by the three-state output capability of the ICL7109. (See Figure 13 and the typical operating circuit on the first page.) It is important that the requirements for setup and hold times, and minimum pulse widths are met. There are also drive limitations on long busses that should be noted. In general, this type of interface is favored only if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can mandate several extra components. The use of interfacing devices will simplify the system in many cases.

Handshake Mode

Handshake Mode permits the interface with a number of external devices. For example, byte enables may be used as load enables or as byte identification flags, and external latches may be clocked by the rising edge of $\overline{\text{CE/Load}}$.

The handshake mode is specifically designed to directly interface the ICL7109 to industry standard UARTs, with no external logic required. The ICL7109 is in the handshake mode whenever the Mode input is high. In the handshake mode the $\overline{\text{CE/Load}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ pins are outputs and Send is an input. A typical UART to ICL7109 interface is shown in Figure 18, with the interface timing shown in Figures 9 through 11.

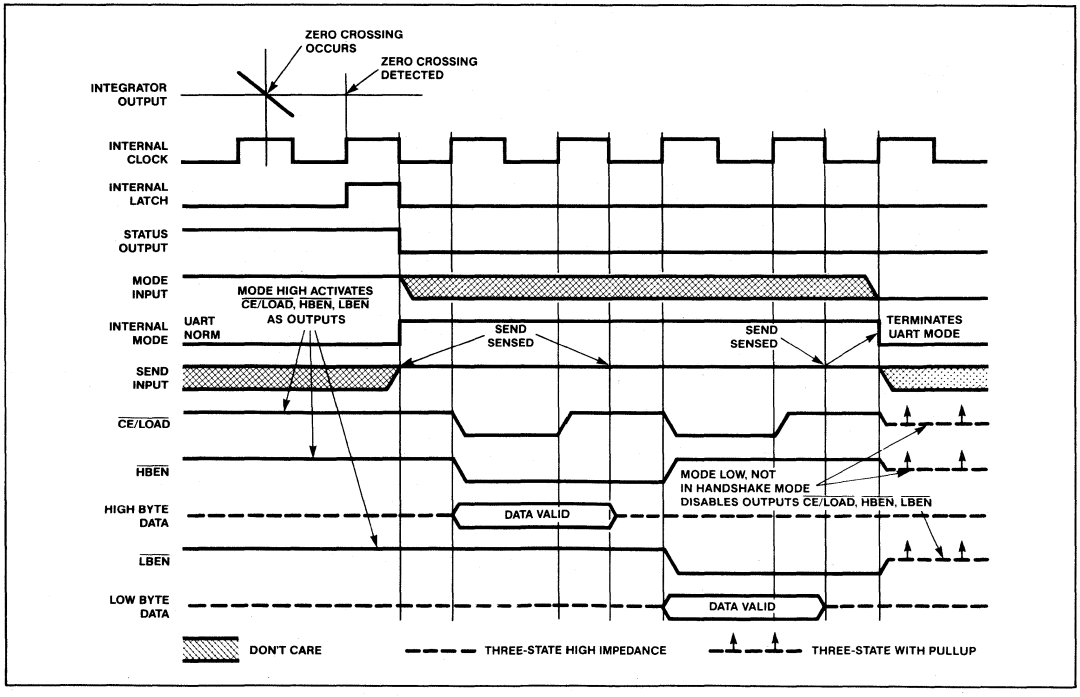


Figure 9. Handshake With Send Held Positive

12 Bit A/D Converter With 3-State Binary Outputs

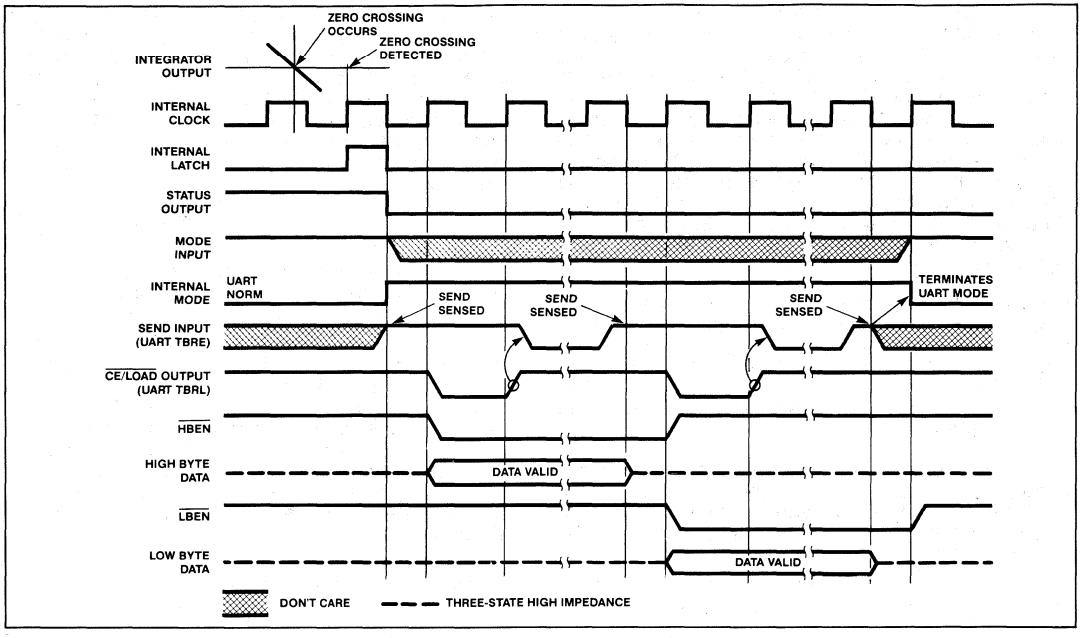


Figure 10. Handshake - Typical UART Interface Timing

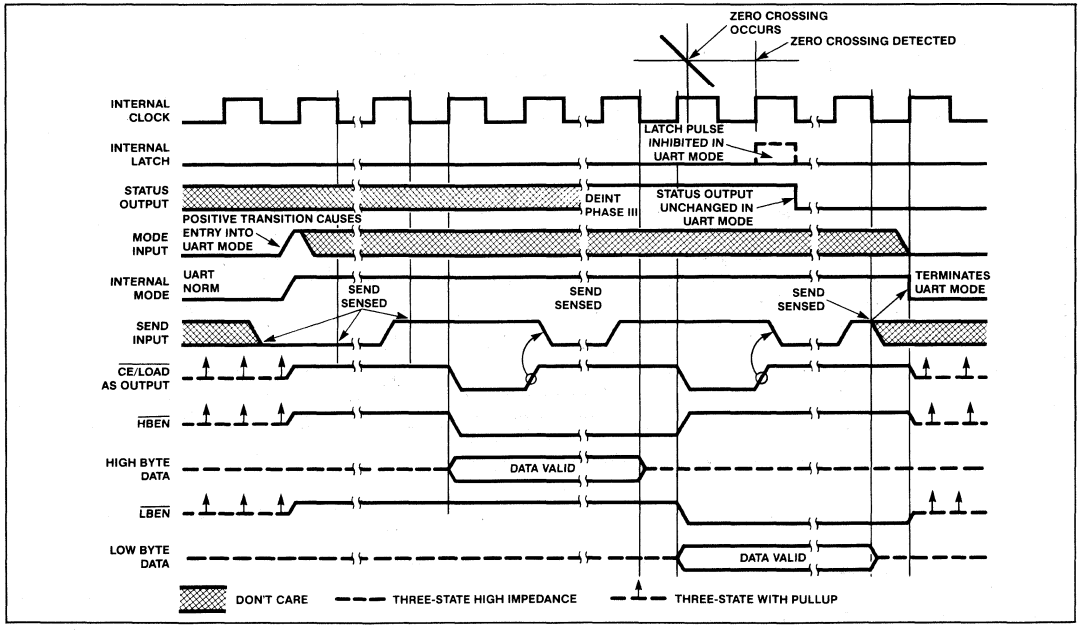


Figure 11. Handshake Triggered By Mode

When Mode is continuously held high, a new UART transmission will be started when Status goes low, provided Send is high at that time. As shown in Figure 10 the high byte of data will be written into the UART by the first pulse of $\overline{CE/Load}$. The $\overline{TBRE}$ signal of the UART will momentarily go low upon receiving the data. After the UART transfers the data to the transmitter register, the UART's $\overline{TBRE}$ output drives the ICL7109's Send input high. The ICL7109 senses the high level on the Send input and loads the low byte of data into the UART with a second pulse of $\overline{CE/Load}$. The ICL7109 continues its conversion cycles while this handshake takes place, and if the UART's $\overline{TBRE}$ has driven the ICL7109 Send input high by the end of the next conversion, the data transfer sequence will repeat. If the UARTs $\overline{TBRE}$ (and therefore the ICL7109's Send input) is low when the ICL7109 completes the next conversion, the internal latch pulse is inhibited and the data from that conversion is lost.

A handshake transfer can be initiated by a high-going pulse on the Mode pin. Upon receiving a high going pulse, the ICL7109 sets an internal Mode latch and will start a handshake transmission when Status goes low at the end of the next conversion. An alternate method of controlling the ICL7109 is to leave Mode high and initiate conversions via the Run/$\overline{Hold}$ input. With this method the ICL7109 will first make a conversion then transmit the data. Another method of initiating a transmission is shown in Figure 11. Here Mode is pulsed high while Send is low. A UART transmission is started when Send is taken high (at least 2 negative clock edges later).

The UART mode is also useful in interfacing the ICL7109 to I/O ports such as the 8255 and 6520. Figure 17 is an example of such an interface. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send input to the ICL7109, and using the $\overline{CE/Load}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1. The next conversion's result will be strobed into the port if the 8255 IBF flag is low and the ICL7109 is in handshake mode. The strobe will cause IBF to go high (Send goes low) which will prevent the ICL7109 from loading the second byte of data. The PPI will generate an interrupt. When executed, the result is that the data is read. The IBF will be reset low when the byte is read which causes the ICL7109 to sequence into the next byte. Figure 17 shows the PC7 line of the PPI connected to the Mode input of the ICL7109. If this input is tied high or left high, the data from every conversion will be sequenced into the system (provided the data access takes less time than a conversion). The output sequence can be obtained on demand by using the PC7 output to drive the Mode input. Note that the 8255 can service another peripheral device since only one port is used. The 8155 can utilize the same arrangement.

The ICL7109 is not limited to the applications described here. These examples show some of the many interfaces and uses of the ICL7109 and merely provide a point of departure for users to develop appropriate systems. Many of the suggestions made here may be combined. More specifically, the uses of the Mode, Status, and Run/$\overline{Hold}$ signals may be mixed.

Typical Applications

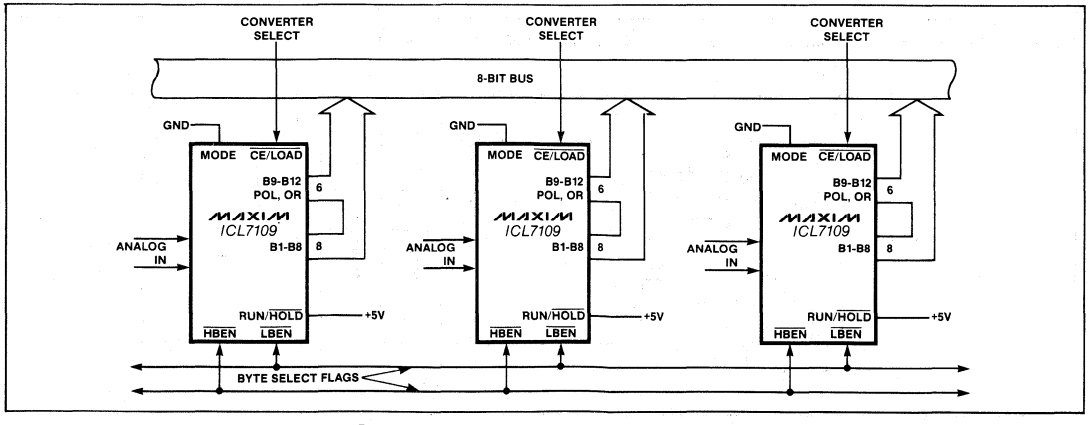


Figure 12. Three-stating several 7109s to a Bus

12 Bit A/D Converter With 3-State Binary Outputs

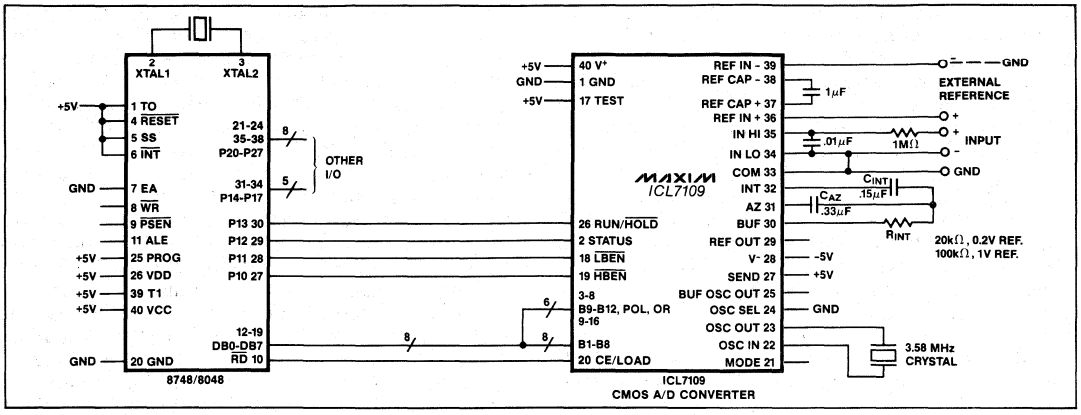


Figure 13. Typical Connection Diagram Parallel Interface with MCS-48 Microcomputer

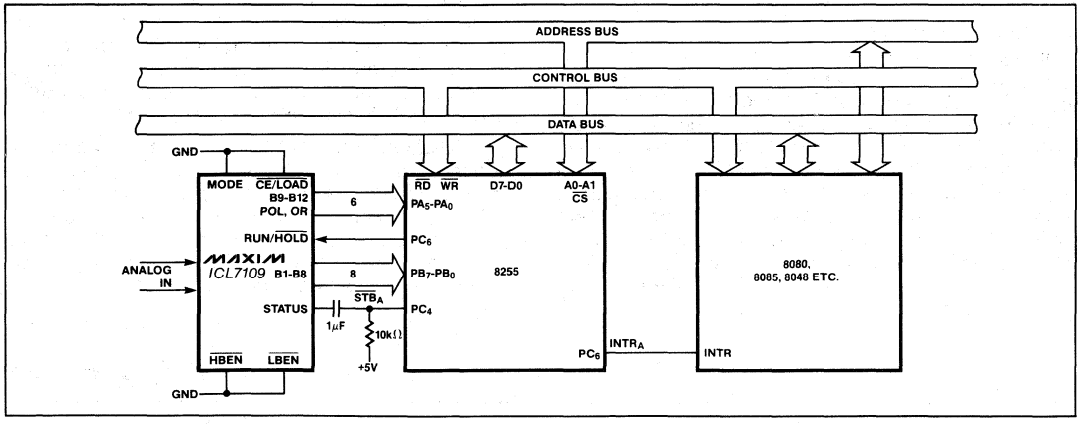


Figure 14. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

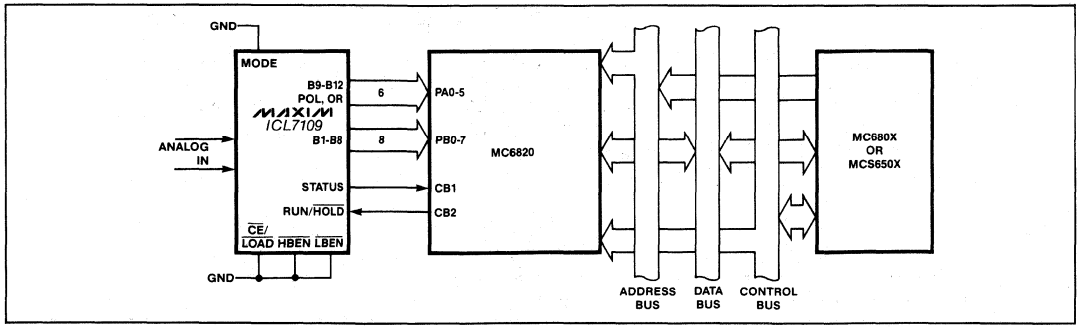


Figure 15. Full-time Parallel Interface to MS680X or MCS650X Microprocessors

12 Bit A/D Converter With 3-State Binary Outputs

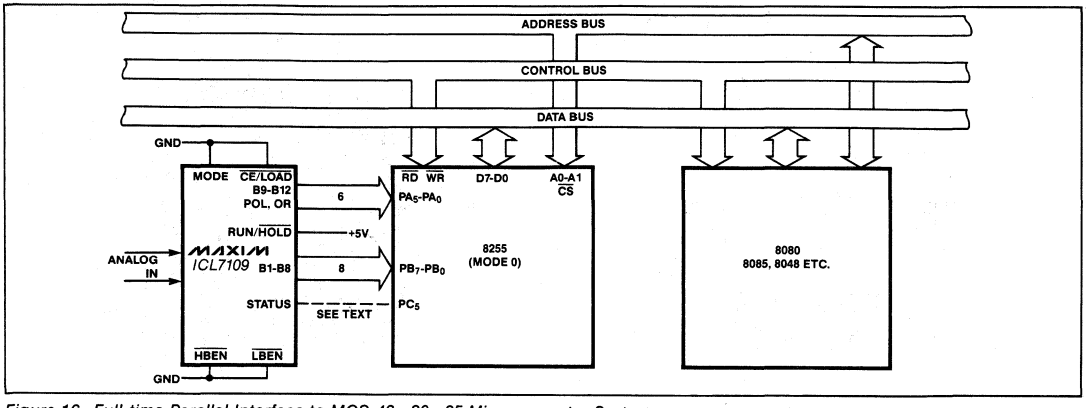


Figure 16. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

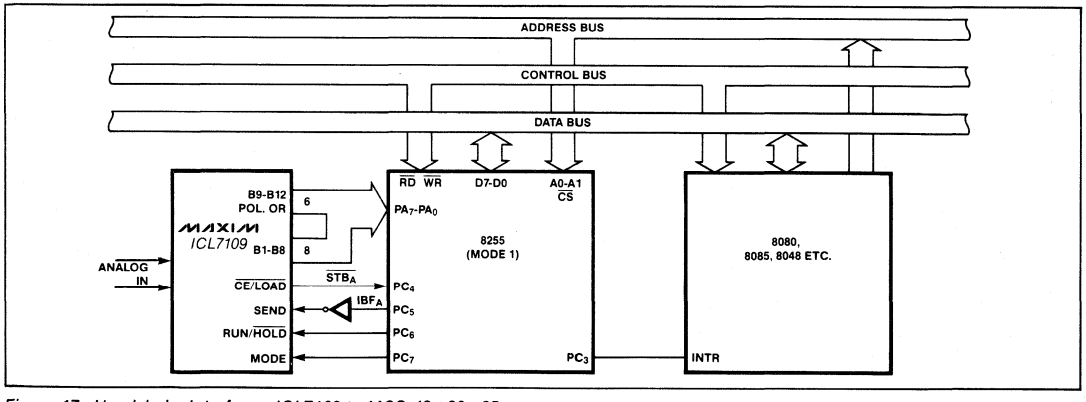


Figure 17. Handshake Interface - ICL7109 to MCS-48, -80, -85

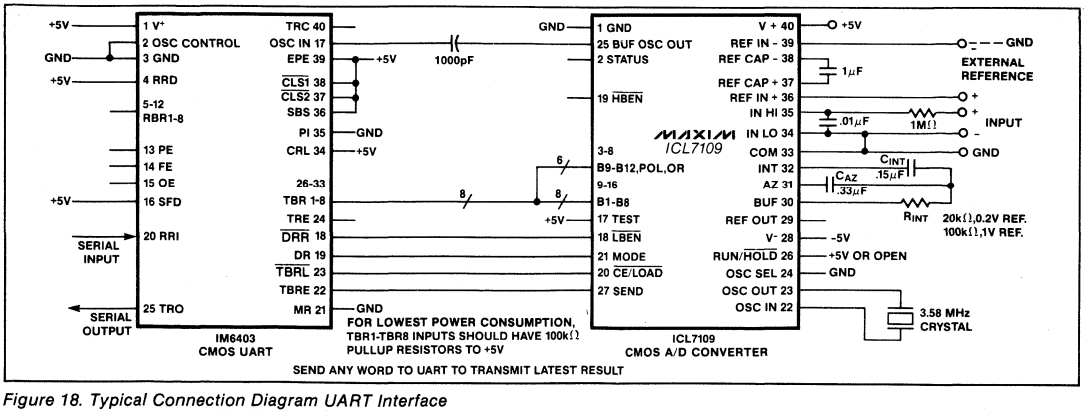
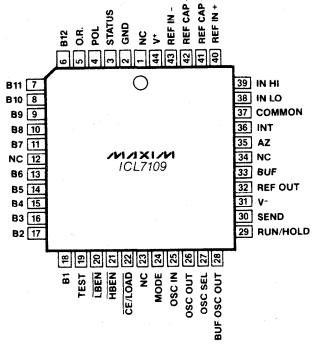


Figure 18. Typical Connection Diagram UART Interface

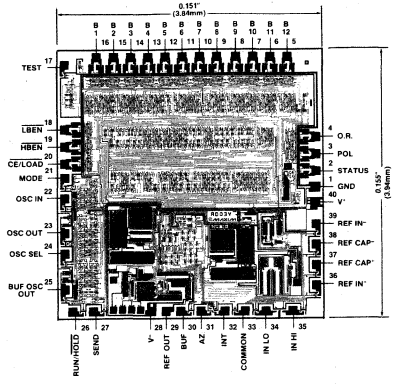
12 Bit A/D Converter With 3-State Binary Outputs

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



MAXIM

3½ Digit A/D Converter With Display Hold

General Description

The Maxim ICL7116 and ICL7117 are 3½ digit monolithic analog to digital converters. They differ from the Maxim ICL7106 and ICL7107 in that the ICL7116 and ICL7117 have a Hold pin which makes it possible to hold or "freeze" a reading. These integrating A/D converters have very high input impedances and directly drive LCD (ICL7116) and LED (ICL7117) displays.

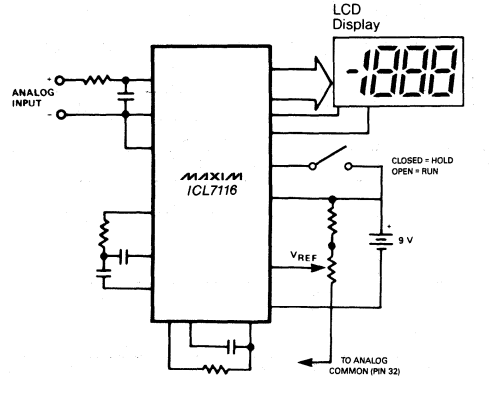
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input is particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7116 and ICL7117, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

Features

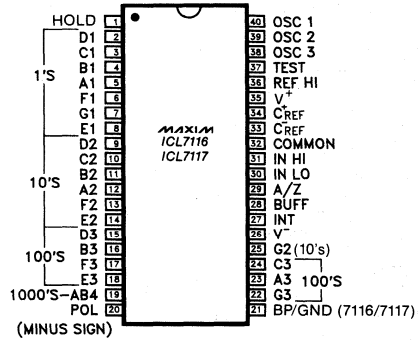
- **Improved 2nd Source! (See 3rd page of this data sheet for "Maxim Advantage™")**
- **Hold pin allows indefinite display hold.**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required: LCD-ICL7116, LED-ICL7117**
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7116CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7116CJL	0°C to +70°C	40 Lead CERDIP
ICL7116CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7116C/D	0°C to +70°C	Dice
ICL7117CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7117CJL	0°C to +70°C	40 Lead CERDIP
ICL7117CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7117C/D	0°C to +70°C	Dice

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7116, V^+ to V^- 15V
- ICL7117, V^+ to GND ..... +6V
- ICL7117, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7116 ..... TEST to V^+
- ICL7117 ..... GND to V^+

Power Dissipation (Note 2)
- Cerdip Package 1000mW
- Plastic Package 800mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	-1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0, 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5			V
7116 ONLY (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4 4	5 5	6 6	V
7117 ONLY (Except Pin 19) Segment Sinking Current (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion. (See Maxim's ICL7106/ICL7107 data sheet).

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

3½ Digit A/D Converter With Display Hold

- ◆ Guaranteed Overload Recovery Time
- ◆ Significantly Improved ESD Protection (Note 8)
- ◆ Low Noise
- ◆ Key Parameters Guaranteed over Temperature
- ◆ Negligible Hysteresis
- ◆ Maxim Quality and Reliability
- ◆ Increased Maximum Rating for Input Current (Note 9)

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1 (ICL7116), Figure 2 (ICL7117) unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C (Note 11)**	−000.0 **−000.0**	±000.0 **±000.0**	+000.0 **+000.0**	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C (Note 11)**	999 **998**	999/1000 **999/1000**	1000 **1001**	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 7) 0° ≤ T_A ≤ 70°C (Note 11)	−1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 7) **0° ≤ T_A ≤ 70°C**		1 **20**	10 **200**	pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 7)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0 T_A = 25°C **0° ≤ T_A ≤ 70°C**		0.6	1.8 **2**	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ −1.5			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7117 Only—Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA mA
7116 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 10)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 7: Test condition is V_{IN} applied between pins IN-HI and IN-LO. i.e., 1MΩ resistor in Figures 1 and 2.
Note 8: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std 883C, Method 3015 .2)
Note 9: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).
Note 10: Number of measurement cycles for display to give accurate reading.
Note 11: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim ICL7116 and ICL7117 3½ digit A/D converter are similar to the Maxim ICL7106 and ICL7107, except for the addition of a Hold pin. For a detailed product description, package dimensions, and applications information (other than the operation of the Hold pin described below) refer to Maxim's ICL7106 and ICL7107 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test (ICL7116) or V^+ and Ground (ICL7117). The ICL7116/7117 continuously performs conversions, independent of the Hold input. When the Hold input is connected to V^+, however, the display latch pulse is inhibited, and the display latches are not updated. The Hold input has a 70 kilohm pulldown resistor to Test (ICL7116) or Ground (ICL7117) and the Hold input will be pulled low if it is left open. When Hold is low the ICL7116/ICL7117 updates the display at the end of each conversion. The Hold input is CMOS compatible, and can also be driven by a switch connected to V^+ (Figure 1 and 2) or by a PNP transistor.

Unlike the ICL7106 and ICL7107, the ICL7116 and ICL7117 do not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

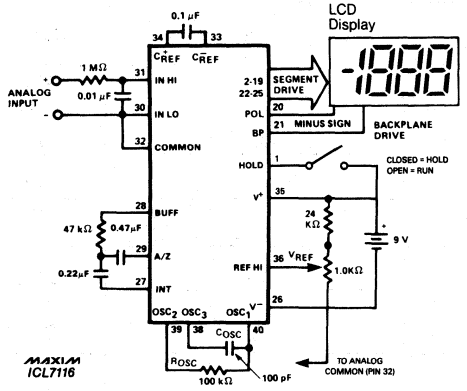


Figure 1. Maxim ICL7116 Typical Operating Circuit, 200mV Reference

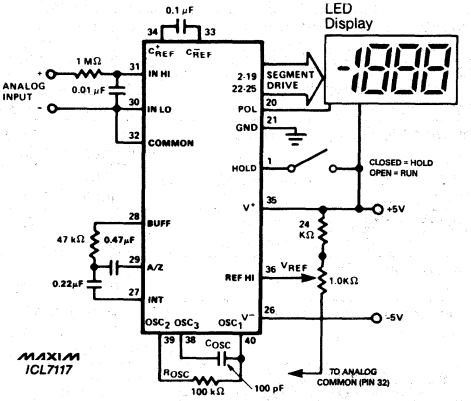
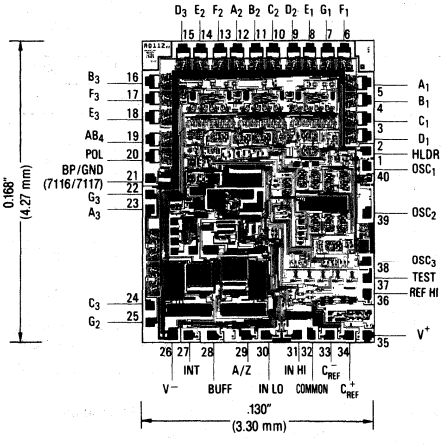
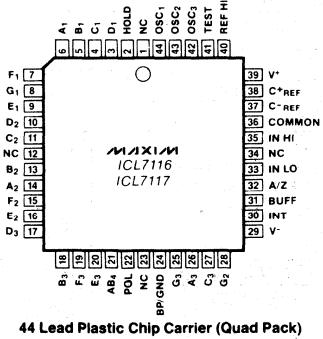


Figure 2. Maxim ICL7117 Typical Operating Circuit, 200mV Reference

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7126 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7126 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7126 a superior device, especially for portable systems.

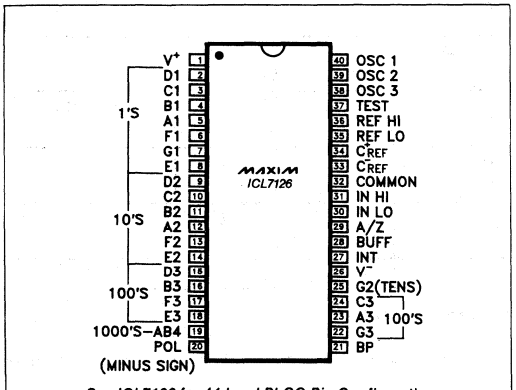
Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7126 eliminates overrange hangover and hysteresis effects. The Zero Integrator phase also allows the use of larger auto zero capacitors reducing noise further. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration



See ICL7106 for 44 Lead PLCC Pin Configuration

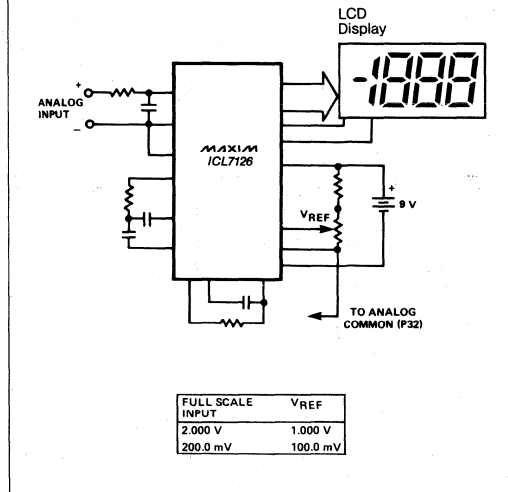
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guaranteed less than 1mW-9V battery life 3000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7126CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7126CJL	0°C to +70°C	40 Lead CERDIP
ICL7126CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7126C/D	0°C to +70°C	Dice

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Figure 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 8)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−V_{IN} = +V_{IN} 200.0mV				
	T_A = 25°C (Note 8)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 12)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		μV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0				
	T_A = 25°C		60	100	μA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	**250kΩ between Common & Pos. Supply**	**2.6**	**2.8**	**3.2**	**V**
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	**V_{IN} changing from ± 10V to 0V**		**0**	**1**	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

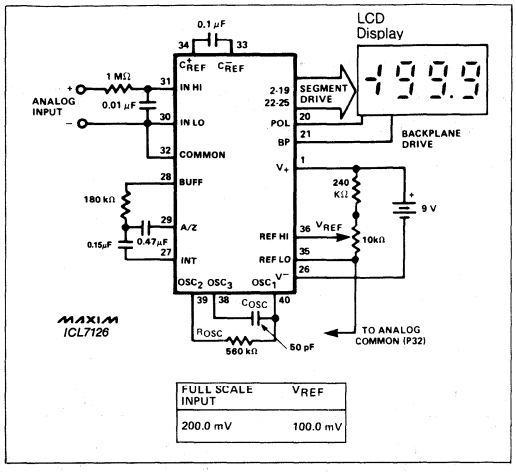


Figure 1. Maxim ICL7126 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

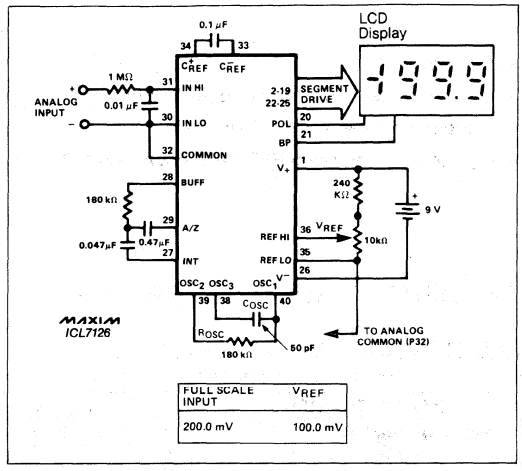


Figure 2. Maxim ICL7126 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

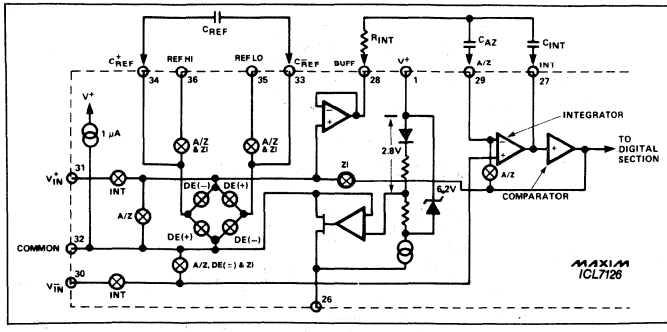


Figure 3. Analog Section ICL7126

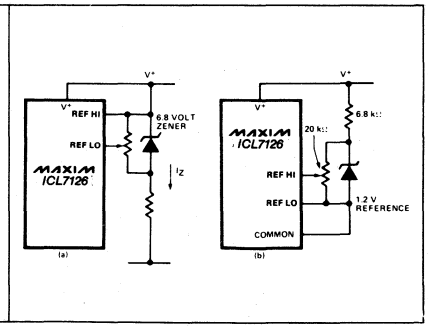


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7126. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

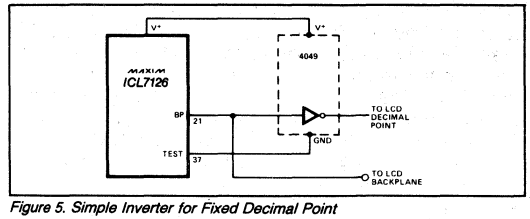


Figure 5. Simple Inverter for Fixed Decimal Point

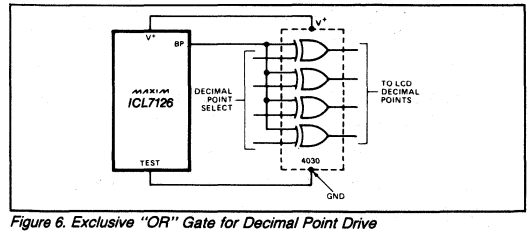


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

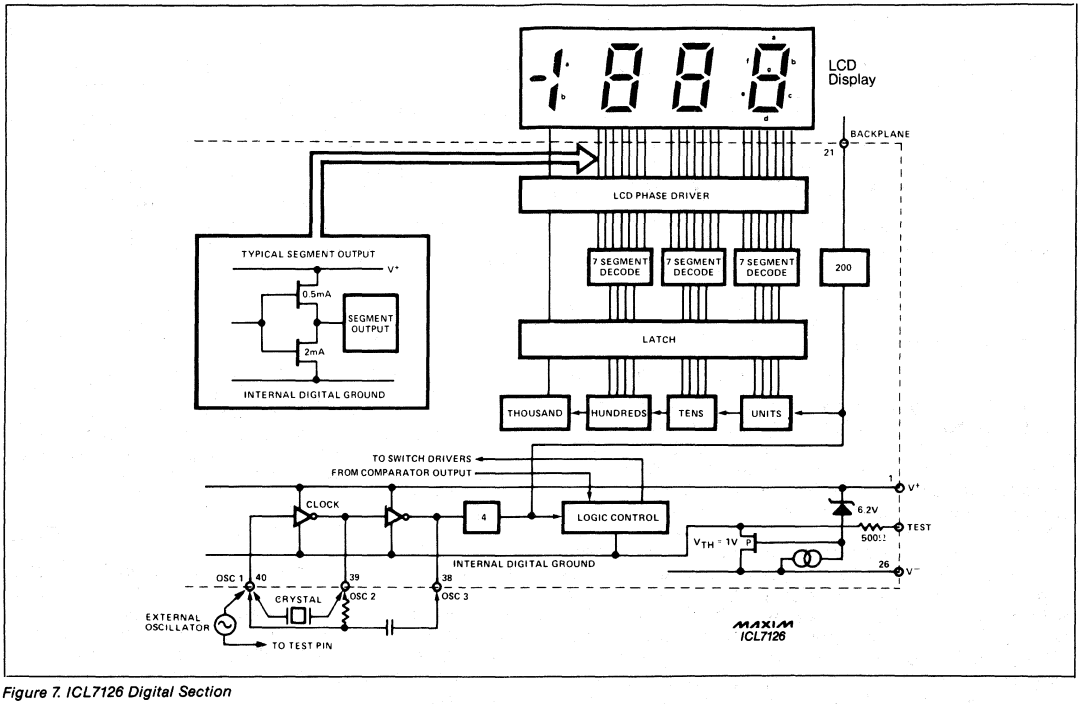


Figure 7. ICL7126 Digital Section

Digital Section

The digital section for the ICL7126 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7126. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7126 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80khZ, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000) clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. While the Maxim ICL7126 will operate with a 0.33μF capacitor, a 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held to half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

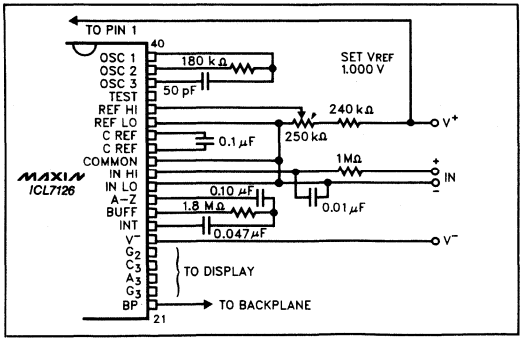


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

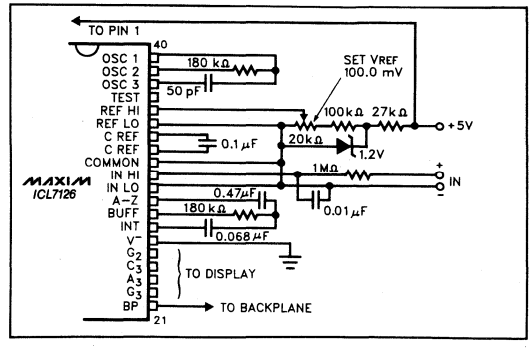


Figure 9. 7126 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V+ and V⁻ is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

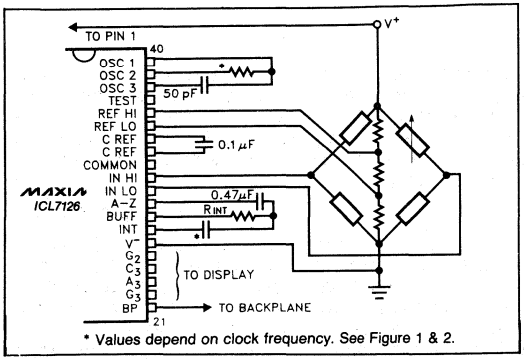


Figure 10. 7126 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

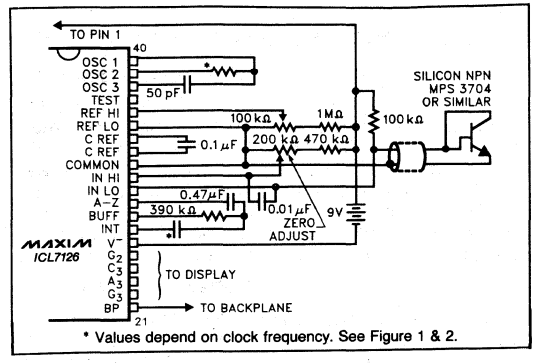
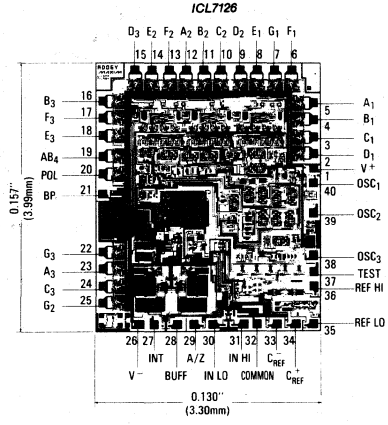


Figure 11. 7126 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/° C/. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography



MAXIM

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

General Description

The Maxim ICL7129A/MAX7129 is a high precision monolithic 4-1/2 digit A/D converter that directly drives a multiplexed liquid crystal display. Using a novel "successive integration" technique, the ICL7129A/MAX7129 has a ±20,000 count resolution on both 2.00000V and 200.00mV ranges. It features high impedance differential inputs, excellent differential linearity, true ratiometric operation and auto polarity. The only external active component required to make precision DVM/DPMs is a reference. The overrange and underrange outputs and the 10:1 range changing input facilitate the design of autoranging systems. The ICL7129A/MAX7129 detects and flags a LOW BATTERY condition and also checks for continuity, giving a visual indication and a logic level output which can be used to generate an audible signal.

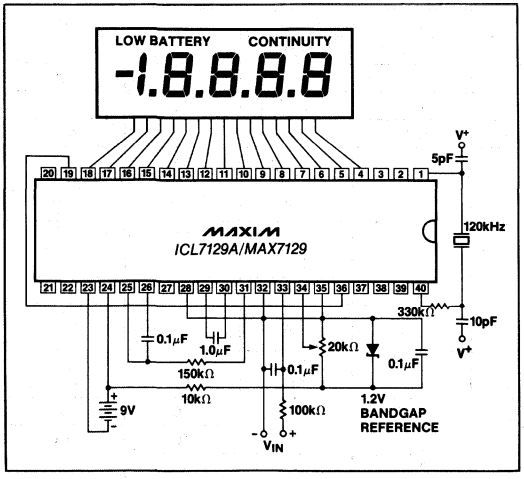
The MAX7129 has a fullscale accuracy of 0.0005%, resolution of 10μV, zero reading drift of 0.5μV/°C, an input bias of 10pA max, and a rollover error of less than 1 count. Maxim has reduced the noise of the ICL7129A to 3μV—significantly lower than the MAX7129.

Applications

This device can be used for a wide range of precision digital voltmeter, multimeter and panelmeter applications. Most applications involve the measurement and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



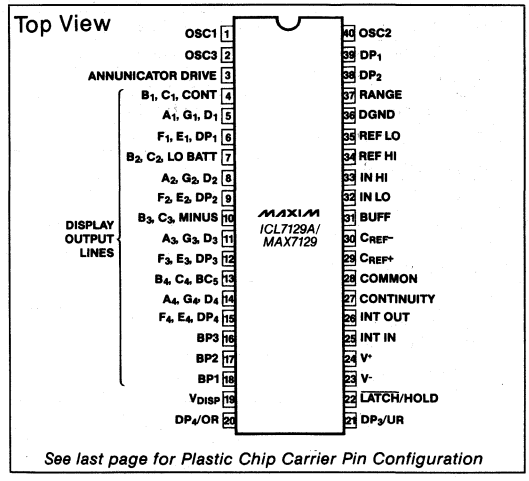
Features

- ±19,999 Count Resolution
- 10pA Max Input Bias Current (MAX7129)
- 3μV peak to peak noise (ICL7129A)
- Onboard Multiplexed LCD Display Driver 4-1/2 Digits, 4 Decimal Points, 3 Annunciators
- Instant Continuity Detector
- Low Battery Detector and Indicator
- Overrange/Underrange Outputs
- Precise 10:1 Range Select
- 10μV Resolution on 200mV Full Scale
- Significantly Improved ESD protection
- Monolithic, Low Power CMOS Design
- Eliminates Need for Compensation Capacitor

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7129CPL	0°C to +70°C	40 Lead Plastic DIP
MAX7129CJL	0°C to +70°C	40 Lead CERDIP
MAX7129CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX7129C/D	0°C to +70°C	Dice
ICL7129ACPL	0°C to +70°C	40 Lead Plastic DIP
ICL7129ACJL	0°C to +70°C	40 Lead CERDIP
ICL7129ACQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7129AC/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND - 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+
Analog Input Pins
25, 29, 30 ..... V^+ to V^-

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Plastic Chip Carrier
(Quad) Package 700mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Soldering Temperature (10 sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX7129)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		µV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	-V_{IN} = +V_{IN} = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		µV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		1 3	10 40	pA pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	µA
DGND Voltage	V^+ to Pin 36	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current			1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate			100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	µA
"Weak Output" Current	Pin 20, 21	0.25	3/3	10	µA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	µA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	µA µA

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS (ICL7129A)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted. Test Circuit without C_c.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		µV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		3.0	(Note 4)	µV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		13 15	20 40	pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	µA
DGND Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.2	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	µA
"Weak Output" Current	Pins 20, 21	0.25	3/3	10	µA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	µA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	µA µA

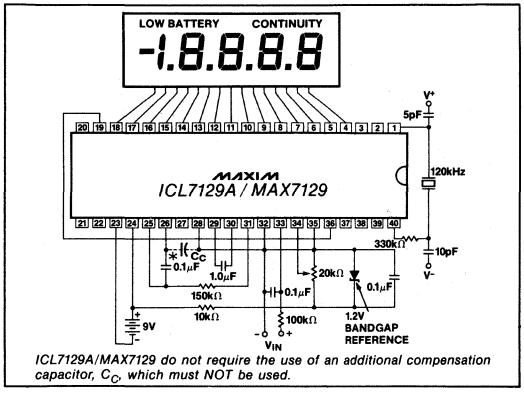
Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Note 3: All pins on Maxim's MAX7129 and ICL7129A are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883, Method 3015.1)

Note 4: The Maxim ICL7129A uses innovative noise reduction techniques to achieve a 3µV noise level. This ensures that for any specific input voltage, the ICL7129A continuously displays one number or fluctuates between two adjacent numbers. In no case will the ICL7129A display three different numbers for a constant input voltage.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver



ICL7129A/MAX7129 do not require the use of an additional compensation capacitor, C_C, which must NOT be used.

Figure 1. MAX7129/ICL7129A Test Circuit

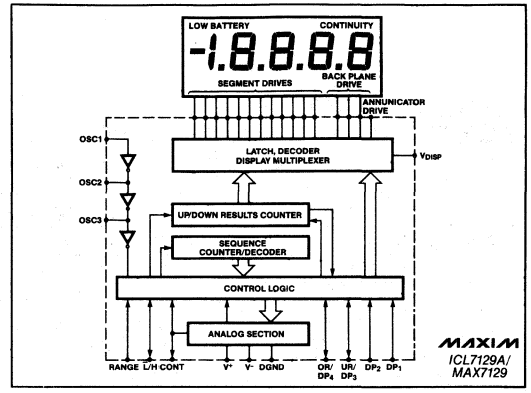


Figure 2. Simplified Block Diagram of MAX7129/ICL7129A Digital Section

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, G_4, D_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative supply for display drivers.
20	DP_4/OR	INPUT: Turns on most significant decimal point when HI. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: When floating, MAX7129/ICL7129 significant decimal point when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{LATCH}$/HOLD	INPUT: When floating, ICL7129 operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used as a converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive supply for display drivers.
25	INT IN	Integrator amplifier input.
26	INT OUT	Integrator amplifier output.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Buffer amplifier output.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input.
35	REF LO	Negative reference voltage input.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. Turns on least significant decimal point when HI.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Table 1. PIN ASSIGNMENTS AND FUNCTIONS

Detailed Description

Conversion Technique

The ICL7129A/MAX7129 differs from earlier integrating A/Ds in two ways. First, it uses a variant of the dual-slope method called "successive integration." Secondly, it uses digital autozeroing rather than an analog autozero loop requiring an external autozero capacitor. Earlier converters stored an offset correction voltage on the autozero capacitor. Although this method worked well for 100μV resolution A/Ds, the autozero loop resulted in greatly increased noise in the earlier generation of integrating A/Ds, making them unsuitable for 10μV resolution systems. The ICL7129A/MAX7129 eliminates the autozero capacitor and the noise associated with the autozero loop by performing two conversions with 5½ digit resolution. The first conversion is performed with the A/D connected to the external inputs, Input HI and Input LO. The second conversion is performed with the A/D inputs internally shorted together. The results of this second conversion, which is proportional to the A/D's offset, is digitally subtracted from the first reading to generate an offset-corrected, autozeroed measurement result.

The ICL7129A/MAX7129 enhances the dual slope conversion technique through multiple dual slope conversions, with each successive conversion having 10 times the resolution of the preceding conversion. The key to this "successive integration" technique is the multiplication of the residual voltage on the integrator capacitor after each conversion. The ICL7129A/MAX7129 first performs a 3½ digit dual slope conversion. The De-integration cycle terminates on the next positive clock edge after the integrator output crosses zero, leaving a small residue of voltage on the integrator capacitor. Unlike other A/D convertors, the ICL7129A/MAX7129 multiplies this residue by a factor of 10, then performs another dual slope conversion. Since the residue on the integrator capacitor has been multiplied by 10 the resolution of the second De-integration cycle is also increased by a factor of 10, and the ICL7129A/MAX7129 achieves 4½ digit resolution during the second De-integration cycle. The integrator capacitor residue left after the second De-integration cycle is again multiplied by 10, and the ICL7129A/MAX7129 performs a third De-integration cycle, this time with 5½ digit resolution.

Figure 2 shows a simplified block diagram of the ICL7129A/MAX7129 digital section. The sequence counter/decoder section keeps track of the many separate phases required for each conversion cycle and provides timing signals to the control logic. The sequence counter runs continuously and is independent of the up/down results counter, which is activated only when the integrator is De-integrating. The data remaining in the results counter at the end of a conversion is latched, decoded and multiplexed to the liquid crystal display.

Figure 3 shows a block diagram of the analog section including all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the conversion cycle. The reference switching and input schemes are very similar to those in other less accurate, integrating A/D converters. A typical waveform on the integrator output is illustrated

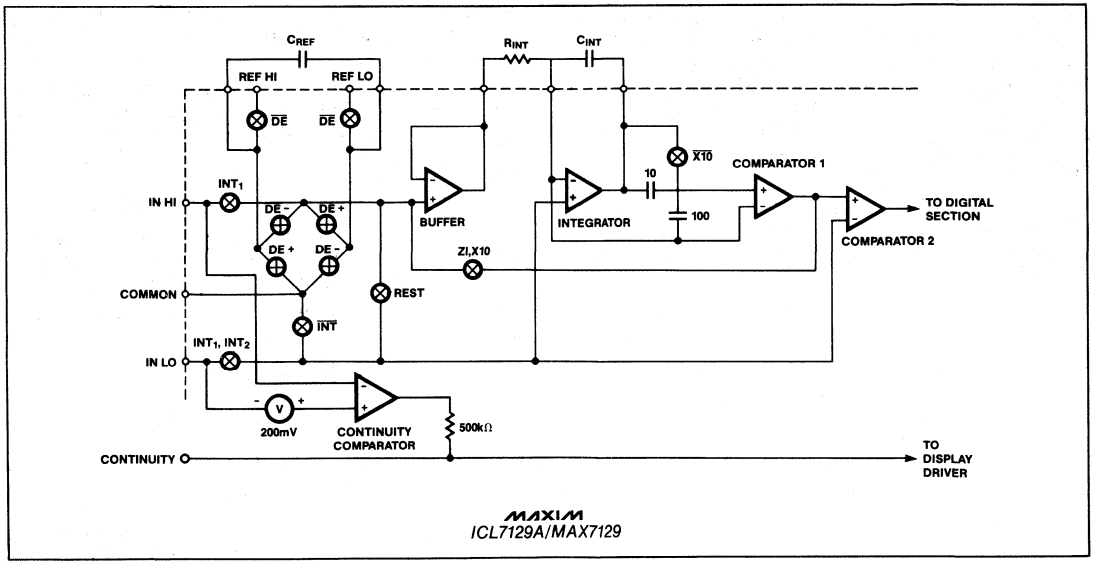


Figure 3. Analog Section Block Diagram

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

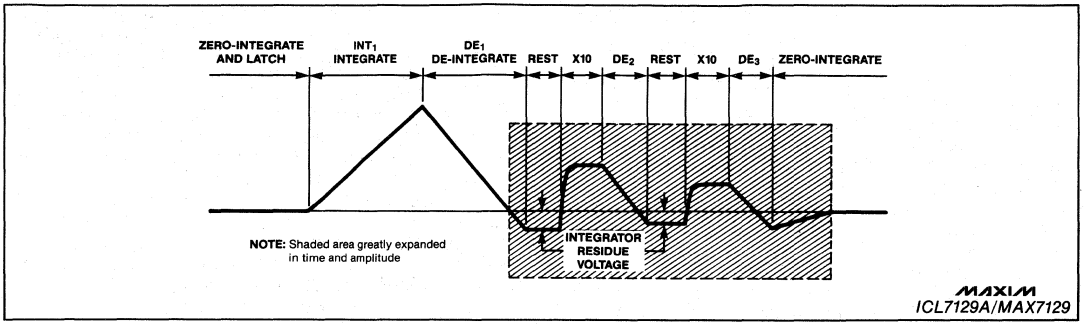


Figure 4. Integrator Waveform for a Negative Input Voltage

in Figure 4. INT_1 refers to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage. In the De-integrate phases, DE_1, DE_2, and DE_3, the reference capacitor is connected to the buffer amplifier and the integrator ramps back down towards Common, the level at which it started integrating. Since the De-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129A/MAX7129 amplifies this overshoot by -10 in the X10 phase and DE_2 begins. Similarly DE_2's overshoot is amplified by -10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This result is obtained by feeding counts to the results counter at the 3½ digit level during DE_1, to the 4½ digit counter during DE_2 and the 5½ digit level during DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted together and subtracting the results from the original reading. The INT_2 switch for this phase is closed so the integrator's common mode voltage is the same as the measurement cycle, thus ensuring excellent CMRR. The data in the up/down results counter at the end of the conversion cycle, accurate to 0.005% of full scale, is sent to the onboard display driver for decoding and multiplexing.

Digital Section

Oscillator and Clock Generator

The ICL7129A/MAX7129 has an oscillator suitable for either crystal or RC operation. The oscillator's output is internally divided by two to generate a system clock with a precise 50% duty cycle. All references to clock cycles in this data sheet refer to the system clock, which is half the frequency of the oscillator.

The crystal oscillator shown in Figure 5A is recommended for most applications. The crystal frequency should be 120kHz for maximum normal mode rejection at 60Hz, and 100kHz for maximum normal mode rejection at 50Hz.

Since an RC oscillator has more short term frequency jitter than a crystal oscillator, a crystal oscillator should be used for 4½ digit, 10μV resolution measurements.

The RC oscillator shown in Figure 5B is adequate for low resolution applications, (3½ digits at 100μV resolution). The capacitor value should be 51pF for all frequencies, and the resistor value calculated from $f_{OSC} = 0.45/RC$.

Sequence Counter and Control Logic

This section provides the signals that control the operation of the analog section. The comparator output is the only input from the analog to the digital

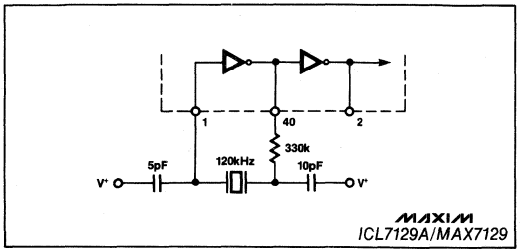


Figure 5A. Crystal Oscillator Circuits

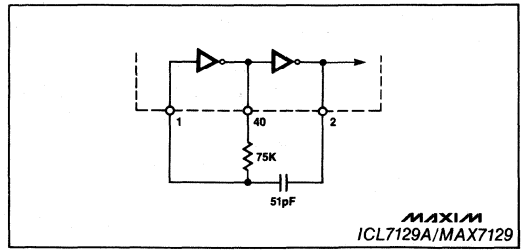


Figure 5B. RC Oscillator Circuit

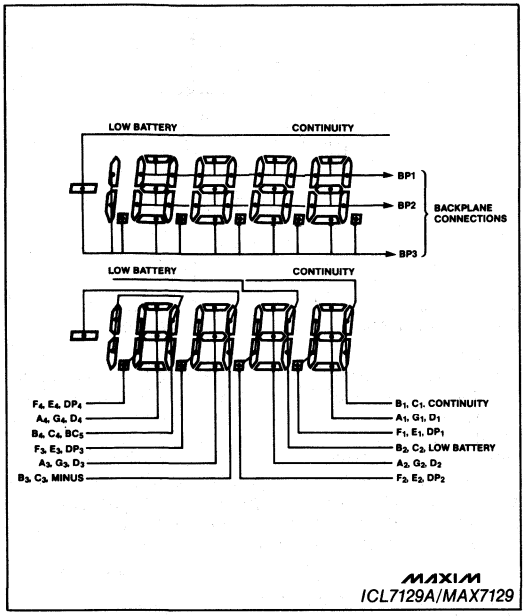


Figure 6. Triplexed Liquid Crystal Display Layout

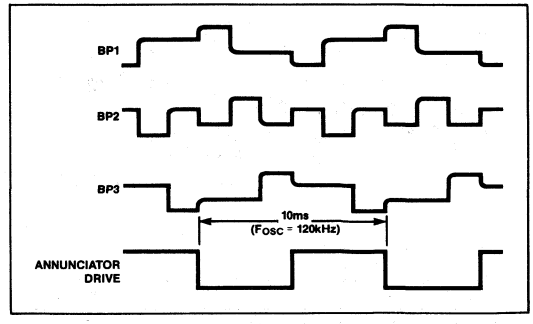


Figure 7. Backplane and Annunciator Drive Waveforms

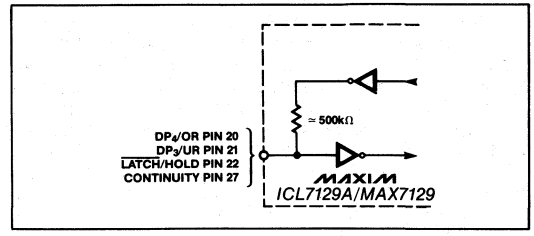


Figure 8. "Weak Output" Digital I/O Pins

section. The digital section uses the comparator output to determine the polarity of the integrator's output and to gate clock counts into the Up/Down Results Counter. The control logic also responds to the external digital inputs: Range, Hold, and Continuity. It also generates the digital outputs: Overrange, Underrange, Latch, and Continuity.

Display Driver

The ICL7129A/MAX7129 can be used to drive a triplexed liquid crystal display with three backplanes. In addition to driving 4½—7 segment digits, the ICL7129A/MAX7129 can directly drive the decimal points, polarity sign, "Continuity," and "Low Battery" annunciators. Figure 6 shows the assignment of the 36 display segments to the three backplanes and 12 segment drive lines. The ICL7129A/MAX7129 divides the oscillator frequency by 1200 to generate the backplane frequency, resulting in a backplane frequency of 100Hz with a 120kHz oscillator crystal or 83.3Hz with a 100kHz crystal. Figure 7 shows the backplane and annunciator output waveforms.

Range Input

With a 1V reference, the ICL7129A/MAX7129 has a 2V full scale when the Range input is high and a 200mV full scale when the Range input is low or open. The ICL7129A/MAX7129 achieves a precise 10:1 change in scale factor by reducing the integration period from 10,000 clock cycles on the 200mV range to 1000 clock cycles on the 2V range.

Digital I/O Pins

Four of the ICL7129A/MAX7129's pins are quasi-directional and can be used as either inputs or outputs. As shown in Table 1, DP4/OR, DP3/UR, Latch/Hold, and Continuity each have dual input/output functions. Figure 8 shows a simplified schematic of these input/output pins. Since there is approximately 500kΩ in series with these outputs, they can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. Since the output drive current is limited to only a few microamps, the outputs are easily overdriven by 4000 series CMOS when the pin is used as an input.

Latch/Hold

The Latch/Hold pin puts out a low-going pulse during the last 100 clock cycles of each conversion. This low-going pulse latches the conversion data into the onboard display driver section. The ICL7129A/MAX7129 will not update the display, and the display will continue to show the previous reading if the Latch/Hold pin is held high. If the Latch/Hold pin is held low, the display latches are transparent and the counting of the sequence counter can be observed during the de-integrating phases.

OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are valid on the falling edge of Latch/Hold and remain in that state until the end of the next conversion cycle.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

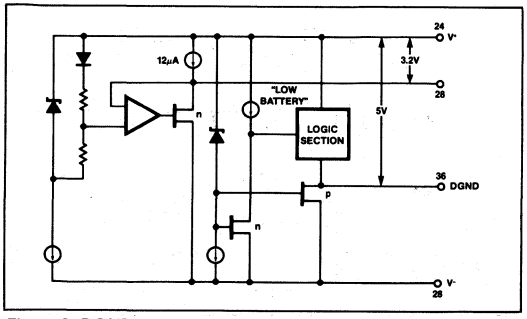


Figure 9. DGND and Common Outputs

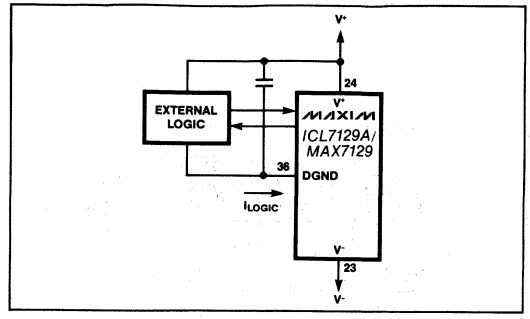


Figure 10. Using DGND as Supply Voltage for External Logic

Overrange and Underrange Outputs

The DP4/OR (Decimal Point 4/Overrange) output goes high if the measurement result is greater than ±19,999. Similarly, the DP3/UR (Decimal Point 3/Underrange) output goes high if the measurement result is less than ±1000. These signals are updated at the end of each conversion, unless Latch/Hold is held high. These pins are also inputs that control the decimal points, DP3 and DP4. A high level input on these pins turns on the decimal point segments of the display. If these decimal points are not required, they can be used as logic level controlled annunciators.

Continuity

An internal comparator with a 200mV threshold is connected directly between the INPUT HI and INPUT LO pins of the ICL7129A/MAX7129 (see Figure 3). The Continuity output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This activates the Continuity annunciator on the display. The Continuity annunciator can also be controlled by an external source if desired, since the Continuity pin is one of the four quasi-bidirectional pins of the ICL7129A/MAX7129. A pull-down resistor connected between Continuity and DGND (pin 36) disables the continuity function when it is not desired.

Analog Section

Common, Digital GrouND, and Low Battery

Figure 9 shows how the Common and DGND (Digital GrouND) outputs of the ICL7129A/MAX7129 are generated from internal zener diodes. Common can be used to set the common mode voltage in applications where the input signals float with respect to the ICL7129A/MAX7129's power supplies, which is typical for battery powered applications. Common can also function as a pre-regulator for an external precision reference voltage source.

The voltage between V^+ and DGND is the internal supply voltage for the logic section of the ICL7129A/MAX7129. Both Common and DGND are capable of sinking current from external loads, but care should be taken to ensure that these outputs are not overloaded. The connection of external logic circuitry to the ICL7129A/MAX7129 is shown in Figure 10. This connection will work provided that the supply current requirements of the logic do not exceed the 1.2mA current sink capability of the DGND pin. The buffer in Figure 10 can be used to keep the loading on DGND to a minimum if more supply current is required. COMMON can source approximately 12μA whereas DGND has no source capability.

Low Battery

The "Low Battery" annunciator of the display turns on when the supply voltage between V^+ and V^- drops below 7.2V. The exact point at which this occurs is determined by the 6.3V zener diode and threshold voltage of the n-channel transistor connected to the V^- rail shown in Figure 9.

Buffer

The ICL7129A/MAX7129 buffer has a common mode input voltage range of V^- + 1.5V to V^+ - 1.0V and can supply up to 20μA of output current.

Integrator

The integator can swing to within 0.3V of the supply rails while delivering 20μA of output current. It should also be noted that, unlike the ICL7129, Maxim's ICL7129A/MAX7129 provides stable operation without the need for an additional capacitor between the Integrator Output and Common pins. The compensation cap used with the ICL7129 must be omitted for correct operation of the ICL7129A/MAX7129.

X10 Amplifier

The X10 ("times ten") amplifier provides a precise gain of -10, without using any external components. This amplifier, unique to the "successive integrator" A/D, is used to multiply the residue left on the integrator capacitor after the DE_1 and DE_2 phases.

Comparator

The comparator has the high gain and bandwidth needed to rapidly detect zero crossing. The comparator's output is used by the digital control logic to select the correct polarity for De-integration, and to gate clock pulses into the up/down results counter during the De-integration phases.

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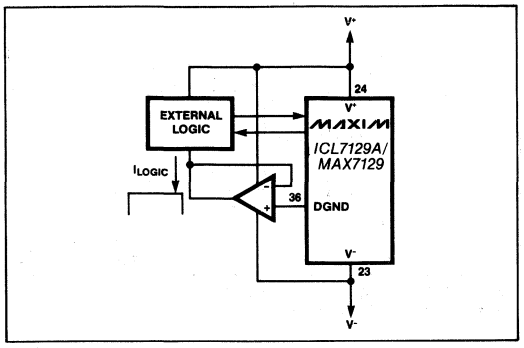


Figure 11. DGND Buffer

Component Selection

Integrating Resistor

Optimum linearity is obtained by choosing the integrating resistor value is chosen so that the buffer's maximum output current is between 5 and 20μA. The quiescent current of the buffer is 70μA, and can supply 13μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the optimum value of integrating resistor can be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{13\mu A} = \frac{2V}{13\mu A} = 150k\Omega$$

Too high a value for the integrating resistor increases the sensitivity to noise pickup and increases errors caused by stray leakage currents. Too low a value degrades integral linearity by attempting to draw more current from the buffer and integrator than they can provide without degrading linearity.

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as

$$Vswing = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

where $I_{INT} = 13\mu A$ if R_{INT} is chosen as described above and T_{INT} = 1,000 clock periods (16.7ms for 120kHz oscillator frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. The integrator will not saturate unless its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. Since Common is a approximately 3V below V^+, the integrator swing should be 2V. Substituting these values in the above formula, C_{INT} can now be calculated as:

$$C_{INT} = \frac{13.3\mu A \times 16.7ms}{2V} = 0.1\mu F$$

Too low a value for C_{INT} increases integrator swing to the point where the integrator saturates and causes integral linearity errors. Too high a value for C_{INT} reduces the integrator swing range and increases the effect of comparator noise. If a positive common mode voltage is applied to IN LO the value of C_{INT} must be reduced to keep the integrator output voltage at least 1V below V^+.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the Input HI is a good indication of the amount of dielectric absorption in the integrator capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon™ capacitors. In less critical applications polystyrene and polycarbonate capacitors may also be used.

Reference Capacitor

The reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are required only where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in digital multimeters.

The reference capacitor must be a low leakage capacitor since it stores the reference voltage while floating during both the Integrate and De-integrate phases. Any leakage or charge loss during these phases causes a change in the scale factor of the ICL7129A/MAX7129. Low cost film capacitors such as polyester or polystyrene are suitable for most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. In most applications the Ref Lo Input terminal is connected to Common, and the Ref Hi Input is 1V above Common. During the integration and idle phases the reference capacitor is connected to the Reference Inputs (C_{REF}^+ to Ref Hi and C_{REF}^- to Ref Lo). At the end of the integration phase the comparator determines the polarity at the integrator output and the digital section closes analog switches so that the reference capacitor is connected to Common and the buffer input with a polarity such that the integrator output will return toward Common during the De-integrate phase. A negative input signal during the integrate phase drives the integrator output positive and the ICL7129A/MAX7129 digital section will connect the C_{REF}^- terminal to Common during the De-integrate phase. Since the C_{REF}^- terminal was also connected to Common during the Integrate phase, the C_{REF} terminals do not change voltage during the transition from Integrate phase to De-integrate phase. If, however, the input voltage during the Integrate phase is positive, the ICL7129A/MAX7129 digital section will connect the Ref Cap^+ terminal to Common. In

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

this case the two terminals of the reference capacitor both move 1V more negative. Any stray capacitance on the reference capacitor terminals must also be charged during the 1V movement, thereby reducing the voltage on the reference capacitor and changing the scale factor for positive input voltages. This error, called "rollover error" can be reduced to less than 1 count by using a reference capacitor value of 1μF or greater.

Crystal Oscillator Components

The ICL7129A/MAX7129 crystal oscillator is designed to work with tuning fork type crystals such as the Statek CX-1V series. The two capacitors are not critical components and can be the low cost disc ceramic type. The crystal frequency should be 120kHz to reject 60Hz normal mode signals and 100kHz to reject 50Hz normal mode signals. With these crystal frequencies the integration will be 10 cycles of the 60/50Hz signal on the 200mV range and 1 cycle on the 2V range. There is no single oscillator frequency that results in good normal mode rejection of both 50Hz and 60Hz on the 2V range, but a 100kHz oscillator frequency will reject both 50Hz and 60Hz on the 200mV scale.

Component Manufacturers

The following list of component suppliers is intended to be of assistance in identifying suitable external components for use with the ICL7129A/MAX7129. The list is not intended to be comprehensive, nor does it constitute an endorsement by Maxim of the companies listed.

Triplexed Liquid Crystal Displays

Epson America, Inc., Torrance, CA.
(213) 534-4500
Part #: LD-H7960A

Crystaloid, Inc., Hudson, OH
(216) 655-2429

Hamlin, Inc., Lake Mills, WI
(414) 648-2361

UCE, Inc., Norwalk, CT
(203) 838-7509

LXD INC, Cleveland, OH
(216) 292-3300
Part #: 353E3/8R03H

Varitronix Limited, Los Angeles, CA
(213) 661-8883
Part #: VIM-503-DP

Display Mounting Bezels

Techknits, Inc., Cranford, N.J.
(201) 272-5500

Conductive Rubber Technology, Santa Barbara, CA.
(805) 969-5807

Crystals

Statek, Inc., Orange, CA
(714) 639-7810
Part #: CX-1V 120C

Saronix, Inc., Palo Alto, CA
(415) 856-6900

Polypropylene Capacitors

West Lake Capacitors, West Lake Village, CA
(818) 889-4120

Seacor, Inc., Westwood, N.J.
(201) 666-5600

TRW Capacitors, Ogallala, NE
(308) 284-3611

Sprague Electric Co., North Adams, MA
(413) 664-4411

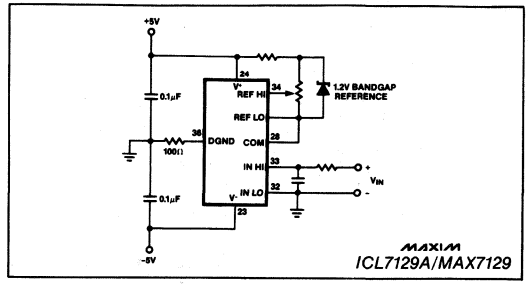


Figure 12. Powering the ICL7129A/MAX7129 from +5V and -5V Power Supplies

Applications

Power Supply

The ICL7129A/MAX7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies.

The standard battery connection using a 9V battery is shown in the Typical Operating Circuit on the front page of this data sheet.

Figure 12 shows the power connection for systems with +5V and -5V supplies. Note that measurements are given with respect to ground. COMMON is not connected to INPUT LO and is used only as a pre-regulator for the external voltage reference. Digital ground of the ICL7129A/MAX7129 (DGND, pin 36) is not directly connected to power supply ground. The ICL7129A/MAX7129's digital inputs have protective diodes to DGND and should not be driven to any voltage below DGND. This problem is handled by placing a 100Ω resistor between the ICL7129A/MAX7129's DGND terminal and the ±5V system's digital ground, which pulls down the ICL7129A/MAX7129's DGND terminal if it reaches a voltage more positive than the ±5V system's digital ground. This prevents the forward biasing of the input protection diodes. If DGND voltage is more negative than the system digital ground the 10Ω resistor will limit the amount of current that DGND sinks.

A power supply with single polarity can be used to power the ICL7129A/MAX7129 in applications where battery operation is not convenient or appropriate. Measurements must be made with respect to COMMON or some other voltage within the ICL7129A/MAX7129's input common mode range.

Voltage References

The Common output has a typical temperature coefficient of ±80ppm/°C. Since the ICL7129A/MAX7129 has a resolution of 1 count in 20,000 or 50ppm, a precision external reference is needed unless the ambient temperature is held constant. The diagram of the Typical Operating Circuit on the front page of this data sheet shows a 1.2V bandgap voltage source used as the reference for the ICL7129A/MAX7129, with Common used only as a pre-regulator for the bandgap

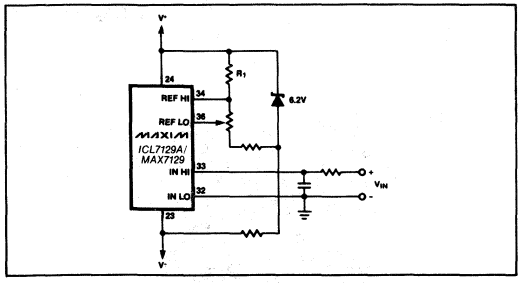


Figure 13. Using a 6.2V Reference Diode with the ICL7129A/MAX7129.

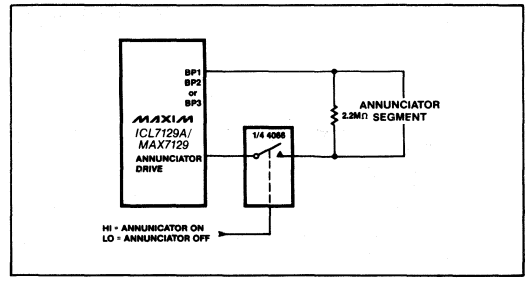


Figure 14. Externally Controlled Annunicators

reference. The ICL7129A/MAX7129 reference voltage is approximately 1.000V for both 2V and 200mV full-scale operation. To trim the reference voltage, first apply a precision 1000.05mV input voltage, then adjust the reference voltage until the display reading alternates equally between 10000 and 10001.

Figure 13 shows the ICL7129A/MAX7129 with an external 6.8V zener reference voltage.

Annunciator Drivers

The Annunciator Drive output is a square wave at the backplane frequency, swinging from V^+ to V_{DISP}. Any segment connected to Annunciator Drive will be turned on, regardless of which backplane drives that segment. Figure 14 shows how to control annunciator segments with external logic levels.

Display Voltage Compensation

An adequate display can be obtained in most applications by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is expected, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers usually specify the temperature variation of the LCD threshold voltage, which is approximately 1/3 of the optimum peak display voltage. The peak display voltage is equal to ($V^+ - V_{DISP}$), so a typical −4mV/°C temperature coefficient of an LCD threshold corresponds to a +12mV/°C temperature coefficient at the V_{DISP} pin. Two circuits that can be adjusted to give a temperature compensation of approximately +12mV/°C at V_{DISP} are shown in Figure 15. The diode between DGND and V_{DISP} should have a low turn-on voltage to ensure that V_{DISP} is never driven more than 300mV negative with respect to DGND.

Input Protection

The input pins of the ICL7129A/MAX7129 have protection diodes built in to protect it from electrostatic discharges (ESD) of up to 2000V (Mil Standard 883, Method 3015.1 test circuit). These diodes also protect the ICL7129A/MAX7129 from excessive input voltage overload in multimeter circuits, provided that the current into these diodes is limited to less than 1mA. The ICL7129A/MAX7129 will therefore be fully protected for input voltages up to 1000V if the input current limiting resistor is 1MΩ.

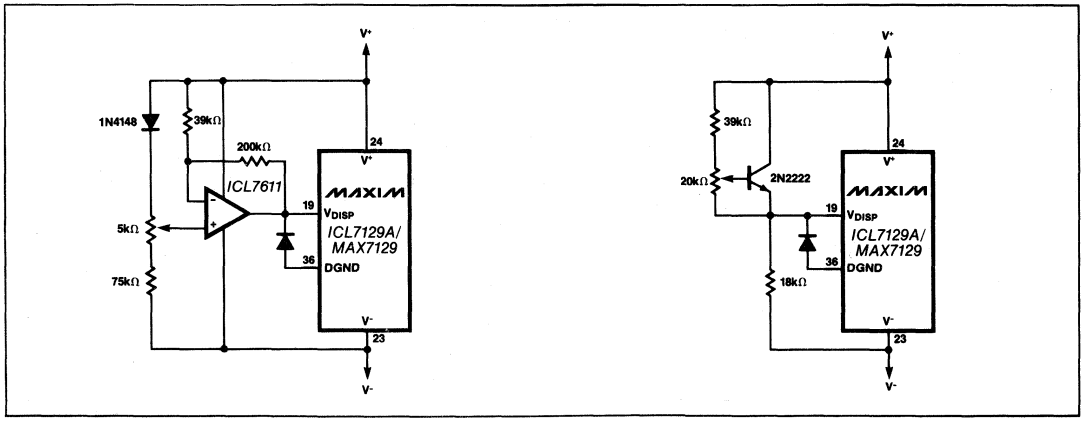
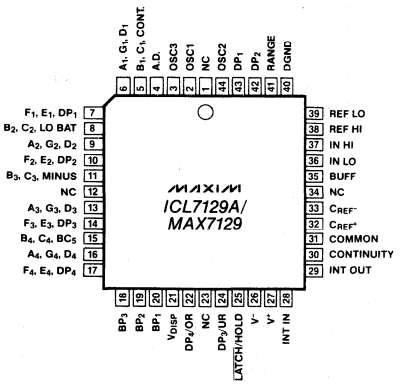


Figure 15. V_{DISP} Temperature Compensation

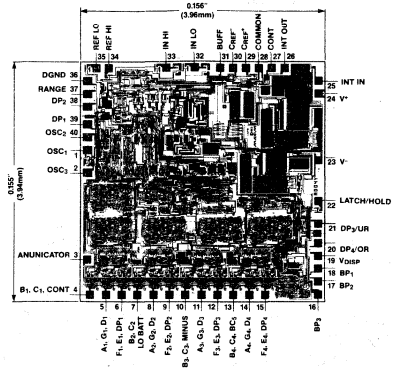
4-1/2 Digit Single-Chip A/D Converter with LCD Driver

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



Substrate is Connected to V+.

MAXIM

4½ Digit A/D Converter with Multiplexed BCD Outputs

General Description

The Maxim ICL7135 is a high precision monolithic 4½ digit A/D converter. Dual slope conversion reliability is combined with ±1 in 20,000 count accuracy and a 2.0000V full scale capability. It features high impedance differential inputs, nearly ideal differential linearity, true ratiometric operation, auto zero and auto-polarity. The multiplexed BCD outputs and digit drivers provide easy interface to external display drivers like the Maxim ICM7211A. The only other external components needed to make precision DVM/DPMs are a reference and a clock. For more complex systems the BCD outputs are enhanced by STROBE, OVERRANGE, UNDERRANGE, RUN/HOLD and BUSY lines providing easy interface to microprocessors and UARTs. This interfacing capability makes the ICL7135 an ideal device for use in microprocessor based data acquisition and control systems.

The ICL7135 has auto-zero accuracy better than 10μV, zero drift of 0.5μV/°C, input bias current of 10pA max. and rollover error of less than 1 count.

Features

- **Improved 2nd Source (See our "Maxim Advantage™" Page 3)**
- **±20,000 Count Resolution**
- **Guaranteed ±1 Count accuracy**
- **Over-range, under-range signals for auto-range capability**
- **Easy interface to UARTs and μPs**
- **TTL compatible, Multiplexed BCD outputs**
- **True differential input. Zero reading guaranteed for 0 volt input**
- **True polarity at zero for precise null detection**
- **Monolithic CMOS design**

Applications

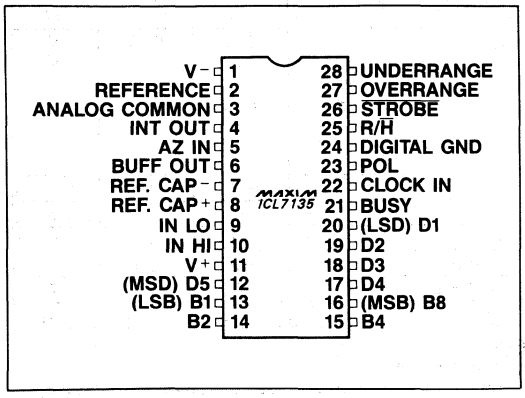
This device is used in a wide range of measurement applications involving the manipulation and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

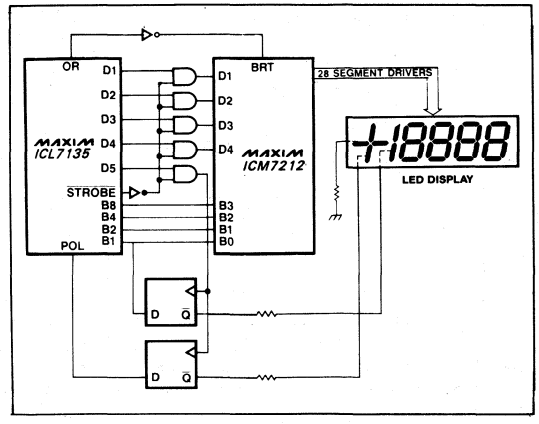
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to 70°C	28 Lead CERDIP
ICL7135CPI	0°C to 70°C	28 Lead Plastic DIP
ICL7135CQI	0°C to 70°C	28 Lead Plastic chip carrier
ICL7135C/D	0°C to 70°C	Dice

Pin Configuration



Typical Operating Circuit



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit A/D Converter with Multiplexed BCD Outputs

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- CERDIP Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Supply Voltage V+ ..... +6V
V− ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Gnd to V+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG (Note 1) (Note 2)		Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
		Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full Scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0° \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	 $V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V mA μA
	OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5 BUSY, STROBE OVER-RANGE, UNDER-RANGE POLARITY	V_{OL} V_{OH} V_{OH}	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$ $I_{OH} = -10\mu A$	 2.4 4.9	0.25 4.2 4.99	0.40	V V V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	$f_c = 0$		1.1	3.0	mA
		−5V Supply Current	I^-	$f_c = 0$		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

4½ Digit A/D Converter with Multiplexed BCD Outputs

- **Guaranteed 2mA Max Supply Current**
- **Key Parameters Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Low Noise**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

	Characteristics	Symbol	Conditions	Min	Typ	Max	Units
ANALOG	**Zero Input Reading**		**V_{IN} = 0.0V, Full Scale = 2.000V $0° \le T_A \le +70°C$**	**−0.0000**	**±0.0000**	**+0.0000**	**Digital Reading**
ANALOG	**Ratiometric Reading (Note 2)**		$V_{IN} = V_{REF}$, Full Scale = 2.000V $T_A = 25°C$ **$0° \le T_A \le +70°C$**	+0.9998 **+0.9995**	+0.9999 **+0.9999**	+1.0000 **+1.0005**	**Digital Reading**
ANALOG	Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
ANALOG	Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
ANALOG	Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} = +V_{IN} \approx 2V$		0.5	1	Digital Count Error
ANALOG (Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	V_{IN} = 0V, Full Scale = 2.000V		15		μV
ANALOG (Note 1) (Note 2)	**Leakage Current at Input**	**I_{ILK}**	V_{IN} = 0V $T_A = 25°C$ **$0° \le T_A \le +70°C$**		1	10 **250**	pA **pA**
ANALOG (Note 1) (Note 2)	Zero Reading Drift		V_{IN} = 0V $0° \le T_A \le +70°C$		0.5	2	μV/°C
ANALOG (Note 1) (Note 2)	Scale Factor Temperature Coefficient (Note 3)	TC	V_{IN} = +2V $0° \le T_A \le +70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	$0° \le T_A \le +70°C$ $0° \le T_A \le +70°C$ V_{IN} = 0 $0° \le T_A \le +70°C$ V_{IN} = +5V $0° \le T_A \le +70°C$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V V mA μA
DIGITAL OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OL} V_{OH}	I_{OL} = 1.6mA I_{OH} = −1mA	 2.4	0.25 4.2	0.40	V V
DIGITAL OUTPUTS	BUSY, $\overline{STROBE}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
DIGITAL SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
DIGITAL SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
DIGITAL SUPPLY	**+5V Supply Current**	**I^+**	**f_C = 0 $T_A = 25°C$ $0° \le T_A \le +70°C$**		**1.1**	**2.0 3.0**	**mA mA**
DIGITAL SUPPLY	**−5V Supply Current**	**I^-**	**f_C = 0 $T_A = 25°C$ $0° \le T_A \le +70°C$**		**0.8**	**2.0 3.0**	**mA mA**
DIGITAL SUPPLY	Power Dissipation Capacitance	C_{PD}	(Note 5)		40		pF
CLOCK	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The Temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Clock Frequency" below for limitations on the clock frequency range in a system.

Note 5: +5V Supply current for $f_C \neq 0$ is $I^+ = I^+_{(f_C = 0)} + C_{PD} \times 5V \times f_C$.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

4½ Digit A/D Converter with Multiplexed BCD Outputs

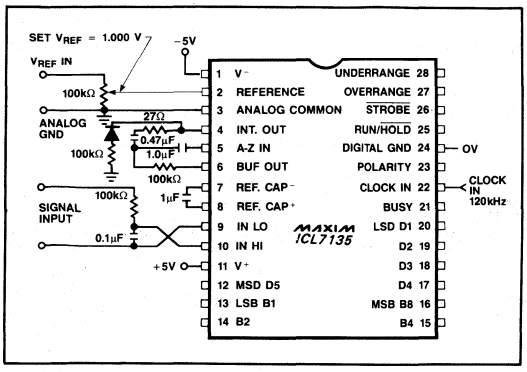


Figure 1. ICL7135 Test Circuit

Detailed Description

General Operation

The ICL7135 is divided into an Analog section and a Digital section. The digital section includes the counters, input and output interfaces, and control logic which controls the timing of each measurement cycle. Each measurement is divided into four phases: 1) auto-zero (AZ), 2) signal integrate (INT), 3) reference deintegrate (DE), and 4) zero integrator (ZI). The digital section controls the operation of the analog section during each of these phases, using counters and the state of the comparator to determine when to start each of the four phases.

Auto-Zero Phase

During auto-zero Input HI and Input LO are disconnected from the input pins and are internally shorted to Analog COMMON. The output of the comparator is connected to the inverting input of the Integrator, and at the same time the non-inverting input of the integrator is connected to the input of the buffer. This feedback loop charges the autozero capacitor, C_{AZ}, to compensate for the offset voltages of the buffer amplifier, integrator, and comparator. Also during auto-zero, the reference capacitor is connected to the voltage reference and is charged to the reference voltage. The auto-zero cycle is a minimum of 9800 clock cycles, except after an over-range reading. After an over-range, the extended zero integrate phase reduces the auto-zero phase to 3800 clock cycles.

Signal Integrate Phase

At the end of the auto-zero phase the auto-zero loop is opened, and the Input High and Input Low are switched to the external pins IN-HI and IN-LO. The analog section integrates the differential voltage between Input High and Input Low. The differential voltage must be within the ICL7135's common mode range. The voltage on the integrator capacitor at the end of signal integrate is directly proportional to the differential voltage between Input High and Input Low, and is also directly proportional to the length of the signal integrate phase. The signal integrate phase lasts precisely 10,000 clock cycles. At the end of this phase the input signal polarity is determined.

De-Integrate Phase

At the end of signal integrate, Input High and Input Low are disconnected from the external pins. The integrator non-inverting input pin is then internally connected to Analog Common and the buffer input is connected to one side of the reference capacitor. The other side of the reference capacitor is connected to Analog Common. The polarity at the output of the integrator (as detected by the comparator at the end of signal integrate phase) determines which terminal of the reference capacitor is connected to the buffer input. The reference capacitor polarity is chosen so that the integrator output will always return towards Analog Common. Since the reference capacitor was charged to the reference voltage during the auto-zero phase, the integrator input voltage is now the reference voltage. The De-Integrate phase lasts for 20,001 counts, or until the comparator detects that the integrator output has crossed zero, whichever occurs first. The time required to return to zero is proportional to the input signal and is inversely proportional to the reference voltage. The number of clock cycles required to return to zero is counted by the digital section and is latched as the measurement result.

$$\text{Displayed reading} = 10{,}000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

The last of the four phases is the zero integrator phase. The non-inverting input of the integrator is internally shorted to Analog Common and the buffer input is internally connected to the output of the comparator. This closes a loop that forces the integrator output to zero. Normally this phase lasts only 100 to 200 counts, sufficient time to remove the small residual charge on the integrator capacitor caused by the comparator delay and the one count delay created by sampling the comparator output only once per clock cycle. However, an overrange condition will exist when the integrator output does not return to zero by the end of the De-Integrate phase, and can leave a residual voltage on the integrator capacitor. In this case, the Zero Integrator phase is increased to 6200 counts to ensure that the integrator capacitor is fully discharged before the next measurement cycle is started.

Analog Section

Analog COMMON

Analog COMMON is the Analog ground reference for the ICL7135. If Input Low is at a voltage other than Analog

4½ Digit A/D Converter with Multiplexed BCD Outputs

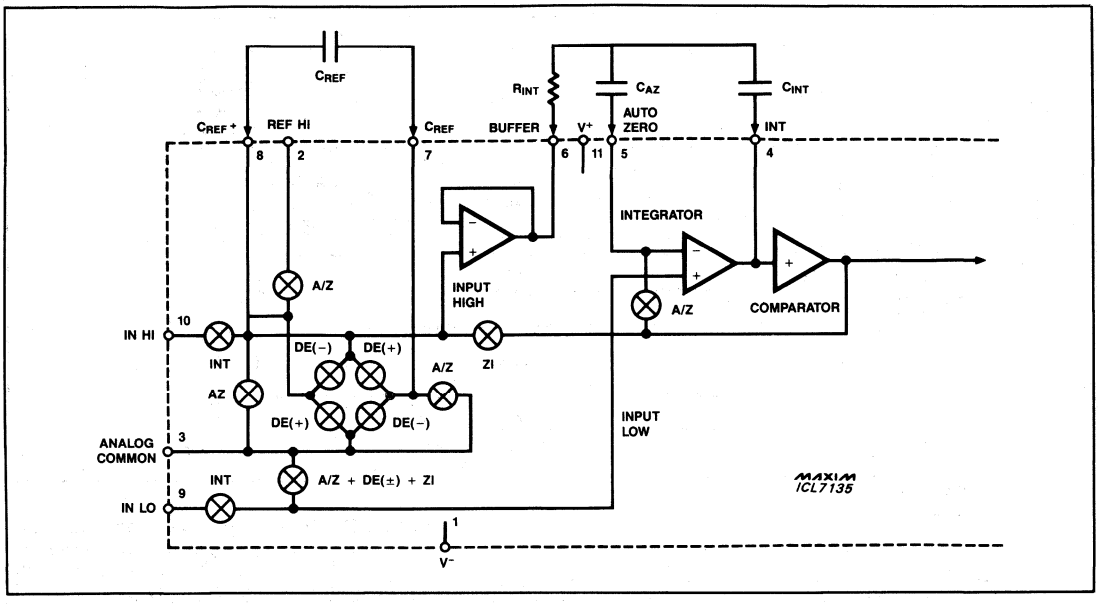


Figure 2. Analog Section of ICL7135

COMMON a common mode voltage will be introduced and, although the ICL7135 has an excellent CMRR, Input Low and Analog COMMON should be connected together whenever possible. Analog COMMON is also the reference point for the reference voltage. The Analog Common voltage is normally connected to the system ground when using ±5V supplies. When the ICL7135 is operated from a single supply voltage the Analog Common should be connected to a voltage source approximately halfway between V^+ and ground.

Input Buffer

The ICL7135 input buffer is a CMOS buffer with a common mode input voltage range of approximately V^+–1.0V to V^-+1.5V. The quiescent current is approximately 100μA and the buffer can deliver up to 40μ of output current with excellent linearity.

Integrator

The integrator amplifier, similar to the buffer amplifier, can deliver 20μA of output current with high linearity while swinging to within 0.3V of either supply rail. The integrator's non-inverting terminal is connected to IN LO during the signal integrate phase, so the voltage on the IN LO terminal sets the starting point for the integrator output during signal integrate. If IN LO is at a voltage other than ground, this will limit the maximum allowable swing at the integrator output, and the value of the integrating capacitor should be increased. (Refer to Component Selection)

Comparator

The comparator monitors the voltage on the integrator capacitor during deintegrate. The digital section samples the comparator output once per clock cycle and terminates the deintegrate cycle when the comparator changes its state as the integrator voltage passes through zero. The offset voltage of the comparator is not critical since the auto-zero phase compensates for the offset. The output of the comparator is the only output from the analog section to the digital section.

Digital Section

As shown in Figure 3, the digital section consists of counters, latches, output multiplexer, and control logic. The control logic monitors the counters and the comparator to determine the start of each phase, and sends control signals to the analog section to drive the analog switches to the proper state for each measurement phase. The control section also responds to the external input, RUN/$\overline{\text{HOLD}}$, and creates the control outputs; OVERRANGE, UNDERRANGE, BUSY, and $\overline{\text{STROBE}}$.

RUN/$\overline{\text{HOLD}}$

When RUN/$\overline{\text{HOLD}}$ is high or open the ICL7135 will continuously perform conversions with each measurement being 40,002 clock cycles long. When RUN/$\overline{\text{HOLD}}$ goes low, the ICL7135 will complete the measurement in progress then remain in the auto-zero cycle, holding the last reading. If RUN/$\overline{\text{HOLD}}$ goes high after the maximum period assigned to deintegrate, a new conversion will start, with a delay of 1 to 10,001 clock cycles between the

4½ Digit A/D Converter with Multiplexed BCD Outputs

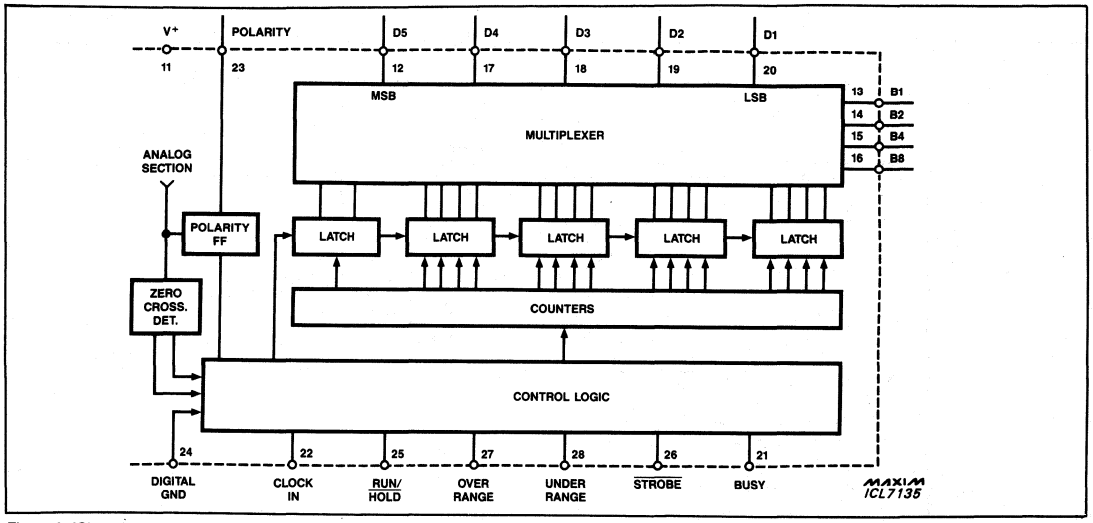


Figure 3. ICL7135 Digital Section

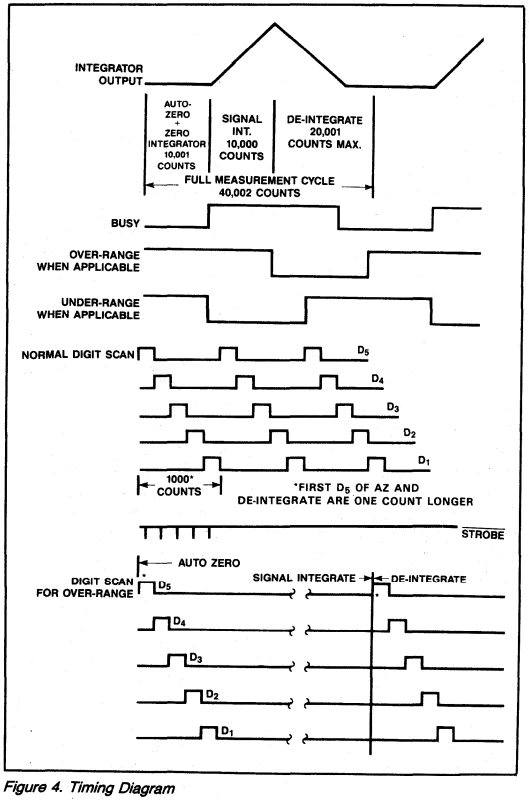


Figure 4. Timing Diagram

rising edge of the RUN/$\overline{\text{HOLD}}$ input and the BUSY output. A RUN/$\overline{\text{HOLD}}$ pulse during the unused portion of deintegrate phase will be ignored, but when in the auto-zero phase a positive pulse of only 300ns (typical) will start the conversion. Figure 5 shows a simple method of obtaining one, and only one, conversion for each measurement request.

BUSY

BUSY is a status output that goes high at the beginning of signal integrate and stays high until the first clock pulse after zero crossing during De-integrate (or end of De-Integrate if overranged). The internal data latches are loaded during the next clock cycle after the falling edge of BUSY. Since BUSY is high for the 10,000 counts of signal integrate + number of counts during De-Integrate + 1 clock cycle, a simple way of sending conversion data down a single pair of wires is to logically 'AND' BUSY with the clock and to subtract 10,001 counts from the number received. Figure 6 shows a system using this method to remotely display data.

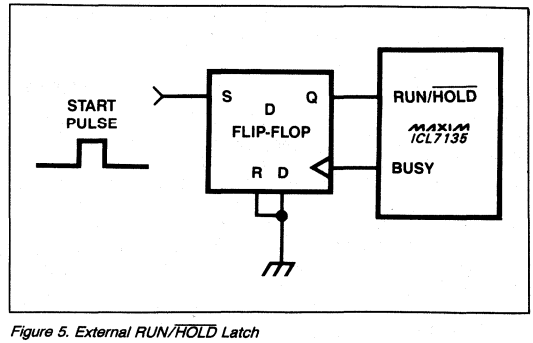


Figure 5. External RUN/$\overline{\text{HOLD}}$ Latch

4½ Digit A/D Converter with Multiplexed BCD Outputs

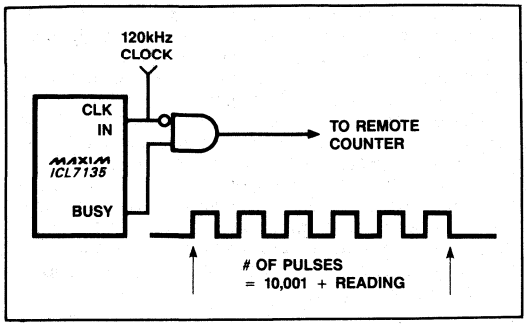


Figure 6. Serial Pulse Stream for Remote Reading

Digit Outputs

The digit outputs go high sequentially, D5 to D1, for a period of 200 clock cycles per digit. The 5 digits are continuously scanned except after an over-range measurement. After an over-range reading the digit scan stops after the strobe sequence, and remains stopped until the start of De-Integrate. For a continuous series of over-range readings, the digits will be scanned for 21,000 counts out of 40,002, resulting in a flashing display as an over-range indicator. D5 is the most significant digit.

BCD Outputs

The 4 BCD output pins are positive logic signals whose BCD data corresponds to the currently active digit strobe. The ICL7135 does not have inter-digit blanking and the BCD data changes simultaneously with the edges of the digit outputs.

$\overline{\text{STROBE}}$

The $\overline{\text{STROBE}}$ output is a negative going pulse that is useful for latching the multiplexed BCD outputs into external BCD latches. Five negative going $\overline{\text{STROBE}}$ pulses occur in the center of the data corresponding to each of the 5 digits of measurement results, once and only once after the end of each conversion (immediately after the falling edge of BUSY). The BCD data is valid at both edges of $\overline{\text{STROBE}}$, and data can be latched in either a level sensitive latch, or an edge triggered latch. Figures 11, 12 and 14 show the use of $\overline{\text{STROBE}}$ to latch the BCD data. $\overline{\text{STROBE}}$ pulse width is 1μs less than ½ clock period.

Over-range and Under-range Outputs

These active high status outputs are set to a high level at the end of BUSY if the measurement result is 1800 or less (Under-range), or greater than 19,999 (Over-range). Under-range is reset at the beginning of the signal integrate phase; over-range is reset at the beginning of the de-integrate phase.

Polarity

The Polarity output is updated at the beginning of each de-integrate phase, and is high for a positive input signal. The Polarity output is valid for all inputs, including ±0 and overrange signals.

Component Selection

The analog component values must be selected with care to achieve optimum performance in each application. Factors that affect the proper values include the reading rate, input common mode voltage, the full scale and reference voltages, and the power supply voltages.

Integrating Resistor

Good linearity is obtained when the integrating resistor value is chosen such that the buffer's maximum output current is between 5 and 40μA. The quiescent current of the buffer is 100μA, and it can supply 20μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the integrating resistor value may be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as:

$$\text{Vswing} = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

Where $I_{INT} = 20\mu A$ if R_{INT} is chosen as described above and $T_{INT} = 10{,}000$ clock periods (83.3ms for 120kHz clock frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. Normally the integrator will not saturate until its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. For ±5V supply and Analog Common and IN LO connected to ground, a ±3.5V to ±4V swing range is optimum. Rearranging the above formula and inserting values as described above, C_{INT} may be calculated as:

$$C_{INT} = \frac{20\mu A \times 83.3ms}{3.5V} = 0.47\mu F$$

The integrator swing must be reduced if either Analog Common or IN LO is not grounded, or if the supply voltage is less than ±5V.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the IN HI is a good indication of the

4½ Digit A/D Converter with Multiplexed BCD Outputs

amount of dielectric absorption in the integrating capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon capacitors. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero Capacitor

The size of the auto-zero capacitor will have a significant effect on the overall system noise, with larger auto-zero capacitors resulting in a quieter system. The dielectric absorption of the auto-zero capacitor affects only the speed of settling at power-up or recovery from overload and nearly any capacitor type can be used. The zero integrator phase of the ICL7135 allows the use of large auto-zero capacitors while avoiding the "over-range hangover" and hysteresis effects that occur in A/D converters without the zero integrator phase.

Reference Capacitor

Like the auto-zero capacitor, the reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are only required where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in multimeters.

The reference capacitor DOES need to be a low leakage capacitor since it must store the reference voltage while floating during both the signal integrate and the reference deintegrate phases. Any leakage or charge loss during these two phases results in an effective change in the scale factor of the ICL7135. Low cost film capacitors such as polyester or polystyrene have been found to be suitable in most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. For a negative polarity input signal, the reference capacitor does not shift its common mode voltage, but with a positive polarity input signal it undergoes a negative common mode shift equal to the reference voltage. If there are stray capacitances on the reference capacitor terminals, some of the charge on the reference capacitor will be used to charge these stray capacitances as the reference capacitor makes this common mode voltage shift. This loss of charge reduces the voltage on the reference capacitor, and causes positive polarity signals to have a higher measured result than a corresponding negative voltage. This error can be reduced by minimizing the stray capacitance on the reference capacitor terminals, and by increasing the value of the reference capacitor.

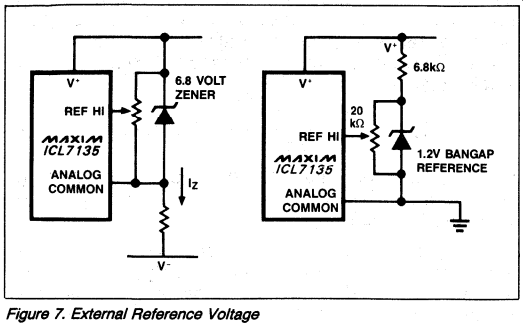


Figure 7. External Reference Voltage

Reference Voltage

The full scale reading of 20,000 will occur when $V_{IN} = 2 \times V_{REF}$. Since the 20,000 count resolution of the ICL7135 is equivalent to a 50ppm resolution, a high stability reference is recommended for high accuracy absolute measurements. Figure 7 shows two suitable methods of generating the reference voltage.

Rollover Resistor and Diode

The ICL7135 is tested for rollover using the circuit of Figure 1, with the 100kΩ resistor and diode in the circuit. The diode is noncritical, and is typically a low cost 1N4148. The resistor value is dependent on many factors including integrator swing, clock frequency, and the amount of rollover error due to "charge suckout" on the reference capacitor. 100kΩ is the optimum value for most circuits and is the value used in testing the ICL7135.

Speedup Resistor

The 27Ω speedup resistor in series with the integrating capacitor adds a pedestal voltage on top of the integrating capacitor voltage. This pedestal voltage causes zero crossing to occur earlier than would occur without the resistor. The effect of the earlier zero crossing is to give the comparator an overdrive voltage, speeding its response and reducing the conversion error due to comparator delay. If the integrator current is changed, the speedup resistor value should be changed so that the $I_{INT} \times R_{SPEEDUP} = 500\mu V$.

Clock Frequency

The clock source should be free of short-term phase and frequency jitter during the conversion period, but long term stability is not critical. The clock frequency is chosen to obtain the desired conversion rate, and to maximize the normal mode rejection of power line frequency interference. The conversion rate is directly proportional to the clock frequency, with each conversion taking 40,002 clock cycles. For maximum normal mode rejec-

4½ Digit A/D Converter with Multiplexed BCD Outputs

tion, the signal integration period should be an integral multiple of the power line cycles.

$$\text{Reading Rate (in readings per second)} = \frac{f_{CLK}}{40{,}002}$$

$$f_{CLK} \text{ for maximum normal mode rejection} = \frac{f_{LINE} \times 10{,}000}{N}$$

Where f_{LINE} is the line frequency, normally 50Hz or 60Hz and N is the number of line cycles that occur during a signal integration period. For maximum normal mode rejection, N should be an integer.

For 60Hz rejection, suitable clock frequencies include 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, and 75kHz. Suitable frequencies for use with 50Hz power include 250kHz, 166⅔kHz, 125kHz, and 100kHz. The two most common clock frequencies are 120kHz (3 readings per second) and 100kHz (2½ readings per second). Note that a 100kHz clock frequency rejects both 50Hz and 60Hz normal mode signals.

The maximum clock rate is limited by the maximum rate at which the digital logic will correctly function (typically 2MHz), and by the speed of response of the comparator. The comparator delay, about 3µs, has the same effect on the measurement result as does an offset voltage with the same polarity of the input signal. At the recommended clock frequency of 120kHz, this small offset is slightly less than ½ count. At higher clock frequencies the value of the speedup resistor in series with the integration capacitor (normally 27Ω) should be increased. At frequencies above 120kHz, ringing on the integrator output may cause nonlinearities in the first few counts.

The minimum clock frequency is limited by the leakage of the auto-zero and reference capacitors. While seldom desired, measurement cycles as long as 10 seconds can be performed with negligible error at room temperature. Figures 8A and 8B show two methods of generating a suitable clock signal for the ICL7135.

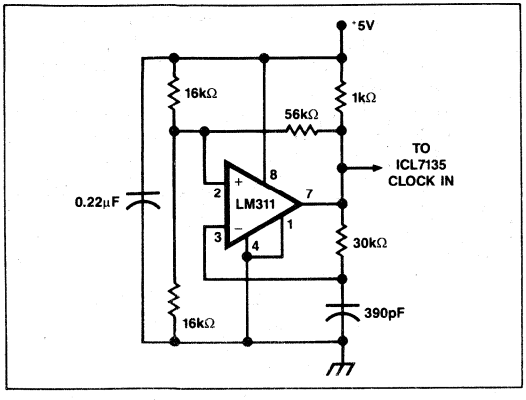


Figure 8A. LM311 Clock Source

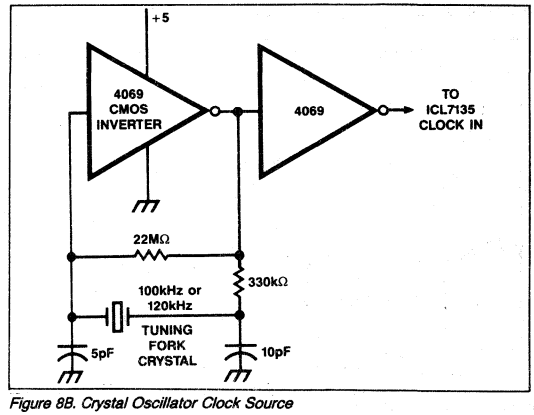


Figure 8B. Crystal Oscillator Clock Source

Application Hints

Grounds

As with all sensitive analog circuitry, it is important to keep the Digital Ground separate from the analog ground (called Analog Common on the ICL7135) to minimize errors caused by the coupling of noise from the digital circuitry into the sensitive analog section. Analog Common should be connected to Digital Ground at only one point, and return currents from digital loads must not flow through the analog ground lines. Avoid any unnecessary current flow in the analog ground path.

Single 5V Supply Operation

The ICL7135 normally uses ±5V supplies, however, in some applications the negative supply is not needed. Specifically, the negative 5V supply is not required if the input signal can be referenced to the center of the ICL7135's common mode voltage range AND the signal voltage is less than ±1.5V. The integrator swing must be reduced, and there will be a slight increase in system noise and nonlinearity. See Figure 9 for recommended component values.

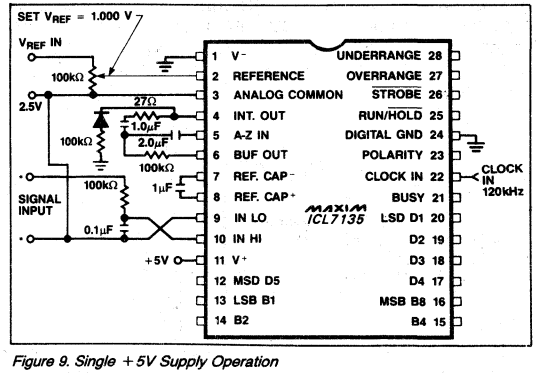


Figure 9. Single +5V Supply Operation

4½ Digit A/D Converter with Multiplexed BCD Outputs

Generating a Negative Supply from +5V

Figures 10A and 10B show two methods of generating a negative supply for the ICL7135. The Maxim ICL7660 will supply 2mA (the maximum supply current of the ICL7135) at 4.85V drop, while the circuit using the CMOS inverter will deliver approximately −3.5V. If the CMOS inverter is used to generate a minus supply, the integrator swing should be reduced to 2.5 to 3V.

Noise

The normal system noise around zero is about 15μV peak-to-peak (not exceeded 95% of the time). Near full scale, the noise increases to about 30μV. The main noise source is the auto-zero loop, and increasing the value of the auto-zero capacitor will reduce the noise. Other noise sources include the buffer and integrator noise; comparator noise; and stray pickup in the input circuitry, the integrator, and the reference capacitor. The noise caused by stray pickup of interfering signals can be reduced by a tight layout and shielding. If the interfering signal frequency is constant, the effects of stray pickup in the input and integrator can be reduced by choosing a clock frequency such that the signal integration period is an integral multiple of the interfering signal's period. Since the length of the de-integration period depends on the input signal level, no single clock frequency can be chosen to reject interfering signals during the de-integrate phase.

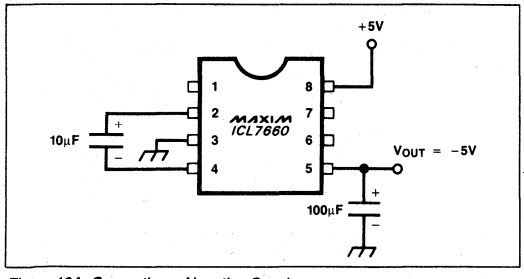


Figure 10A. Generating a Negative Supply

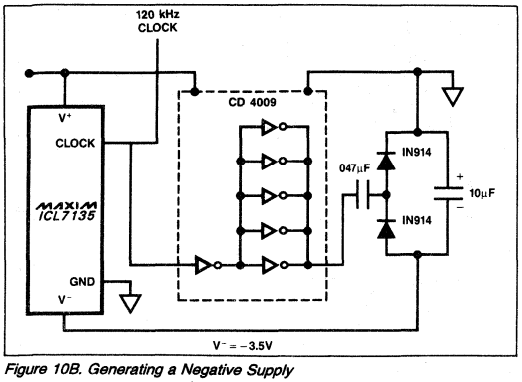


Figure 10B. Generating a Negative Supply

Typical Applications

Figure 11 uses Maxim's ICL7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICL7211 and the CMOS exclusive OR gates are used to drive the ½ digit and the polarity sign. The four AND gates combine the digit outputs with the $\overline{\text{STROBE}}$ output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is ample data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when over-range goes high. The ICL7211A will blank the display when all ones (hex F) is loaded.

The typical operating circuit on the first page of this data sheet shows a 4½ digit A/D with LED drive using the Maxim ICL7212 display driver. In this case the polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135 Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Some applications require non-multiplexed, latched BCD outputs. The circuit shown in Figure 12 will demultiplex and latch the ICL7135 output. If only the first rank of latches is used, the data should not be used during the 800 clock cycle update period that takes place at the end of each conversion since during this update period the

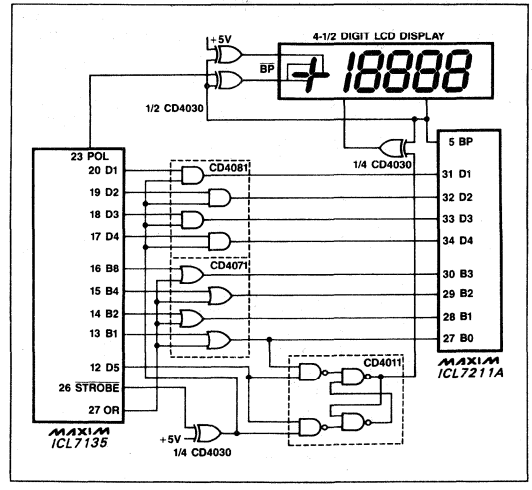


Figure 11. LCD Display with Digit Blanking on Overrange

4½ Digit A/D Converter with Multiplexed BCD Outputs

most significant digit (MSD) data will correspond to the new reading and the least significant digit (LSD) data will be old data from the previous converison. The second rank of latches shown in dotted lines will eliminate this problem by updating all digits simultaneously with the rising edge of D5.

There are many different possible ways of interfacing the ICL7135 to a microprocessor. Figure 13 shows a method that uses only 8 I/O lines. The digit outputs drive a priority encoder, which converts the 1-of-5 format of the digit outputs to a 3 bit binary code. When no digit is active (as in over-range), the binary output code is 0, otherwise the output corresponds to the digit number of the active digit. By sensing BUSY as either an input or as an interrupt, the microprocessor can detect when new data is available.

Another possible interface scheme is to sense only digit D5, then use time delays to choose when to read the other digits' data.

Interfacing With UARTs and Microprocessors

Figure 14 shows a simple interface between a UART and a free running ICL7135. The transmission of the five data words is started by the five STROBE pulses. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. The polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). A parity flag at the receiver can be decoded as a positive signal, no flag as negative, if EPE of the receiver is held low. Figure 15 shows a more complex arrangement. DR goes high when the UART receives a byte via the send input, $\overline{RRI}$. Since DR is connected to the ICL7135's RUN/$\overline{HOLD}$ input this starts a new conversion. At the end of the conversion the falling edge of BUSY resets DR via the UART's DRR input. The transmit sequence is again started by STROBE. A quad 2-input multiplexer is used to superimpose polarity, over-range, and under-range onto the D5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

To insure proper operation, it is necessary that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives.

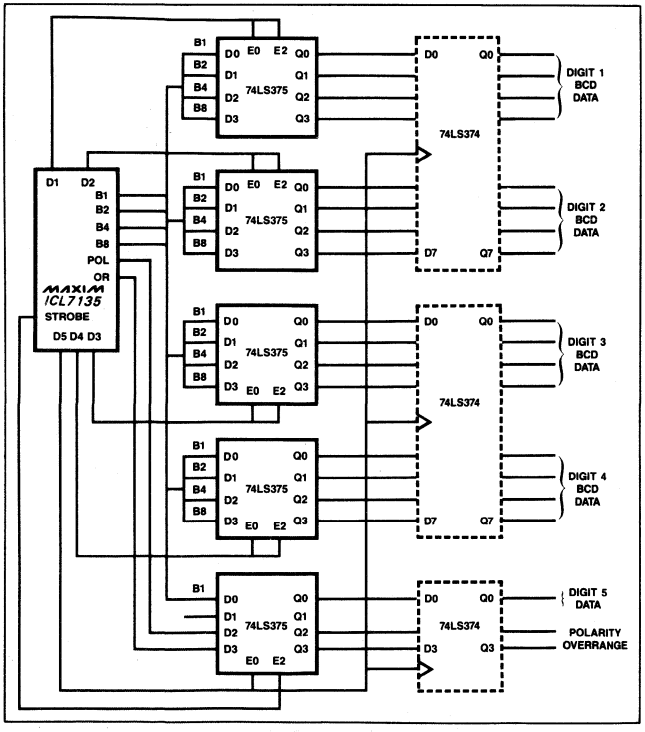


Figure 13. µP Interface

Figure 12. Non-Multiplexed, Latched BCD Output

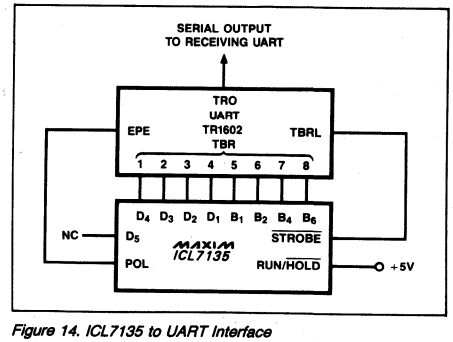


Figure 14. ICL7135 to UART Interface

4½ Digit A/D Converter with Multiplexed BCD Outputs

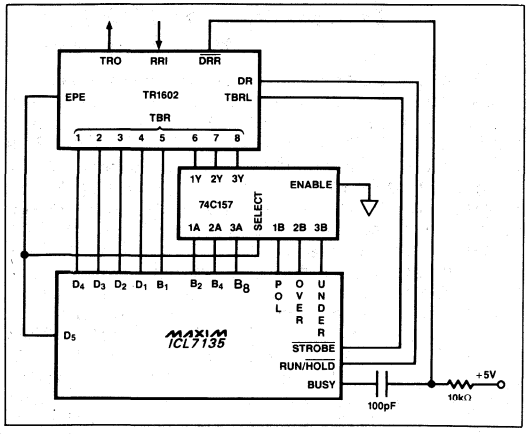
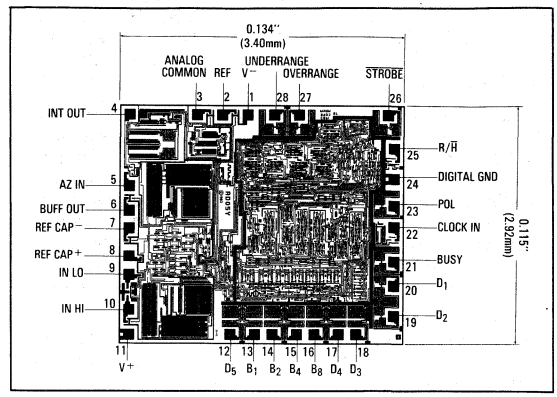


Figure 15. Complex ICL7135 to UART Interface

Chip Topography



MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7136 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7136 a superior device, especially for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7136 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

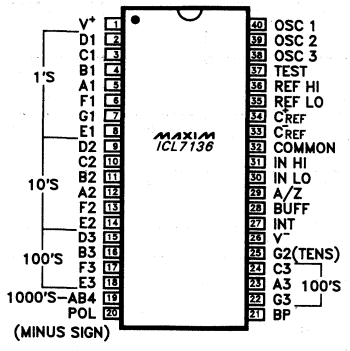
Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration

Top View



See Page 1-12 for 44 Lead Chip Carrier Pin Configuration

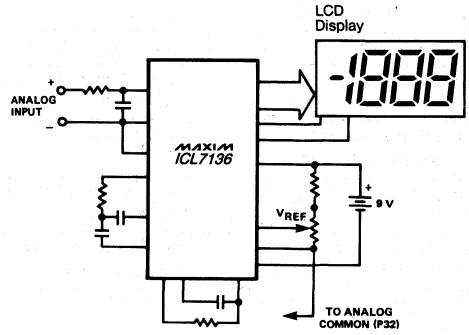
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guarateed less than 1mW-9V battery life 3000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

Part	Temp. Range	Package
ICL7136CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7136CJL	0°C to +70°C	40 Lead CERDIP
ICL7136CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7136C/D	0°C to +70°C	Dice

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Figures 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 8)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≈ 200.0mV				
	T_A = 25°C (Note 8)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 12)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0				
	T_A = 25°C		60	100	µA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ±10V to 0V		0	1	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

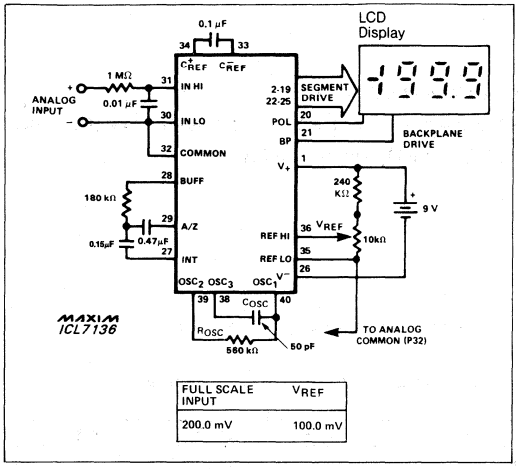


Figure 1. Maxim ICL7136 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

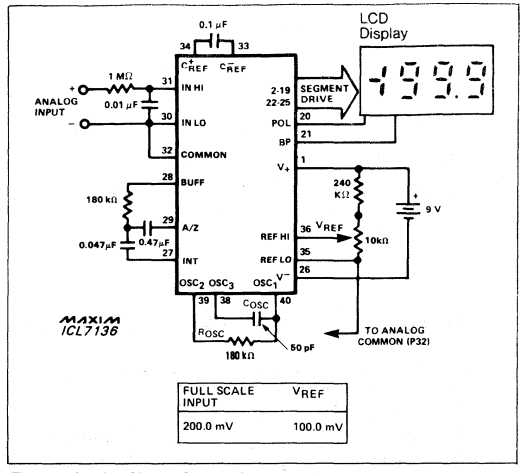


Figure 2. Maxim ICL7136 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

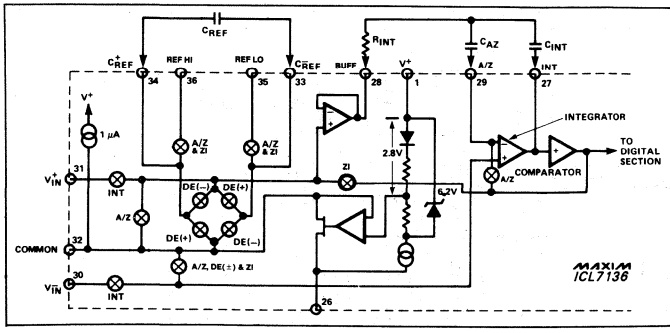


Figure 3. Analog Section of 7136

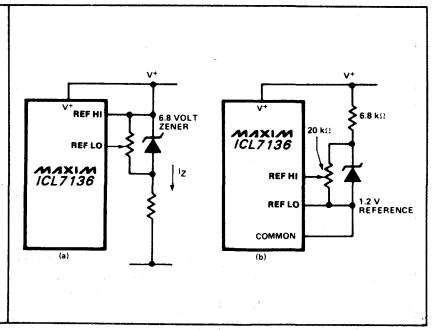


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7136. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

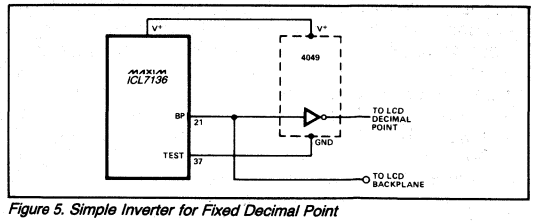


Figure 5. Simple Inverter for Fixed Decimal Point

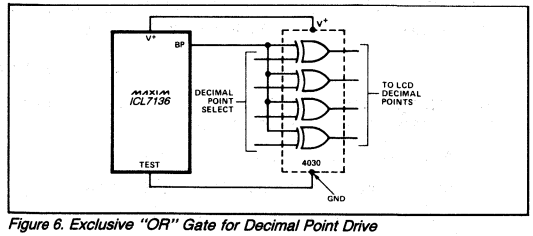


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

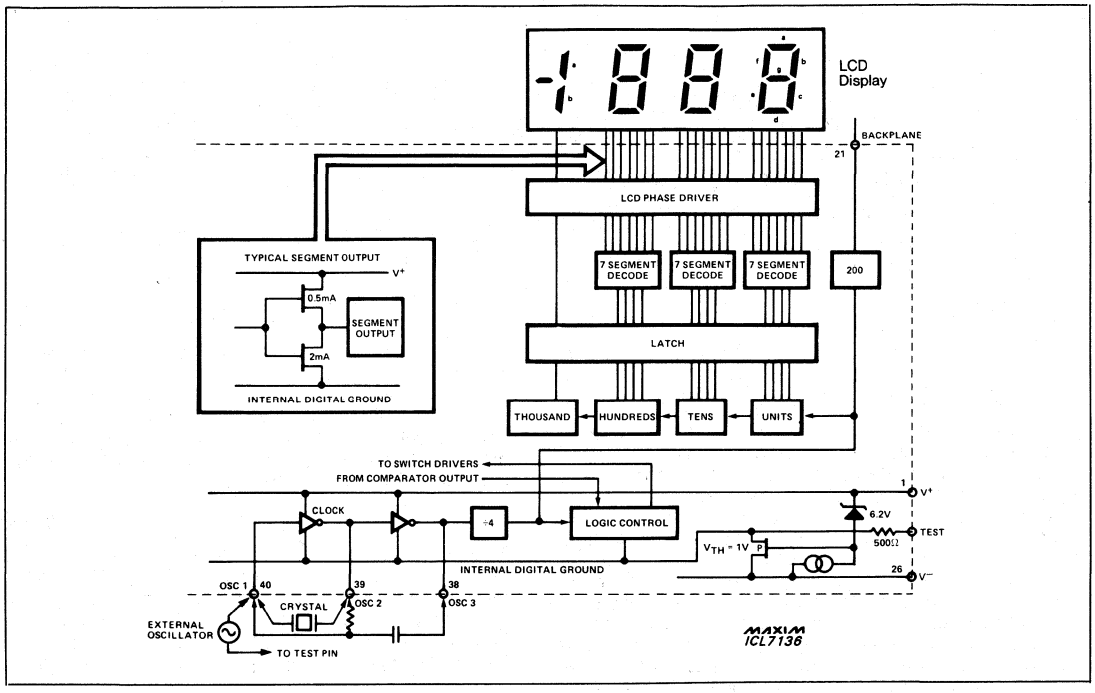


Figure 7. ICL7136 Digital Section

Digital Section

The digital section for the ICL7136 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currrents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7136. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7136 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Low Power, 3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. A 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible non-linearity.

The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

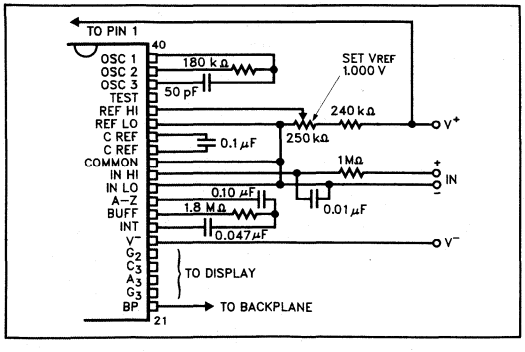


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

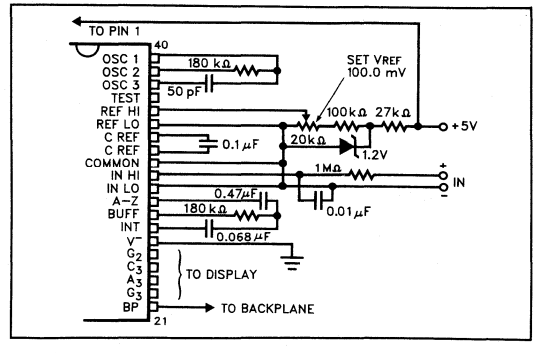


Figure 9. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

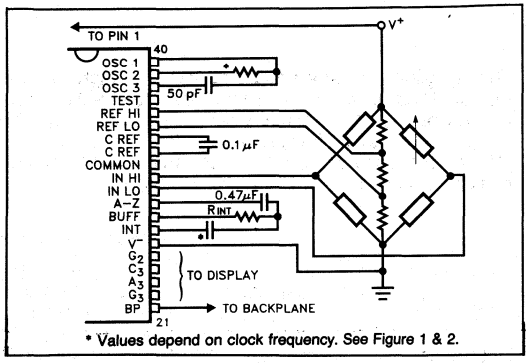


Figure 10. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

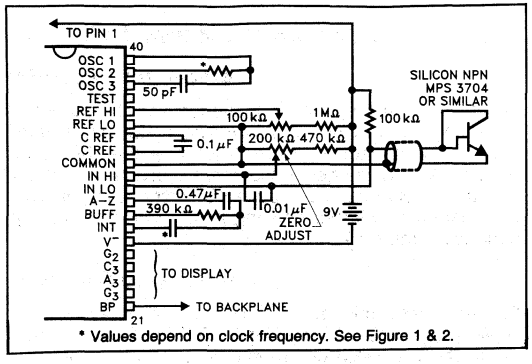
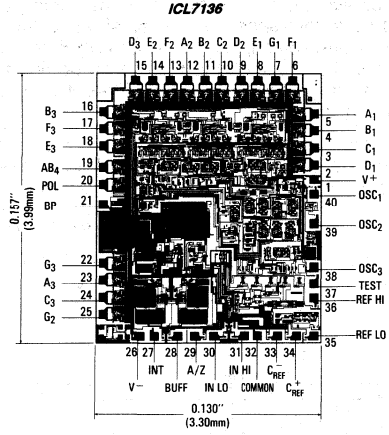


Figure 11. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography



MAXIM
Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7137 is a monolithic analog to digital converter with all the necessary active devices to directly interface with a light emitting diode (LED) display. Excluding the LED display current, the ICL7137 supply current is under 200μA, making it suitable for battery operation.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7137 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

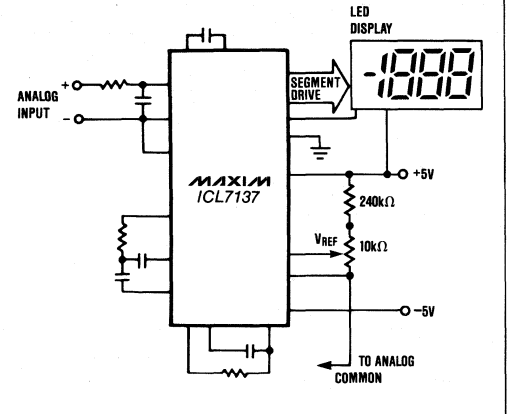
Features

- **Improved 2nd Source! (see 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LED Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7137CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7137CJL	0°C to +70°C	40 Lead CERDIP
ICL7137CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7137C/D	0°C to +70°C	Dice

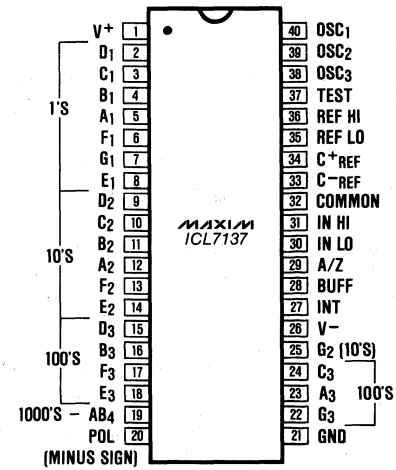
Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... -9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near full scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0° < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply Current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (with respect to Positive Supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A=25°C, f_{CLOCK}=16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion in the ICL7136 data sheet.
Note 5: 48kHz oscillator, Figure 2, increases current by 35μA (typ).
Note 6: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed Over Temperature**
- **Guaranteed Overload Recovery Time**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 8)**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 7)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1 unless noted.)

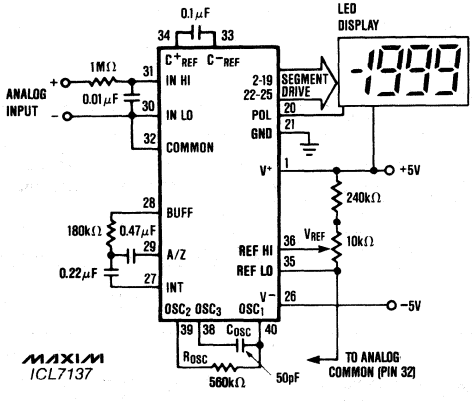
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 9) **0° ≤ T_A ≤ 70°C (Note 10)**	-000.0 **-000.0**	±000.0 **±000.0**	+000.0 **+000.0**	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 9) **0° ≤ T_A ≤ 70°C (Note 10)**	999 **998**	999/1000 **999/1000**	1000 **1001**	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200mV T_A = 25°C (Note 9) 0° ≤ T_A ≤ +70°C (Note 10)	-1	±0.2 ±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio	**V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV**	**-100**	**±5**	**+100**	μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		μV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 9) **0° ≤ T_A ≤ +70°C**		1	10 **200**	pA
Zero Reading Drift	V_{IN} = 0V, 0° ≤ T_A ≤ 70°C (Note 9)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C)(Note 9)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0V T_A = 25°C **0° ≤ T_A ≤ 70°C**		60	200 **240**	μA
V^- Supply Current	**V_{IN} = 0V,**		**60**	**200**	μA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA mA
Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015.2)
Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).
Note 9: Test condition is V_{IN} applied between the "Analog Input" pins (Figure 1).
Note 10: 1MΩ resistor is removed in Figures 1 and 2.
Note 11: Number of measurement cycles for display to give accurate reading.

Low Power, 3½ Digit A/D Converter

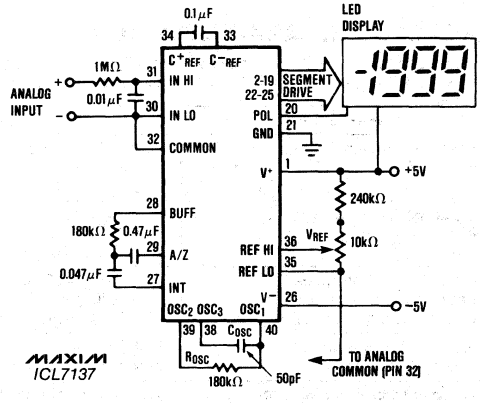
Detailed Description

The Maxim ICL7137 3½ digit A/D converter is similar to the Maxim ICL7136 except for the LED segment driver outputs, and is similar to the ICL7107 except for much reduced power supply currents (exclusive of the LED currents.) For a detailed product description, component value selection, and package dimensions, refer to Maxim's ICL7136 data sheets; for applications information refer to Maxim's ICL7107 data sheets.



FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

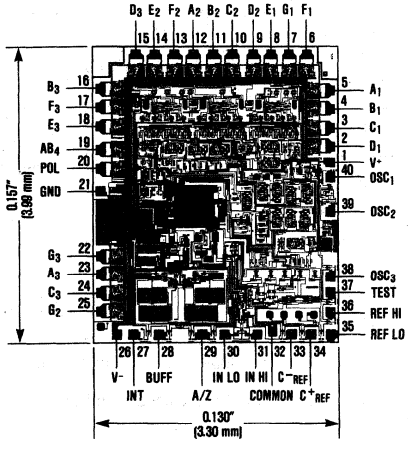
Figure 1. Maxim ICL7137 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)



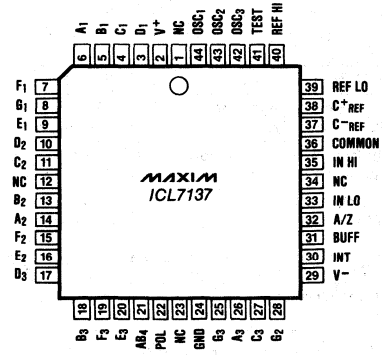
FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

Figure 2. Maxim ICL7137 Typical Operating Circuit Clock Frequency 48kHz (3 reading/sec)

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

MAXIM

D/A Converters

2

Part Number	Type	Resolution	Relative Accuracy % F.S.	Gain Tempco ppm/°C Max	Settling Time	Output	Power Dissipation (mW)	Page No.
AD565A	Bipolar, w/Ref.	12-bit	0.012 to 0.006	20	250ns max	Current	345	2-1
AD566A	Bipolar	12-bit	0.012 to 0.006	20	350ns max	Current	300	2-1
AD7224	Multiplying	8-bit	0.2	20	5μs max	Voltage	75	2-9
AD7225	Quad, Multiplying	8-bit	0.2	20	4μs max	Voltage	150	2-19
AD7226	Quad, Multiplying	8-bit	0.2	20	4μs max	Voltage	195	2-19
AD7520	Multiplying	10-bit	0.2 to 0.05	10	500ns typ	Current	30	2-31
AD7521	Multiplying	12-bit	0.2 to 0.05	10	500ns typ	Current	30	2-31
AD7523	Multiplying, Low Cost	8-bit	0.2 to 0.05	67	150ns typ	Current	1.6	2-37
AD7524/ MAX7624	Multiplying	8-bit	0.5 to 0.2	40	250ns max	Current	30	2-41
AD7528/ AD7628	Dual, Multiplying	8-bit	0.5 to 0.2	35	180ns max	Current	15	2-49
AD7530	Multiplying	10-bit	0.2 to 0.05	10	500ns typ	Current	30	2-61
AD7531	Multiplying	12-bit	0.2 to 0.05	10	500ns typ	Current	30	2-61
AD7533	Multiplying	10-bit	0.2 to 0.05	10	600ns max	Current	30	2-65
AD7541	Multiplying	12-bit	0.025 to 0.012	10	1μs max	Current	30	2-71
AD7541A	Multiplying	12-bit	0.025 to 0.012	5	600ns typ	Current	30	2-75
AD7542	Multiplying	12-bit	0.012	5	2μs max	Current	12.5	2-81
AD7543	Serial Input	12-bit	0.012	5	2μs max	Current	12.5	2-89
AD7545	Multiplying	12-bit	0.05 to 0.012	5	2μs max	Current	30	2-97

Digital/Analog Converter Terminology

Absolute Accuracy: The difference between the ideal expected DAC output voltage or current and the actual observed output. See Total Unadjusted Error.

Channel-To-Channel Isolation: In multiple DAC devices, the amount of signal which couples from one DAC reference input to a different DAC output. Specified in dB.

Differential Nonlinearity: The difference between the measured and the ideal output step change for a 1 LSB digital input change. Specified in LSB. A specification of ±1 LSB or less guarantees monotonicity.

Digital Crosstalk: In multiple DAC devices, the Glitch Impulse coupled from the digital inputs of one DAC to the analog output of a different DAC channel. Specified in nV-s.

Digital To Analog Converter: Also DAC, D/A, and D-to-A. A device which converts a digital input code to a variable analog output current or voltage.

Feedthrough Error: Signal caused by coupling from reference input to output when the DAC logic inputs are all LOW. Expressed in mV or dB relative to V_{REF} and measured with an AC reference input.

Four-Quadrant: Refers to the ability of the DAC to operate with reference inputs and analog outputs of both positive and negative polarity.

Full-Scale Error: Also Gain Error. The difference between the actual and ideal DAC output at Full-Scale. Expressed in mV, % of FSR, or LSBs.

Gain: Ratio of output voltage to input voltage. For DMOS multiplying DACs, when used with an output amplifier, it is the ratio of output voltage to reference voltage.

Glitch Impulse: The amount of charge injected from the digital inputs to the analog output when the inputs change state. Specified as the area under the impulse, in pA-s or nV-s.

Least Significant Bit (LSB): The digital input bit that has the smallest weight. Also the smallest analog step that a DAC can take. As an analog quantity, 1 LSB = $V_{REF} \times 2^{-N}$, where N is the number of DAC input bits.

Linearity: Also Nonlinearity and Integral Nonlinearity. See Relative Accuracy.

Monotonic: A DAC is said to be monotonic if its analog output either increases or stays the same for an increasing digital input. Monotonicity is either guaranteed by direct statement or by a maximum Differential Nonlinearity Specification of ±1 LSB.

Most Significant Bit: The digital input bit that has the largest weight.

Multiplying DAC: A type of DAC in which the reference input can be varied. The output signal is then the "product" of the reference input and the digital input code.

Output Amplifier: Typically an op-amp, connected to a DAC output, which converts an output current to a voltage. Also used to buffer a high impedance voltage output or provide additional gain. Some DACs include on-chip output amplifiers.

Output Capacitance: Capacitance from DAC output terminals to ground.

Output Leakage Current: DAC output current when the ideal value is zero. OUT1 current when all digital inputs are low and OUT2 current when all digital inputs are high.

Propagation Delay: Time required, after an input code change, for a DAC output to reach 90% of its final value. Usually specified for a Full Scale output step.

R-2R Ladder: A resistor network used to generate binarily weighted currents or voltages in Digital-to-Analog and Analog-to-Digital Converters.

Relative Accuracy: (or End-Point Nonlinearity) The maximum deviation from a straight line which passes through the endpoints of the DAC transfer function (Zero and Full Scale). It is expressed in % or ppm of the Full Scale Range (FSR) or in LSBs.

Resolution: The number of steps that a DAC can take expressed in number of bits. A DAC with N-bit resolution can take 2^N steps.

Settling Time: The time required for a DAC to settle (and remain) within ½ LSB of its final value. Usually specified for a Full Scale step change.

Temperature Coefficient: The variation of a parameter (such as Zero Error, Full Scale Gain, or Linearity) with ambient temperature. Specified in %/°C or ppm/°C.

Total Unadjusted Error: Includes Full Scale, Relative Accuracy, and Zero Code Error specifications. The maximum output deviation from the ideal expected values. Specified in LSBs or % of FSR at a fixed reference voltage, usually +10V.

Unipolar: Refering to DAC output, either 0 to +V or 0 to -V output.

Bipolar: Refering to DAC output, -V to +V output.

Zero Code Error: Also Offset Error. The DAC output voltage for an all zero digital input code (Unipolar configuration). Specified in mV or LSBs.

MAXIM

High Speed 12-Bit Monolithic D/A Converters

General Description

The AD565A and AD566A are 12-bit monolithic digital to analog converters (DACs) built in bipolar technology that offer an excellent combination of high speed settling and ±¼LSB linearity. The AD565A also features an on-chip precision 10V reference, whereas the AD566A requires an external reference.

Laser trimming of the on chip thin film resistor networks achieve ±⅛LSB typical linearity (±¼LSB max.) at +25°C. Full scale settling time to ±½ LSB is specifed at 250ns max. for the AD565A and 350ns max. for the AD566A. This high speed and accuracy makes the AD565A and AD566A DACs ideal choices for fast analog to digital converters and CRT display drivers.

The AD565A and AD566A contain onboard application resistors that can be used as feedback and offset resistors with an external output amplifier to generate unipolar and bipolar outputs or as the input resistors in analog to digital converter applications. The excellent matching and tracking of the DAC's current setting resistor and application resistors assure good gain stability over both time and temperature.

Applications

High Speed Display Drivers
High Speed Control Systems
High Speed A/D Converters
Data Acquisition Systems
Test Equipment

Features

- **250ns Settling to ±½LSB**
- **Montonicity Guaranteed Over Temperature**
- **TTL and CMOS Logic Compatibility**
- **High Stability Buried Zener 10V Reference (AD565A Only)**
- **±½LSB Linearity Guaranteed Over Temperature (AD565AK,AT and AD566AK,AT Only)**
- **Low Power Consumption: 225mW**
- **Widely Second Sourced**

Ordering Information

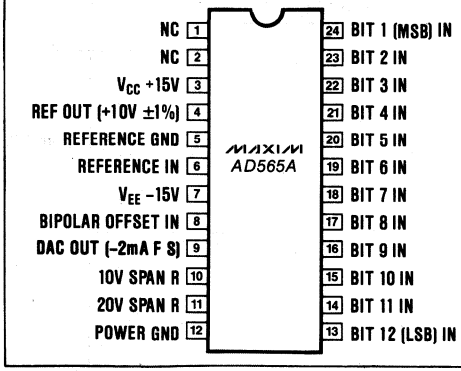
PART	TEMP. RANGE	PACKAGE*	ERROR
AD565AJN	0°C to +70°C	Plastic DIP	±½LSB
AD565AJD	0°C to +70°C	Ceramic	±½LSB
AD565AJQ	0°C to +70°C	CERDIP**	±½LSB
AD565AJCWG	0°C to +70°C	Small Outline	±½LSB
AD565AJC/D	0°C to +70°C	Dice	±½LSB
AD565AKN	0°C to +70°C	Plastic DIP	±¼LSB
AD565AKD	0°C to +70°C	Ceramic	±¼LSB
AD565AKQ	0°C to +70°C	CERDIP**	±¼LSB
AD565AKCWG	0°C to +70°C	Small Outline	±¼LSB
AD565ASD	-55°C to +125°C	Ceramic	±½LSB
AD565ASQ	-55°C to +125°C	CERDIP**	±½LSB
AD565ATD	-55°C to +125°C	Ceramic	±¼LSB
AD565ATQ	-55°C to +125°C	CERDIP**	±¼LSB

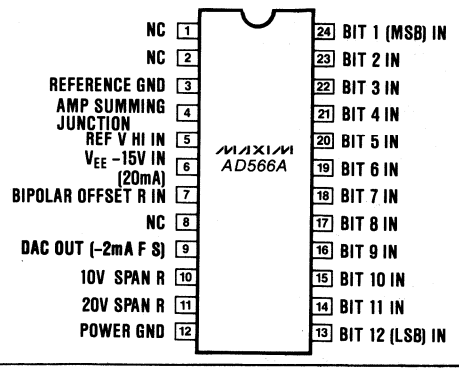
* *All devices — 24 lead packages*
** *MAXIM reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering information for AD566A continued on back page

2

Pin Configurations

Top View





High Speed 12-Bit Monolithic D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground (AD565A only) ..... 0V to +18V
V_{EE} to Power Ground ..... 0V to -18V
Voltage on DAC Output ..... -3V to +12V
Digital Inputs (pins 13 to 24) to Power Ground ..... -1V to +7V
REF IN to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
REF OUT (AD565A only)
Short Circuit to Power Ground ..... Continuous
Short to V_{CC} ..... Momentary
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering, 10 sec) ..... +300° C
Package Dissipation 1000mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25° C, V_{CC} = +15V (AD565A only), V_{EE} = -15V , unless noted)

PARAMETER	CONDITIONS	AD565AJ, AS AD566AJ, AS			AD565AK, AT AD566AK, AT			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data Inputs (Pins 13 to 24)								
Input Voltage								
Bit ON Logic "1"	TTL or 5V CMOS	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	T_{MIN} to T_{MAX} (Note 1)	0		+0.8	0		+0.8	V
Logic Current (each bit)								
Bit ON Logic "1"			+120	+300		+120	+300	µA
Bit OFF Logic "0"			+35	+100		+35	+100	µA
Resolution				12			12	Bits
Output								
Output Current								
Unipolar (all bits on)		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Output Resistance (exclusive of span resistors)		6	8	10	6	8	10	kΩ
Output Offset								
Unipolar (adjustable to zero per Fig. 1)			0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Fig. 2, R_1 and R_2 = 50Ω fixed)			0.05	0.15		0.05	0.1	
Output Capacitance			25			25		pF
Output Compliance Voltage	T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
Accuracy (error relative to full scale)	+25° C		±¼ (0.006)	±½ (0.012)		±⅛ (0.003)	±¼ (0.006)	LSB
	T_{MIN} to T_{MAX}		±½ (0.012)	±¾ (0.018)		±¼ (0.006)	±½ (0.012)	(% of F.S.)
Differential Nonlinearity	+25° C		±½	±¾		±¼	±½	LSB
	T_{MIN} to T_{MAX}	Monotonicity Guaranteed						
Temperature Coefficients								
AD565A with Internal Reference								
Unipolar Zero			1	2		1	2	
Bipolar Zero			5	10		5	10	
Gain (Full Scale)								
AD565AJ			15	50				ppm/° C
AD565AK						10	20	
AD565AS			15	30				
AD565AT						10	15	
Differential Nonlinearity			2			2		
AD566A								
Unipolar Zero			1	2		1	2	
Bipolar Zero			5	10		5	10	
Gain (Full Scale)								ppm/° C
AD566AJ, AS			7	10				
AD566AK, AT						2	3	
Differential Nonlinearity			2			2		

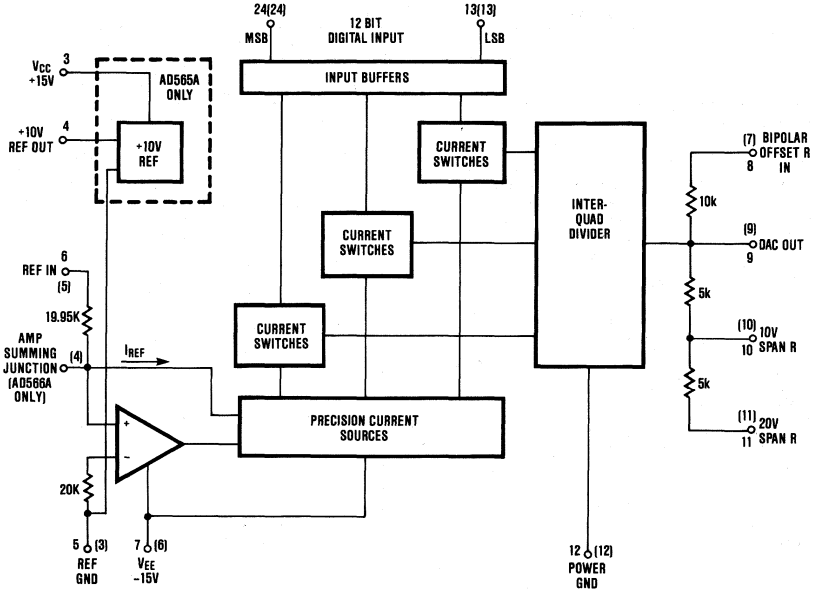
ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25° C, V_{CC} = +15V (AD565A only), V_{EE} = -15V , unless noted)

PARAMETER	CONDITIONS	AD565AJ, AS AD566AJ, AS			AD565AK, AT AD566AK, AT			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Full Scale Transition 70% to 90% Delay plus Rise Time 90% to 10% Delay plus Full Time	(Note 3)		15 30	30 50		15 30	30 50	ns
Settling Time to within ±½ LSB All Bits on-to-off or off-to-on	AD565A (Note 3) AD566A (Note 3)		150 250	250 350		150 250	250 350	ns
Temperature Range (Operating)	AJ, AK AS, AT	0 -55		+70 +125	0 -55		+70 +125	°C
Power Requirements (AD565A Only)								
$+I_{PS}$ $-I_{PS}$	11.4V > |V_{CC}| > 16.5V		3 -12	5 -18		3 -12	5 -18	mA
$+V_{CC}$ Gain Sensitivity $-V_{EE}$ Gain Sensitivity (Note 2)	11.4V > |V_{EE}| > 16.5V		3 15	10 25		3 15	10 25	ppm of F.S./%
Power Requirements (AD566A Only)								
$-I_{PS}$	11.4V > |V_{EE}| > 16.5V		-12	-20		-12	-20	mA
$-V_{EE}$ Gain Sensitivity			15	25		15	25	ppm of F.S./%
Programmable Output Ranges (AD565A and AD566A)	See Figs. 4,5		0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10		V
External Adjustments								
Gain Error with Fixed 50Ω Resistor Bipolar Zero Error with Fixed 50Ω Resistor Gain Adjustment Range Bipolar Zero Adjustment Range	See Figs. 4,5		±0.1 ±0.05 ±0.25 ±0.15	±0.25 ±0.15		±0.1 ±0.05 ±0.25 ±0.15	±0.25 ±0.1	% of F.S.
Reference Input Impedance		15	20	25	15	20	25	kΩ
Reference Output Voltage (AD565A Only) **Reference Output Current** (available for external loads) (AD565A Only)		9.90 1.5	10.00 2.5	10.10	9.90 1.5	10.00 2.5	10.10	V mA
Power Dissipation (AD565A) AD566A			225 180	345 300		225 180	345 300	mW
Multiplying Mode Performance (AD566A Only)								
Quadrants Reference Voltage Accuracy Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p] sinewave frequency for ½ LSB [p-p] feedthrough) Output Slew Rate 10%-90% 90%-10% Output Settling Time (all bits on and a 0-10V step change in reference voltage)		Two (2): Bipolar Operation at Digital Input Only +1V to +10V, Unipolar 10 Bits (±0.05% of Reduced F.S.) for 1V DC Reference Voltage 40kHz typ 5mA/μs 1mA/μs 1.5μs to 0.01% F.S.						
Control Amplifier (AD566A)								
Full Power Bandwidth Small-Signal Closed-Loop Bandwidth		300kHz 1.8MHz						

Note 1: The digital input levels are guaranteed but not tested over the temperature range.
Note 2: The power supply gain sensitivity is tested in reference to a V_{CC} of +15V and V_{EE} of -15V d.c.
Note 3: Sample tested at +25°C to ensure compliance.

High Speed 12-Bit Monolithic D/A Converters



Note 1: Pin #s in parenthesis for AD566A.

Figure 1. Functional Block Diagram

Circuit Description

The AD565A and AD566A are 12-bit precision DACs that consist of three binary weighted quad current sources with 16:1 interquad current dividers (see figure 1). Each quad has four current switches with 8-4-2-1 current weighting ratios. The current switches are optimized for fast switching and low transient glitches at the output of the DAC during input code changes.

Full scale accuracy of the DACs are maintained over temperature and time by the DAC control amplifier that includes a current switch reference device that implements first order correction for resistor, transistor V_{BE} and beta changes with temperature so that the only remaining errors are those that are induced by component mismatch.

The AD565A has a buried zener diode that is used for the on chip 10V voltage reference. In the feedback of the reference amplifier is a temperature compensation circuit that allows reference temperature coefficients as low as 10ppm/°C to be achieved. The 10V output of the voltage reference is laser trimmed to within ±10mV.

Application Hints

To realize the true performance of the AD565A and AD566A special attention must be taken in the application of the device.

The settling time of the DAC is specified in the current output mode. However, most DAC applications require a current to voltage conversion. The simplest, and fastest voltage conversion technique is achieved by connecting a low value resistor directly between the output and ground (see figure 2). The settling time is a function of the cell switching and the RC time constant of the AD565A and AD566A output capacitance (typically 25pF) plus any stray capacitance, and the value of the output resistor. Settling to 0.01% (½LSB) of full scale for a full scale change requires 9.1 time constants. The effect of the external resistor becomes important when the equivalent resistance at the output of the DAC is over 1kΩ

The wide compliance voltages of the AD565A and AD566A allow direct current to voltage conversion with just an output resistor. Connecting the internal gain (span) resistors (pins 10 and 11) to ground and the bipolar offset resistor to the internal 10V reference on the AD565A and an external 10V reference for the AD566A, a bipolar output voltage swing of ±1.60V

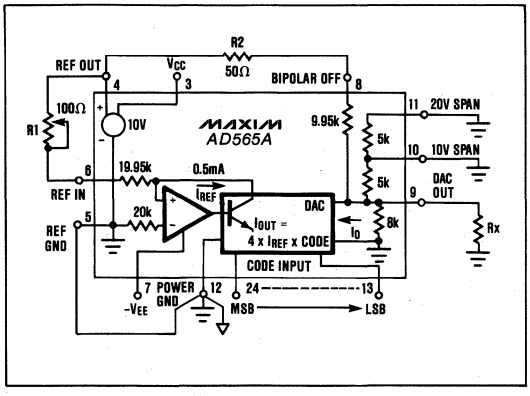


Figure 2. Unbuffered Bipolar Voltage Output

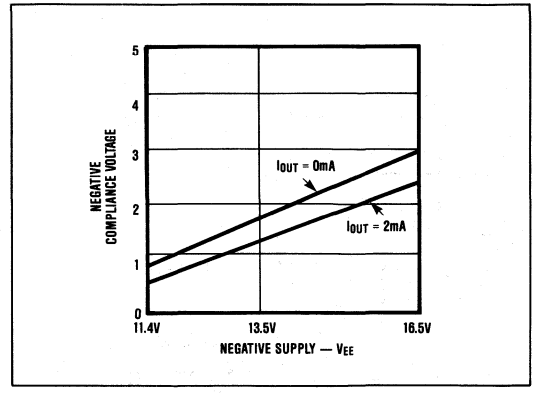


Figure 3. Typical Negative Compliance Range vs. Negative Supply

can be generated. Other combinations of external and the internal resistors can scale the full scale output current of 0 to -2mA to any voltage as long as this voltage stays within the compliance voltage of the AD565A and AD566A, which is typically -2V to +10V. For example, setting the Rx = 2.67kΩ produces an equivalent impedance of 1kΩ giving a ±1V output voltage swing.

The output voltage compliance of typically -2V to +10V allows the performance of the DAC to be unaffected by changes in the output terminal voltage. There is however, an equivalent output resistance of 8kΩ in parallel with 25pF which produces an equivalent current error when the output voltage deviates from ground. This effect is linear and is independent of the digital input code. Output swings outside the compliance range can cause either output stage saturation or breakdown which may result in non-linear performance. The compliance limits are affected only by the output current and the negative supply voltage. The positive supply voltage has no effect. Figure 3 shows the typical negative compliance versus the negative supply voltage.

The current output of the DAC can directly drive 50Ω and 75Ω coaxial cable. Terminating the cable in it's characteristic impedance would produce a ±50mV full scale swing for the 50Ω and ±75mV for the 75Ω cable. The settling times are dominated by the internal settling of the AD565A and AD566A.

The high speed current steering switching cell and internally compensated reference amplifier of the AD565A and AD566A have been specifically designed for fast settling. The typical settling time to ±0.01% (½LSB) for the major carry or full scale change (worst case transition) is about 200ns; the lower order bits all settle in less than 200ns. The maximum guaranteed settling time to 0.01% (±½LSB) for the AD565A is 250ns and 350ns for the AD566A.

Buffered Voltage Output

If an external op-amp is used to provide low impedance output drive and high voltage swing, some loss in settling time will occur due to the op-amp's own settling characteristics. In these applications the DAC's output capacitance should be compensated by a feedback capacitor connected across the amplifier's output and inverting input as shown in figures 4 and 5.

If a low offset amplifier such as the MAX400M (10μV max.) or MAX400C (15μV max.) is used, excellent performance can be obtained without any trimming. Figures 4(a), 4(b), and 4(c) show how to connect the AD565A for both unipolar and bipolar voltage outputs. The connections for the AD566A are shown in figures 5(a), 5(b), and 5(c). The preferred trimming techniques are shown for both offset and gain adjustments if required. Substituting a fixed 50Ω resistor in place of the 100Ω potentiometers, the unipolar zero offset error will be within ±½LSB (plus op-amp offset), and full scale accuracy will be within 0.1% (0.25% max.). Similarly, the bipolar zero offset error will be typically within ±2LSB (0.05%).

Unipolar configuration zero and gain adjustment

Figures 4(a) and 5(a) show the configurations for a unipolar 0 to +10V output. The bipolar offset resistor is tied to ground if zero offset adjustment is not required.

Turn all bits OFF and adjust potentiometer R1 until DAC output reads 0.000V (1LSB = 2.44mV). If offset adjust is not required tie pin 8 to ground.

Next, turn all bits ON and adjust gain potentiometer R2 until DAC output reads 9.9976V (full scale -1 LSB). If full scale of 10.2400V is required (2.5mV/bit) then insert a 120Ω resistor between op-amp output and pin 10 (10V span resistor).

High Speed 12-Bit Monolithic D/A Converters

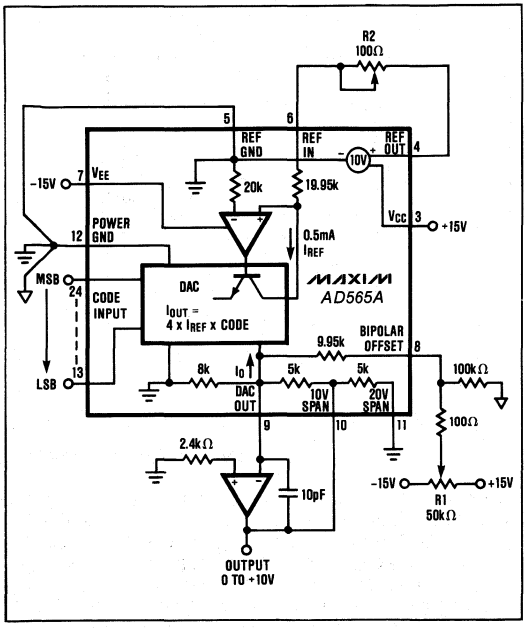


Figure 4(a). AD565A 0 to +10V Unipolar Voltage Output

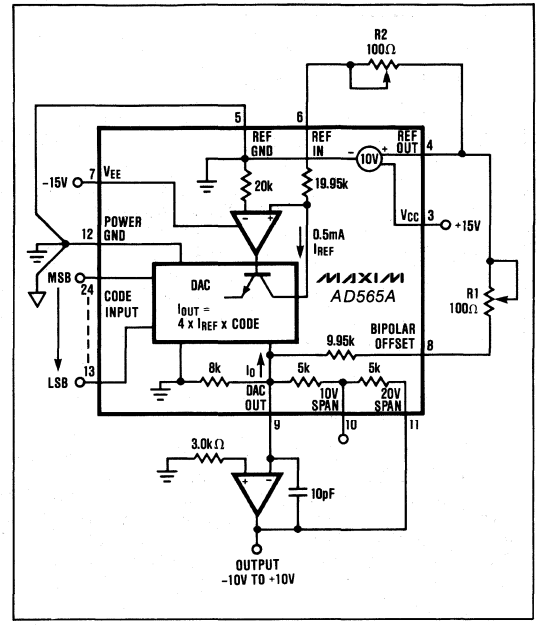


Figure 4(c). AD565A ±10V Bipolar Voltage Output

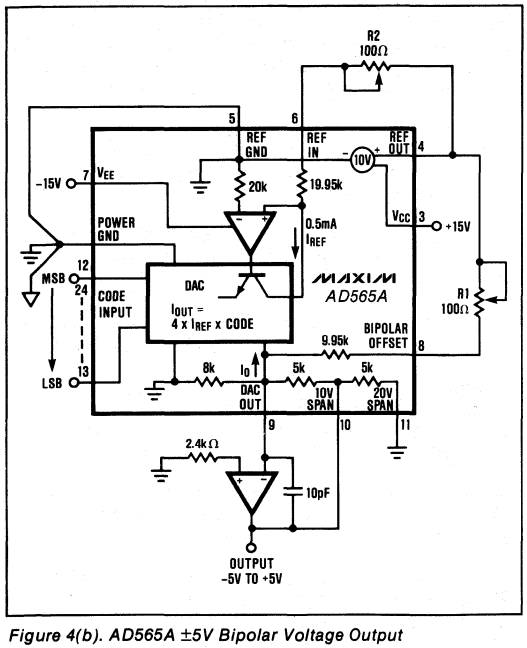


Figure 4(b). AD565A ±5V Bipolar Voltage Output

Bipolar configuration offset and gain adjustment

Figures 4(b) and 5(b) show how to configure the DAC to produce an output from -5.000V (all 0's) to +4.9976V (all 1's).

First turn OFF all bits, adjust potentiometer R1 to give -5.000V output.

Then turn all bits ON. Adjust potentiometer R2 to give a DAC output of +4.9976V.

Other voltage ranges

The AD565A and AD566A can easily be configured for unipolar 0 to +5V range or ±2.5V and ±10V bipolar ranges by using the 20V span resistor (pin 11). Connecting pin 9 and 11 together a 5V span can be developed by connecting pin 10 to the output of the op-amp and the bipolar offset resistor to either ground for the unipolar 0 to +5V range or to REF OUT for the bipolar ±2.5V range. For the ±10V (20V span) connect pin 11 to the op-amp output and the bipolar offset resistor to potentiometer R1 as shown in figures 4(c) and 5(c).

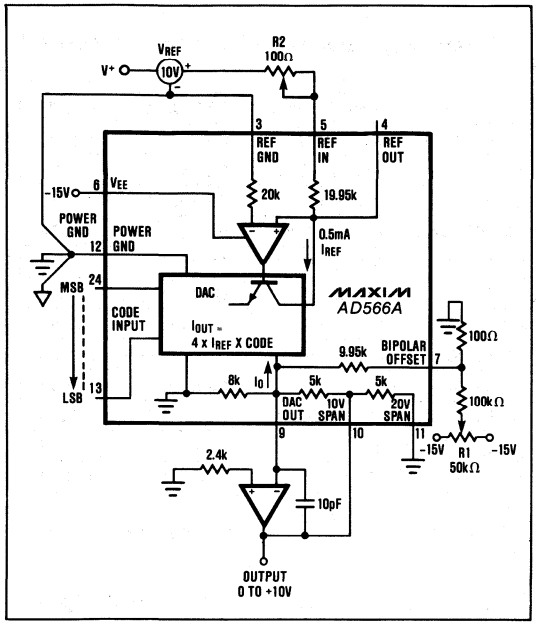


Figure 5(a). AD566A 0 to +10V Unipolar Voltage Output

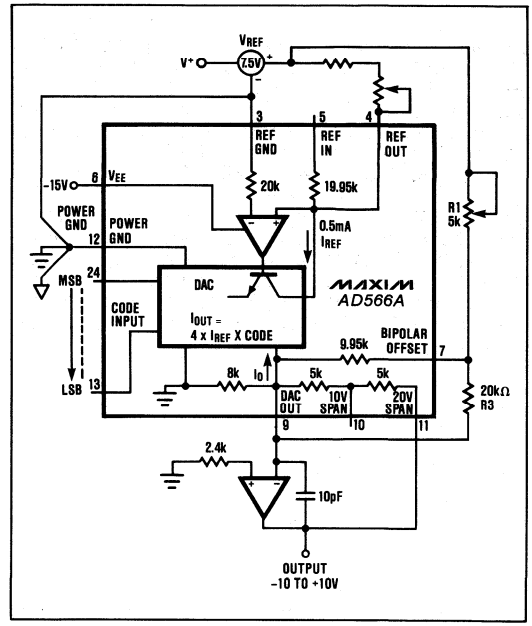


Figure 5(c). AD566A ±10V Bipolar Voltage Output

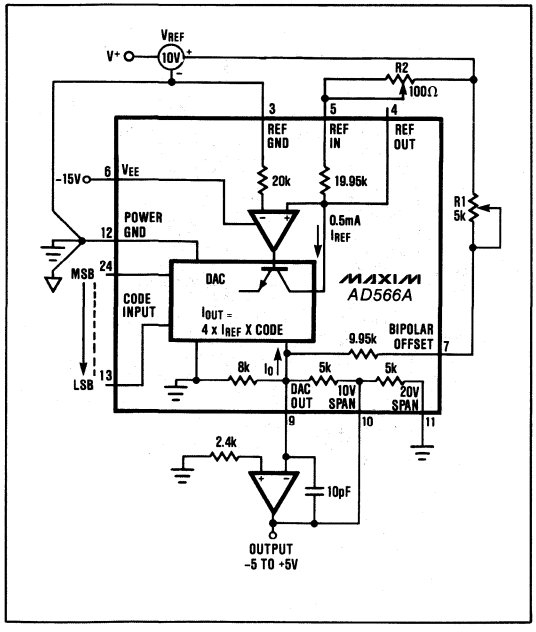


Figure 5(b). AD565A ±5V Bipolar Voltage Output

Grounding

The AD565A and AD566A have two ground pins, Reference GND and Power GND. The current in the power ground varies with the digital input code and should be connected to the local ground, digital ground or power ground. The reference ground is the ground point for the internal reference amplifier and should be connected to the system's "high quality" ground, usually called signal or analog ground.

Internal/External Reference Use

The AD565A has an internal reference whereas the AD566A requires an external reference. The AD565A can be used with either the internal reference or an external reference. With an external 10V reference there may not be enough adjustment range to accommodate a reference that does not match the internal reference voltage. The AD566A is recommended for applications that need to be driven with an external reference.

The internal reference of the AD565A is a low noise buried zener diode that is buffered by an internal amplifier whose gain is trimmed for absolute accuracy and temperature stability. The performance of the AD565A DAC is tested and specified using the internal reference.

High Speed 12-Bit Monolithic D/A Converters

In addition, the internal reference of the AD565A has sufficient buffering to drive the internal DAC (typically 0.5mA to REF IN and 1.0mA to Bipolar Offset, if used) plus an additional 1.5mA for driving external circuits. The temperature coefficient of the reference output voltage is comparable to the DAC's full scale TC for the particular grade of AD565A.

For the AD566A an external reference is required that should have a low temperature coefficient, such as the AD581, AD584, or precision references such as the AD2700 and AD2710. For the ultimate in performance use the MAX670 and MAX671, which have kelvin sense connections for both the +10V reference output and ground return.

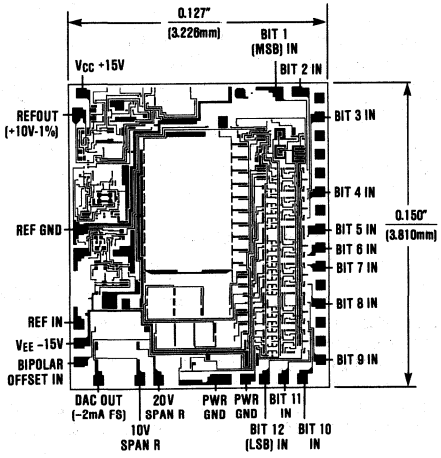
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD566AJN	0°C to +70°C	Plastic DIP	±½LSB
AD566AJD	0°C to +70°C	Ceramic	±½LSB
AD566AJQ	0°C to +70°C	CERDIP**	±½LSB
AD566AJCWG	0°C to +70°C	Small Outline	±½LSB
AD566AKN	0°C to +70°C	Plastic DIP	±¼LSB
AD566AKD	0°C to +70°C	Ceramic	±¼LSB
AD566AKQ	0°C to +70°C	CERDIP**	±¼LSB
AD566AKCWG	0°C to +70°C	Small Outline	±¼LSB
AD566ASD	-55°C to +125°C	Ceramic	±½LSB
AD566ASQ	-55°C to +125°C	CERDIP**	±½LSB
AD566ATD	-55°C to +125°C	Ceramic	±¼LSB
AD566ATQ	-55°C to +125°C	CERDIP**	±¼LSB

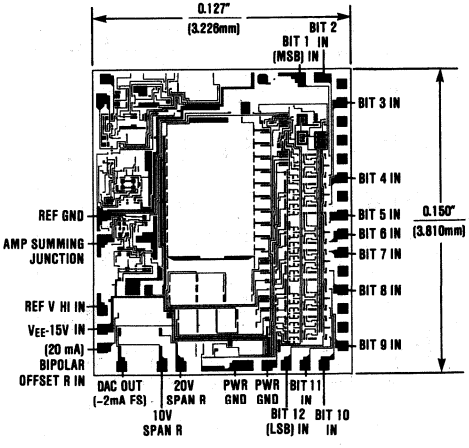
* *All devices — 24 lead packages*
** *MAXIM reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography

AD565A



AD566A



CMOS 8-Bit DAC with Output Amplifier

General Description

The AD7224 is a precision voltage-output CMOS digital-to-analog converter (DAC) which includes an output amplifier on chip. Only an external reference source is required for operation and the fully specified accuracy is achieved with no external trims.

Double buffered interface logic is included to allow simultaneous updating in systems which have several DAC channels in operation. Control is provided by $\overline{CS}$, $\overline{WR}$, and $\overline{LDAC}$ (Load DAC) inputs. A $\overline{RESET}$ input is provided which acts as a zero override. All logic inputs are compatible with TTL and 5V CMOS logic levels.

Specified Performance is guaranteed for reference inputs ranging from +2V to +12.5V when using dual supplies. With a +10V reference the performance is also specified for single supply operation. The DAC output can drive +10V into a 2kΩ load.

Applications

Automatic Calibration

Motion Control

Digital Attenuators

Function Generators

Features

- **Voltage Output**
- **Complete DAC with Output Amplifier**
- **Single or Dual Supply Operation**
- **1 LSB Unadjusted Error**
- **Double Buffered Logic Inputs**

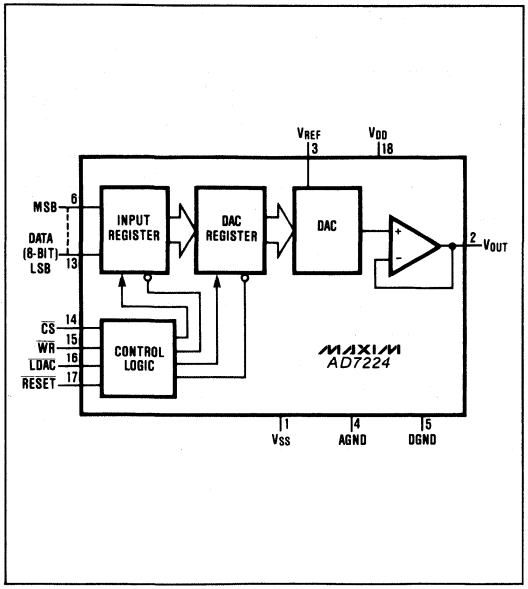
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7224KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7224LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7224C/D	0°C to +70°C	Dice	±2 LSB
AD7224KCWN	0°C to +70°C	Wide S.O.	±2 LSB
AD7224LCWN	0°C to +70°C	Wide S.O.	±1 LSB
AD7224BQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7224CQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7224TD	-55°C to +125°C	Ceramic	±2 LSB
AD7224UD	-55°C to +125°C	Ceramic	±1 LSB
AD7224TQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7224UQ	-55°C to +125°C	CERDIP**	±1 LSB

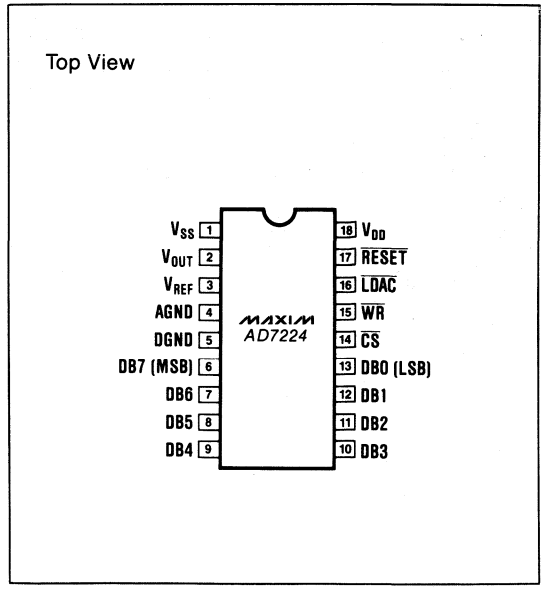
* *All devices—18 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Functional Diagram



Pin Configuration



CMOS 8-Bit DAC with Output Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
AGND to DGND ..... -0.3V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD} + 0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}

Power Dissipation (Any Package) to +75°C 450mW
Derating above +75°C ..... 6mW/°C
Operating Temperature
AD7224K/L ..... 0°C to +70°C
AD7224A/B ..... -25°C to +85°C
AD7224T/U ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering 10 secs) ..... +300°C

The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{REF} = +10V V_{DD} = +15V ± 5%	AD7224L/C/U AD7224K/B/T			±1 ±2	LSB
Relative Accuracy		AD7224L/C/U AD7224K/B/T				±½ ±1	LSB
Differential Nonlinearity		Guaranteed Monotonic				±1	LSB
Full Scale Error		AD7224L/C/U AD7224K/B/T				±1 ±1½	LSB
Full Scale Temperature Coefficient		V_{REF} = +10V			±5		ppm/°C
Zero Code Error		AD7224L/C/U AD7224K/B/T				±20 ±30	mV
Zero Code Temperature Coefficient		AD7224L/C/U AD7224K/B/T			±30 ±50		μV/°C
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}			2		V_{DD} - 4	V
Reference Input Resistance	V_{REF}			8			kΩ
Reference Input Capacitance (Code Dependent, Note 2)	C_{REF}	DAC at full scale code.				100	pF
DIGITAL INPUTS							
Digital Input High Voltage	V_{INH}			2.4			V
Digital Input Low Voltage	V_{INL}					0.8	V
Digital Input Leakage Current		V_{IN} = 0V or V_{DD}				±1	μA
Digital Input Capacitance (Note 2)						8	pF

ELECTRICAL CHARACTERISTICS—AD7224, Dual Supply Operation (Continued)

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V) (Note 1), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/µs
Voltage Output Settling Time (Note 5)		To 1/2 LSB, V_{REF} = +10V		2	5	µs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+11.4		+16.5	V
V_{SS} Range		For Specified Performance	-4.5		-5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			4 6	mA
Negative Supply Current	I_{SS}	Outputs unloaded, at V_{INL}/V_{INH} T_A = 25°C Over Temp			3 5	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C Over Temp	90 100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C Over Temp	150 200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C Over Temp	150 200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C Over Temp	150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C Over Temp	150 200			ns

Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Note 5: Positive or negative full scale change.

CMOS 8-Bit DAC with Output Amplifier

ELECTRICAL CHARACTERISTICS—AD7224, Single Supply Operation

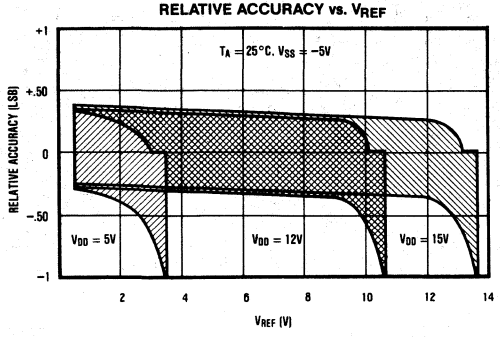
(V_{DD} = +15V ± 5%, V_{SS} = AGND = DGND = 0V, V_{REF} = +10V (Note 1), Over Temperature unless otherwise stated.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error					±2	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
REFERENCE INPUT						
Reference Input Resistance	R_{REF}		8			kΩ
Reference Input Capacitance (Code Dependent)(Note 2)	C_{REF}	DAC at full scale code			100	pF
DIGITAL INPUTS						
Digital Input High Voltage	V_{INH}		2.4			V
Digital Input Low Voltage	V_{INL}				0.8	V
Digital Input Leakage Current		V_{IN} = 0V to V_{DD}			±1	μA
Digital Input Capacitance (Note 2)					8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate (Note 2)			2.5	10		V/μs
Output Settling Time (Note 2)		To 1/2 LSB, Positive FS Chg		2	5	μs
		To 1/2 LSB, Negative FS Chg		3	8	μs
Digital Feedthrough (Notes 3, 4)		All 0's to all 1's code change, V_{REF} = 0V		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+14.25		+15.75	V
Positive Supply Current	I_{DD}	Outputs unloaded, at V_{INL}/V_{INH}, T_A = 25°C			4	mA
		Outputs unloaded, at V_{INL}/V_{INH}, Over Temp			6	mA
SWITCHING CHARACTERISTICS (Note 2)						
Chip Select to Write Setup Time	t_{CS}		0			ns
Load DAC to Write Setup Time	t_{LS}		0			ns
Chip select to Write Hold Time	t_{CH}		0			ns
Load DAC to Write Setup Time	t_{LH}		0			ns
Data Valid to Write Setup Time	t_{DS}	T_A = 25°C	90			ns
		Over Temp	100			ns
Data Valid to Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C	150			ns
		Over Temp	200			ns
Chip Select Pulse Width	t_{CW}	T_A = 25°C	150			ns
		Over Temp	200			ns
Reset Pulse Width	t_{RS}	T_A = 25°C	150			ns
		Over Temp	200			ns
Load DAC ($\overline{LDAC}$) Pulse Width	t_{LD}	T_A = 25°C	150			ns
		Over Temp	200			ns

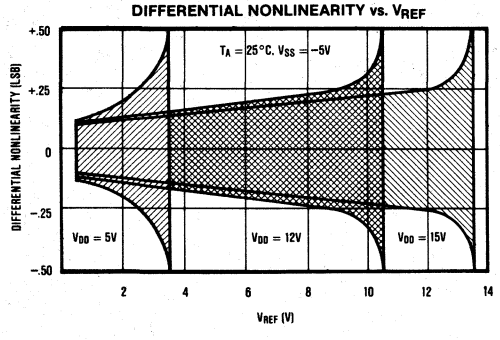
Note 1: Maximum possible reference voltage.
Note 2: Sample tested at 25°C to ensure compliance.
Note 3: Guaranteed, but not 100% production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Typical Operating Characteristics

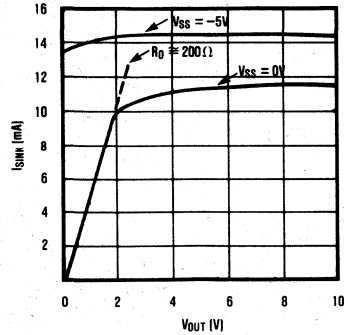
RELATIVE ACCURACY vs. V_{REF}



DIFFERENTIAL NONLINEARITY vs. V_{REF}



OUTPUT SINK CURRENT vs. V_{OUT}



Detailed Description

D/A Section

The AD7224 contains an 8-bit digital-to-analog converter that operates in the voltage output mode. The output voltage is of the same polarity as the external reference voltage thus allowing single supply operation. A DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2V to +12.5V.

The DAC consists of a stable thin-film resistor R-2R ladder and eight NMOS single pole, double-throw switches. A simplified circuit diagram is shown in Figure 1.

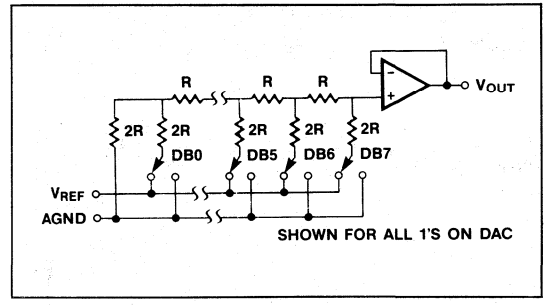


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and varies from 8kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low impedance under changing load conditions. Capacitance at the reference terminal is also code dependent and typically varies from 25pF to 50pF.

The V_{OUT} pin can be considered as a digitally-programmable voltage source with the output defined by:

$$V_{OUT} = D \cdot V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

Output Buffer Amplifier

The DAC's voltage output is buffered by a unity-gain CMOS voltage follower that slews at greater than 2.5V/μs. This amplifier is capable of driving a 2kΩ load to +10V. When driving a 2kΩ load in parallel with 100pF with full-scale transitions (0V to +10V or +10V to 0V), the output settles to 1/2LSB in less than 5μs. Typical dynamic response and settling performance of the AD7224 is shown in Figures 2 through 7.

The AD7224 can be operated single or dual supply. In single supply operation, Maxim's AD7224 can sink and source up to 5mA.

CMOS 8-Bit DAC with Output Amplifier

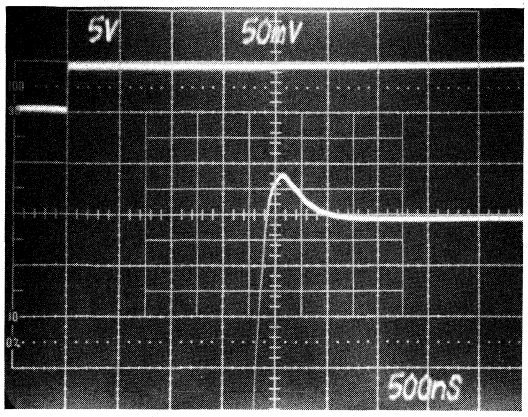


Figure 2. Positive Settling Time with V_{DD} = +15V, V_{SS} = -5V.

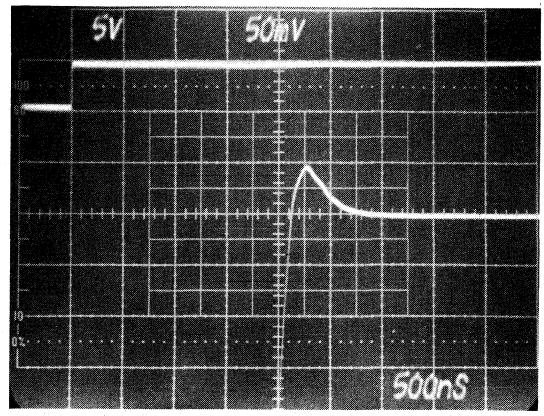


Figure 3. Positive Settling Time with V_{DD} = +15V, V_{SS} = 0V.

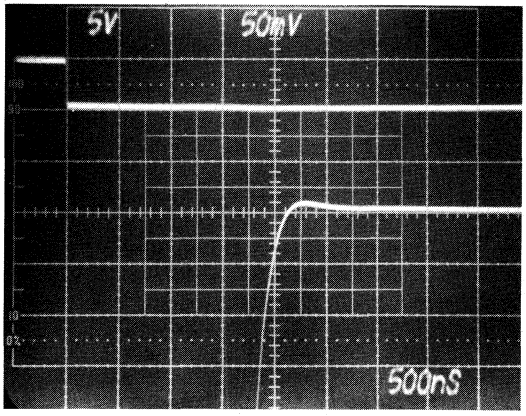


Figure 4. Negative Settling Time with V_{DD} = +15V, V_{SS} = -5V.

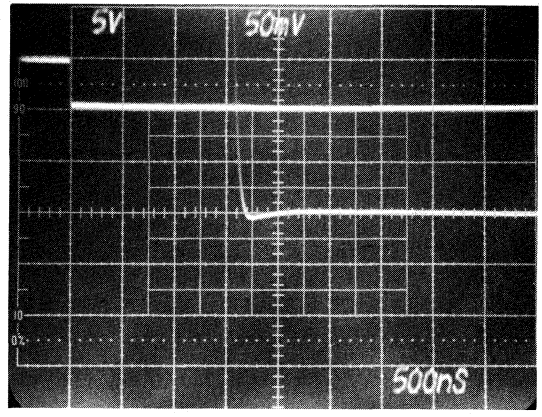


Figure 5. Negative Settling Time with V_{DD} = +15V, V_{SS} = 0V.

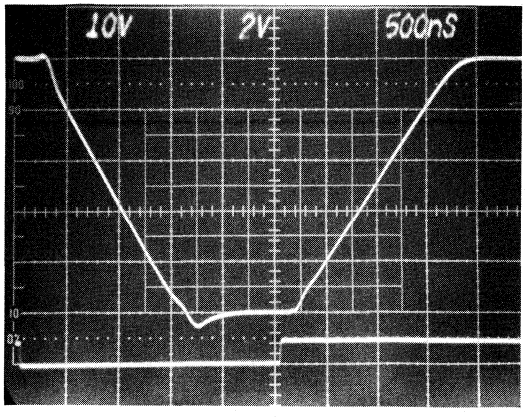


Figure 6. Dynamic Response with V_{DD} = +15V, V_{SS} = -5V.

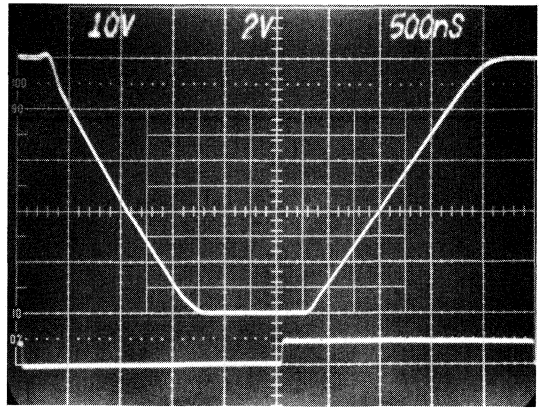


Figure 7. Dynamic Response with V_{DD} = +15V, V_{SS} = 0V.

A simplified circuit diagram of the output buffer is shown is Figure 8. Input common-mode range to V_{SS} is provided by a PMOS input structure. The improved output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive V_{OUT} to within typically +15mV of the negative supply (V_{SS}). Maxim's improved buffer circuitry allows the output to sink and source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to GND, so that zero error is kept at or under 1/2LSB (V_{REF} = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

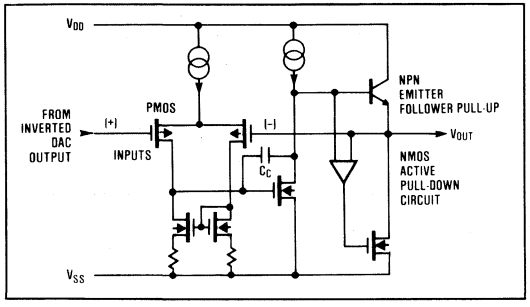


Figure 8. Simplified Output Buffer Circuit

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. Power supply current, I_{DD} and I_{SS}, are specified for TTL input levels. The supply currents are somewhat dependent on input logic level and are highest when the AD7224 is driven from TTL, however, they can be significantly reduced if the inputs are driven as close to +5V as possible.

Table 1 shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input to the DAC register. Only the data held in the DAC register will determine the converter's analog output.

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW," the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW." The rising edge of the $\overline{WR}$ input latches input data.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line overrides input data for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on the $\overline{RESET}$ will latch all 0's into the registers, with the output remaining at 0V after the reset pulse has been removed. The $\overline{RESET}$ line can be used to force 0V on the output at power-up, and is also useful as a zero override in system calibration cycles. Figure 9 shows the input control logic for the AD7224.

Table 1. AD7224 Truth Table

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded with all Zeros
↓	H	H	H	Both Registers Latched with all Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

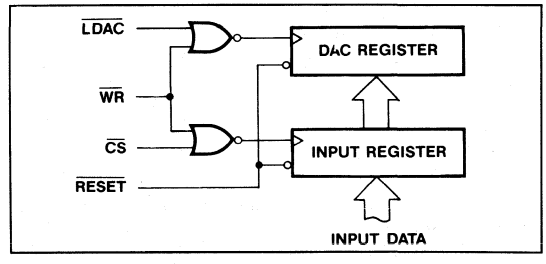


Figure 9. Input Control Logic

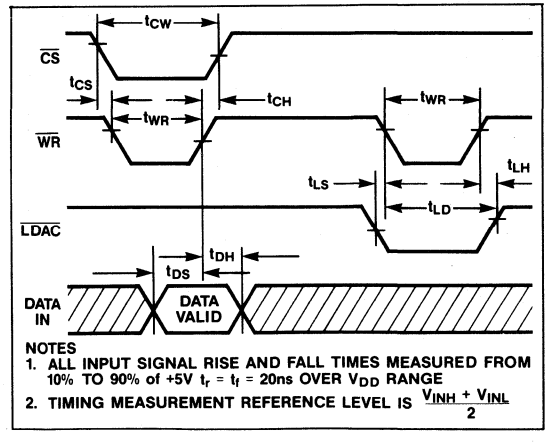


Figure 10. Write Cycle Timing Diagram

CMOS 8-Bit DAC with Output Amplifier

Applications Information

Power Supply and Reference Operating Ranges

The AD7224 is fully specified to operate with V_{DD} between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. Eight bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. The AD7224 is specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between the DAC output, the reference input, and the digital inputs. This is particularly important if the reference is driven from an AC source.

Unipolar Output

In unipolar operation, the output voltage and the reference input are the same polarity. The unipolar circuit configuration is shown in Figure 11. A slight increase in zero error occurs when the AD7224 is operated from a single supply (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to DGND. The unipolar code table is given in Table 2.

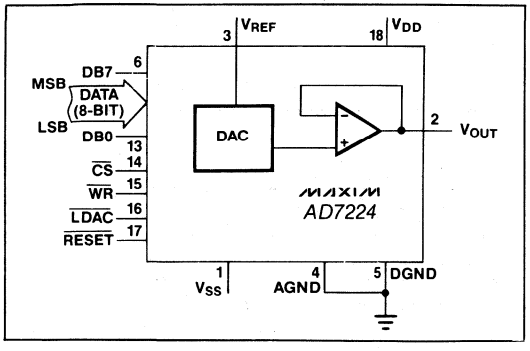


Figure 11. Unipolar Output Circuit

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Bipolar Output

The DAC output may be configured for bipolar operation using the circuit in Figure 12. Only one op-amp and two resistors are required. With R1 = R2:

$$V_{OUT} = V_{REF} \cdot (2D - 1)$$

where D is a fractional representation of the digital word in the DAC regiser.

Table 3 shows the digital code versus output voltage for the circuit in Figure 12.

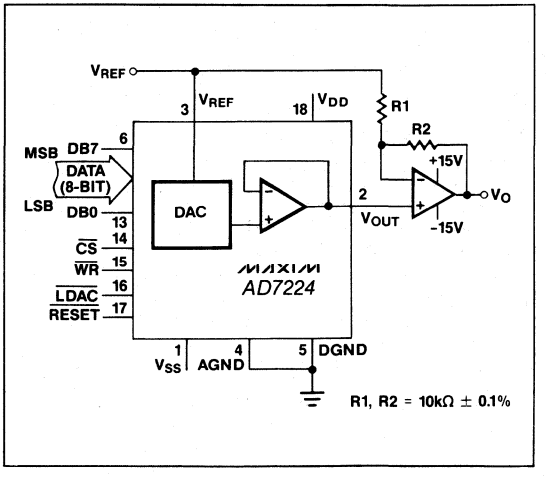


Figure 12. Bipolar Output Circuit

Table 3. Bipolar (Offset Binary) Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary non-zero output voltage for a "zero" input code. This is shown in Figure 13. The output voltage at V_{OUT} is:

$$V_{OUT} = V_{BIAS} + (D \cdot V_{IN})$$

where D is a fractional representation of the digital input word and can vary from 0 to 255/256. For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}-V_{REF} which must be at least 4V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

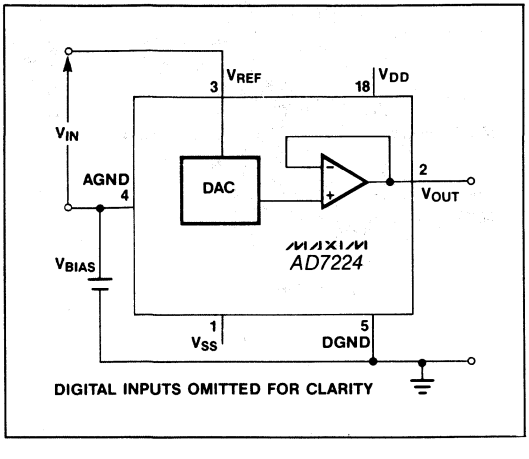


Figure 13. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7224 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 14 shows a technique for applying a sinewave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

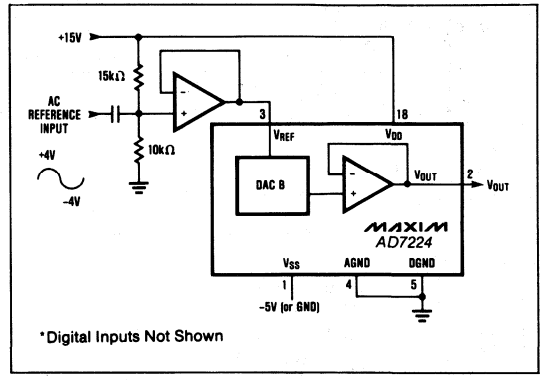


Figure 14. AC Reference Input Circuit

Generating V_{SS}

The performance of the AD7224 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 15.

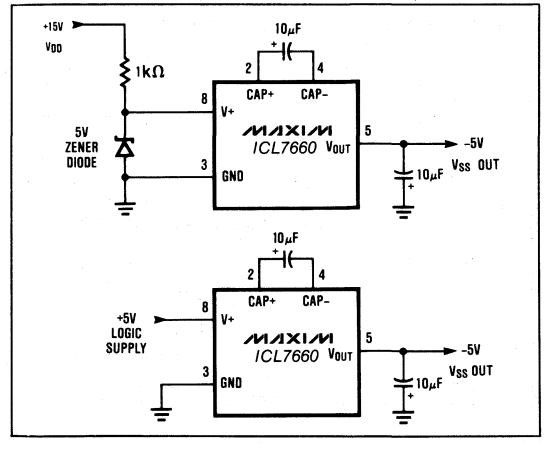


Figure 15. Generating -5V for V_{SS}

CMOS 8-Bit DAC with Output Amplifier

Microprocessor Interfacing

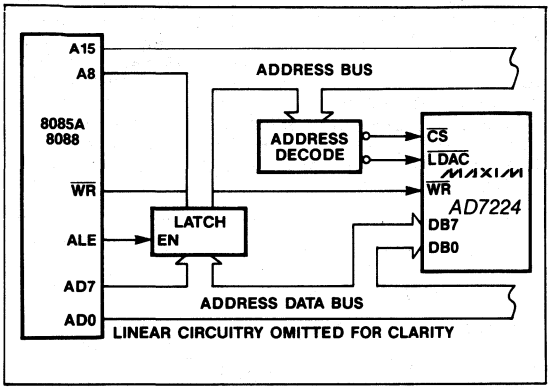


Figure 16. AD7224 to 8085A/8088 Interface

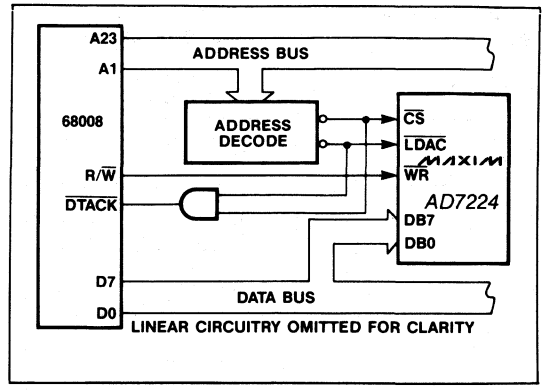


Figure 19. AD7224 to 68008 Interface

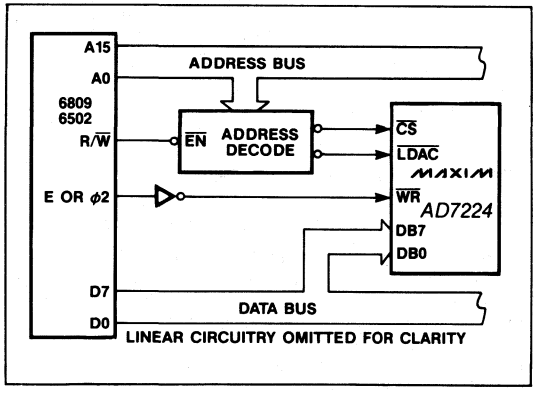


Figure 17. AD7224 to 6809/6502 Interface

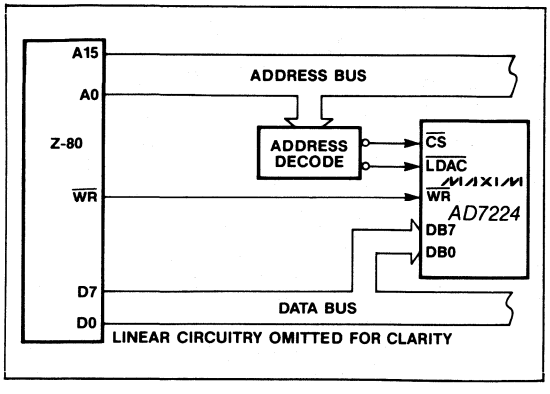
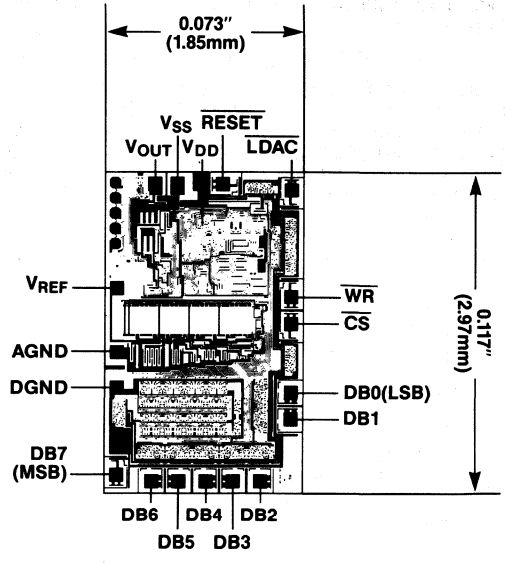


Figure 18. AD7224 to Z-80 Interface

Chip Topography



MAXIM

CMOS Quad 8-Bit D/A Converters

General Description

Maxim's AD7225 and AD7226 each contain four 8-bit voltage output digital-to-analog converters (DACs). They include output buffer amplifiers and input logic for simple microprocessor and TTL/CMOS interfaces. 8-bit performance is achieved over the full operating temperature range without external trimming.

The AD7225 contains double-buffered logic inputs which allow all analog outputs to be simultaneously updated using one control signal. There are also four separate reference inputs so that the range of each DAC can be independently set.

The AD7226 has separate input registers for each of its four DACs. Data is transferred into an input register from a common 8-bit TTL/CMOS compatible input port. Address inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. All DACs share a common reference input.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor Controlled Calibration

Features

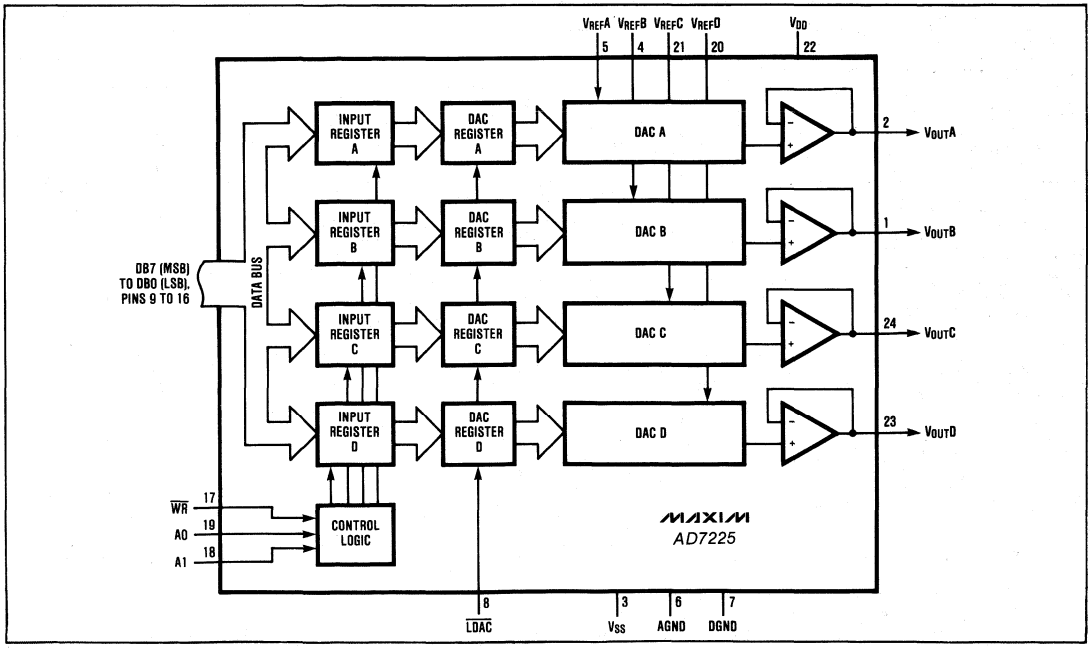
- **Buffered Voltage Output**
- **Double-Buffered Inputs (AD7225)**
- **Microprocessor and TTL/CMOS Compatible**
- **Operates from Single or Dual Supplies**
- **Requires No External Adjustments**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7225KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7225KCWG	0°C to +70°C	Small Outline	±2 LSB
AD7225LN	0°C to +70°C	Plastic DIP	±1 LSB
AD7225LCWG	0°C to +70°C	Small Outline	±1 LSB
AD7225KC/D	0°C to +70°C	Dice	±2 LSB
AD7225BQ	-25°C to +85°C	CERDIP	±2 LSB
AD7225CQ	-25°C to +85°C	CERDIP	±1 LSB
AD7225TQ	-55°C to +125°C	CERDIP	±2 LSB
AD7225UQ	-55°C to +125°C	CERDIP	±1 LSB
AD7226KN	0°C to +70°C	Plastic DIP	±2 LSB
AD7226KCWP	0°C to +70°C	Small Outline	±2 LSB
AD7226KC/D	0°C to +70°C	Dice	±2 LSB
AD7226BQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7226TD	-55°C to +125°C	Ceramic	±2 LSB
AD7226TQ	-55°C to +125°C	CERDIP**	±2 LSB

** AD7225 — 24 lead package, AD7226 — 20 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Functional Block Diagram



CMOS Quad 8-Bit D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to AGND ..... -7V, V_{DD}
V_{SS} to DGND ..... -7V, V_{DD}
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
V_{REF} to AGND ..... -0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}

Power Dissipation (Any Package) to +75°C 500mW
Derating above +75°C ..... 2mW/°C
Operating Temperature
Commercial (AD722XK/L) ..... 0°C to +70°C
Industrial (AD722XB/C) ..... -25°C to +85°C
Military (AD722XT/U) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +300°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Dual Supply Specifications

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), Over Temperature unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error		V_{DD} = +15V±5%, V_{REF} = +10V: AD7225LN/CQ/UQ All other devices			±1 ±2	LSB
Relative Accuracy		AD7225LN/CQ/UQ All Other Devices			±½ ±1	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
Full Scale Error		AD7225LN/CQ/UQ AD7225KN/BQ/TQ All other devices			±½ ±1 ±1½	LSB
Full Scale Temperature Coefficient		V_{REF} = +10V		±5		ppm/°C
Zero Code Error		AD7225LN/CQ/UQ, T_A = +25°C Over Temp. AD7225KN/BQ/TQ, T_A = +25°C All other devices, Over Temp.			±15 ±20 ±20 ±30	mV
Zero Code Temperature Coefficient				±30		µV/°C
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		2		V_{DD} - 4	V
Reference Input Resistance	R_{REF}	AD7225 AD7226	11 2			kΩ
Reference Input Capacitance (Code Dependent, Note 3)	C_{REF}	AD7225 AD7226	 65		100 300	pF
Channel-to-Channel Isolation		V_{REF} = 10kHz, 10V_{P-P} (Note 2)	-60			dB
AC Feedthrough		**V_{REF} = 10kHz, 10V_{P-P} (Note 2, 4)**	-70			dB
DIGITAL INPUTS						
Digital Input High Voltage	V_{INH}		2.4			V
Digital Input Low Voltage	V_{INL}				0.8	V
Digital Input Leakage Current		**V_{IN} = 0V or V_{DD}**			±1	µA
Digital Input Capacitance		**(Note 2)**			8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		**(Note 2)**	3			V/µs
Voltage Output Settling Time (Pos. or Neg. Full Scale Change)		to ½LSB, V_{REF} = +10V, 2kΩ and 100pF Load **(Note 2)**			4	µs
Digital Feedthrough and Crosstalk		All 0's to 1's code change (Note 4)		50		nV-s
Output Load Resistance		V_{OUT} = +10V	2			kΩ

Note 1: The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.
Note 2: Sample tested at +25°C to ensure compliance.
Note 3: Guaranteed by design. Not production tested.
Note 4: Feedthrough is reduced by connecting the metal lid on the ceramic package (suffix D) to DGND. (AD7226 only)

ELECTRICAL CHARACTERISTICS Dual Supply Specifications (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+11.4		+16.5	V
Positive Supply Current (Outputs Unloaded)	I_{DD}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			10 12 13	mA
Negative Supply Current (Outputs Unloaded)	I_{SS}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			-9 -10 -11	mA
SWITCHING CHARACTERISTICS (Note 2)						
Address to Write Setup Time	t_{AS}	Over Temp.	0			ns
Address to Write Hold Time	t_{AH}	Over Temp. AD7225 AD7226	0 10			ns
Data Valid to Write Setup Time	t_{DS}	AD7225, T_A = +25°C Over Temp. AD7226, T_A = +25°C Over Temp.	70 90 90 100			ns
Data Valid to Write Hold Time	t_{DH}	Over Temp.	10			ns
Write Pulse Width	t_{WR}	AD7225, T_A = +25°C AD7225KN/BQ/LN/CQ, Over Temp. AD7225TQ/UQ, Over Temp. AD7226, T_A = +25°C Over Temp.	95 120 150 150 200			ns
Load DAC ($\overline{LDAC}$) Pulse Width (AD7225 Only)	t_{LC}	AD7225, T_A = +25°C AD7225KN/BQ/LN/CQ, Over Temp. AD7225TQ/UQ, Over Temp.	95 120 150			ns

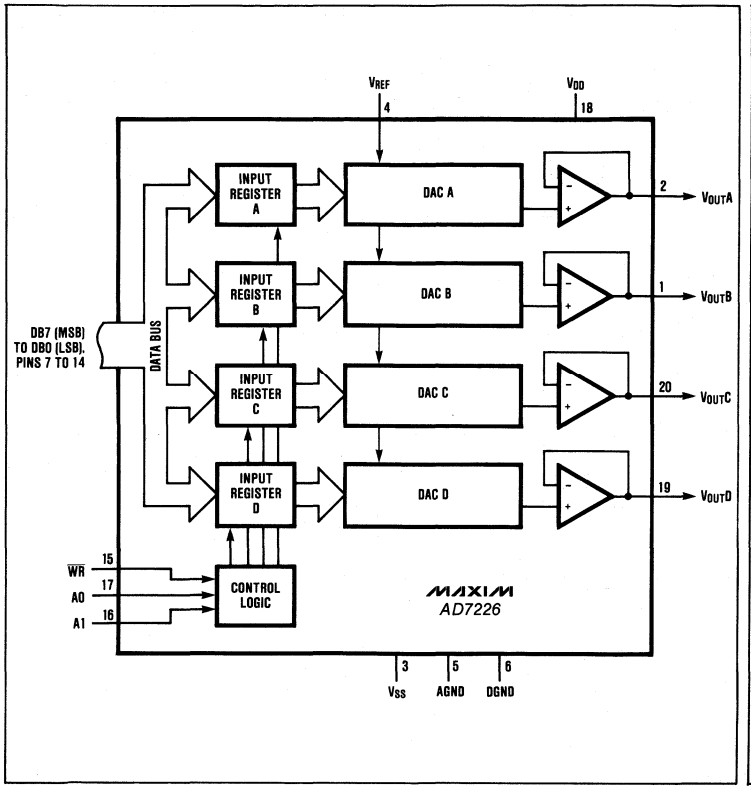
ELECTRICAL CHARACTERISTICS Single Supply Specifications

(V_{DD} = +15V ± 5%, V_{SS} = AGND = DGND = 0V, V_{REF} = +10V, Over Temperature unless otherwise stated.)

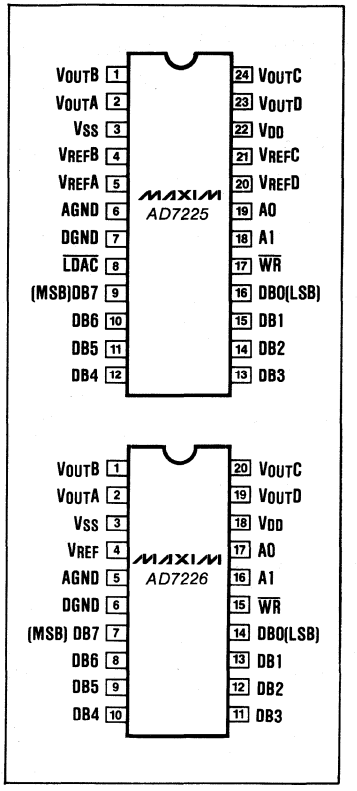
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error		AD7225LN/CQ/UQ All other devices			±1 ±2	LSB
Differential Nonlinearity		Guaranteed Monotonic			±1	LSB
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		2		V_{DD}-4	V
Reference Input Resistance	R_{REF}	AD7225 AD7226	11 2			kΩ
Reference Input Capacitance (Code Dependent, Note 3)	C_{REF}	AD7225 AD7226	 65		100 300	pF
Channel-to-Channel Isolation		V_{REF} = 10kHz, 10V_{P-P} (Note 2)	-60			dB
AC Feedthrough		V_{REF} = 10kHz, 10V_{P-P} **(Note 2, 4)**	-70			dB
DIGITAL INPUTS — All Specifications Are The Same as For Dual Supply Operation						
DYNAMIC PERFORMANCE — All Specifications Are The Same as For Dual Supply Operation						
POWER SUPPLIES						
V_{DD} Range		For Specified Performance	+14.25		+15.75	V
Positive Supply Current Output Unloaded	I_{DD}	AD7225KN/BQ/LN/CQ AD7225TQ/UQ AD7226			10 12 13	mA
SWITCHING CHARACTERISTICS — All Specifications Are The Same as For Dual Supply Operation						

CMOS Quad 8-Bit D/A Converters

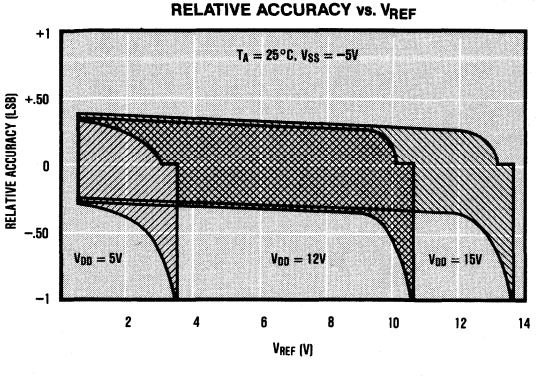
Functional Block Diagram (AD7226)

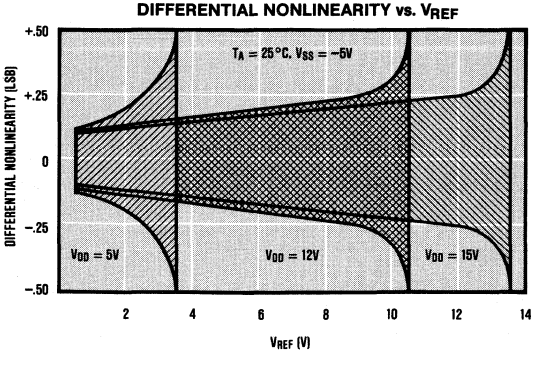


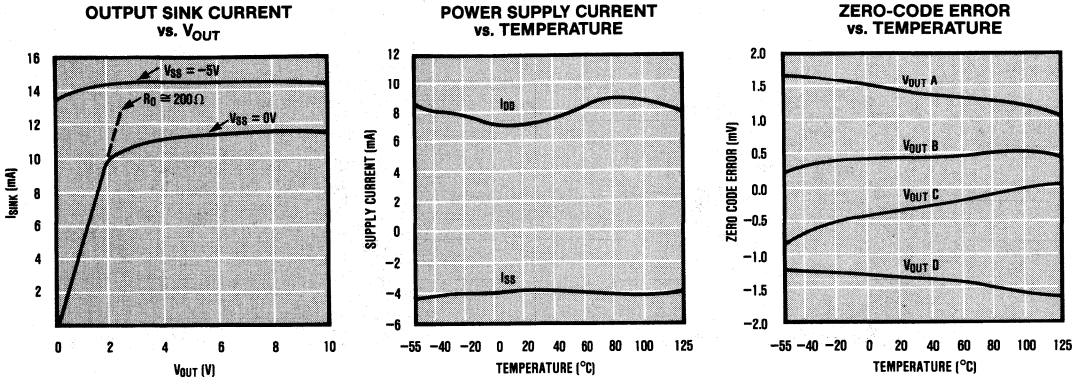
Pin Configurations



Typical Operating Characteristics







Detailed Description

The AD7225 and AD7226 have four matched voltage output digital-to-analog converters (DACs). The DAC's are "inverted" R-2R ladder networks which convert 8 bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the AD7225 has a separate reference input whereas in the AD7226, all reference inputs are tied together. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

V_{REF} Input

The voltage at V_{REF} sets the full-scale output of the DAC. The input impedance of the V_{REF} input(s) is code dependent. The lowest value, approximately 11kΩ for the AD7225 and 2kΩ for the AD7226, occurs when the input code is 01010101. The maximum value is infinity, which occurs when the input code is 00000000. Because the input resistance at V_{REF} is code dependent, the DAC's reference sources must have an output impedance of no more than 20Ω for the AD7225 and 4Ω for the AD7226, to maintain output linearity. The input capacitance at V_{REF} is also code dependent and typically varies from 15pF to 35pF for the AD7225 and 100pF to 250pF for the AD7226.

V_{OUT}A, B, C, or D can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_B \times V_{REF}/256,$$

where N_B is the numeric value of the DAC's binary input code.

Ouput Buffer Amplifiers

All AD7225/26 voltage outputs are internally buffered by precision unity gain followers which slew at greater than 3V/μs. When driving 2kΩ in parallel with 100pF with full scale transitions (0V to +10V or +10V to 0V), the output settles to ±1/2LSB in less than 4μs. The buffers will also drive 2kΩ in parallel with 3500pf to 10V levels without oscillation. Typical dynamic response and settling performance of the AD7225 and AD7226 is shown in Figure 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to V_{SS} is provided by a PMOS input structure. The improved

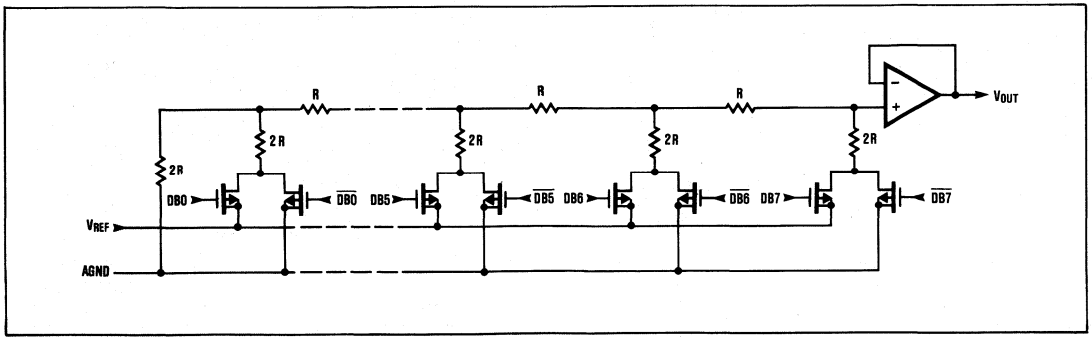


Figure 1. Simplified DAC Circuit Diagram

CMOS Quad 8-Bit D/A Converters

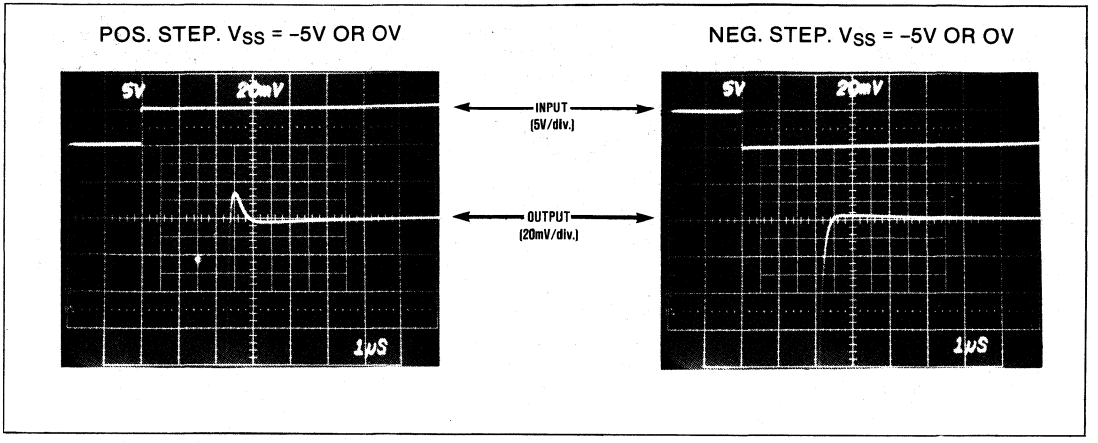


Figure 2. Positive and Negative Settling Times, V_{SS} = 0V or -5V

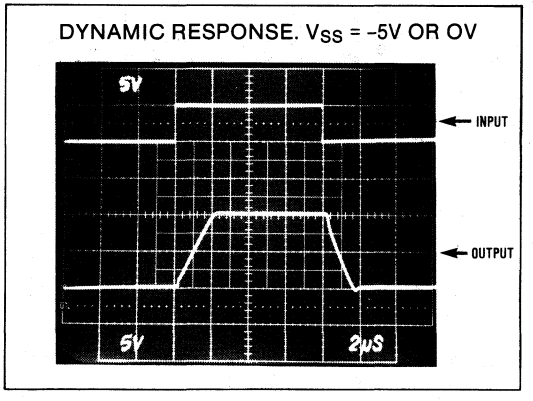


Figure 3. Dynamic Response, V_{SS} = 0V or -5V

output circuitry incorporates a Maxim proprietary pull-down circuit to actively drive V_{OUT} to within typically +15mV of the negative supply (V_{SS}). The buffer circuitry allows each DAC output to sink, as well as source, up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to GND, so that zero error is kept at or under 1/2LSB (V_{REF} = +10V). A plot of output sink current versus output voltage is shown in the Typical Operating Characteristics section.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however power supply currents, I_{DD} and I_{SS}, are somewhat dependent on input logic level. Supply currents are specified for TTL input levels (worst case) but are significantly reduced when the logic inputs are driven as close to V_{DD} and DGND as possible.

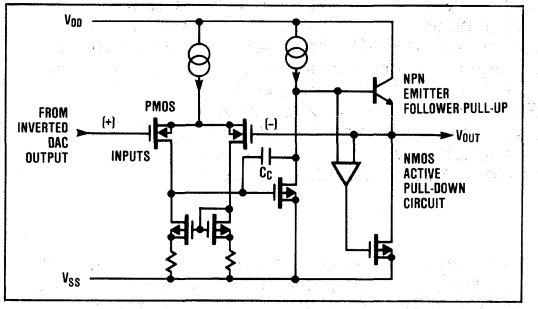


Figure 4. Simplified Output Buffer Circuit

Address lines A0 and A1 select which DAC receives data from the input port. When $\overline{WR}$ is low, the input register of the addressed DAC is transparent. The data is then latched when $\overline{WR}$ goes high. Figure 5 shows the input control logic for the AD7225 and AD7226. Table 1 lists the channel addresses.

The AD7226's four DAC outputs represent the data held in four 8 bit input registers. The AD7225 differs from the AD7226 in that in addition to the input registers, there is a separate DAC register for each DAC as well. A DAC's analog output is based only on the contents of its DAC register. Data is transferred from the input registers to the DAC registers by the $\overline{LDAC}$ input. When $\overline{LDAC}$ is LOW, all four DAC registers are transparent to the input registers so that all DACs are updated simultaneously. With $\overline{LDAC}$ held LOW, the AD7225 interface behaves like the AD7226.

Since $\overline{LDAC}$ (AD7225 only) is asynchronous with respect to $\overline{WR}$, care must be taken to assure that incorrect data is not latched through to the output. If $\overline{LDAC}$ is brought LOW before or at the same time that $\overline{WR}$ goes HIGH, then $\overline{LDAC}$ must remain LOW for at least t_{LD} to ensure that the correct data is latched. Data is latched into all four DAC registers on the

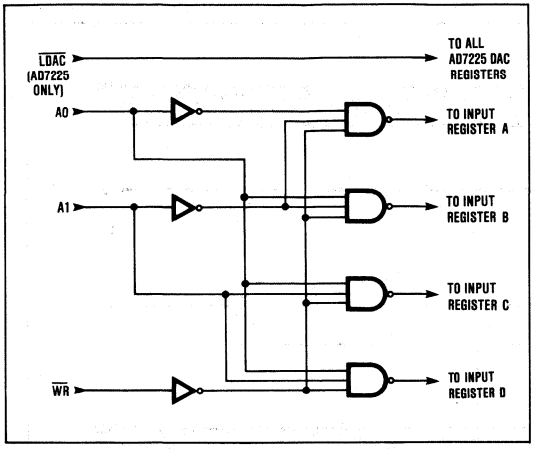


Figure 5. AD7225, AD7226 Input Control Logic

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table 2. AD7225, AD7226 Write Cycle Truth Table

$\overline{WR}$	$\overline{LDAC}$ (AD7225 ONLY)	FUNCTION
H	H	No operation. Device deselected.
L	H	Input register of selected DAC transparent.
⌐¬	H	Latch the input register of selected DAC.
H	L	(AD7225 only) All four DAC registers transparent i.e. DAC outputs reflect the data held in their respective input registers. Input registers are latched.
H	⌐¬	(AD7225 only) Latch the four DAC registers. Input registers are latched.
L	L	(AD7225 only) DAC Registers and the selected input register transparent. DAC output follows input data for selected channel.

rising edge of $\overline{LDAC}$. Table 2 shows the truth table for $\overline{WR}$ and $\overline{LDAC}$ operation. Figure 6 shows the write cycle timing for both the AD7225 and AD7226.

Applications Information

Power Supply and Reference Operating Ranges

The AD7225 and AD7226 are fully specified to operate with V_{DD} between +12V ± 5% and +15V ± 10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. 8 bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. Both the AD7225 and AD7226 are specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (IN914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 and 8 show suggested circuit board layouts for minimizing crosstalk.

Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configurations are shown in Figure 9 and 10 for the AD7225 and AD7226. Both devices can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to DGND. The unipolar code table is given in Table 3.

Bipolar Output

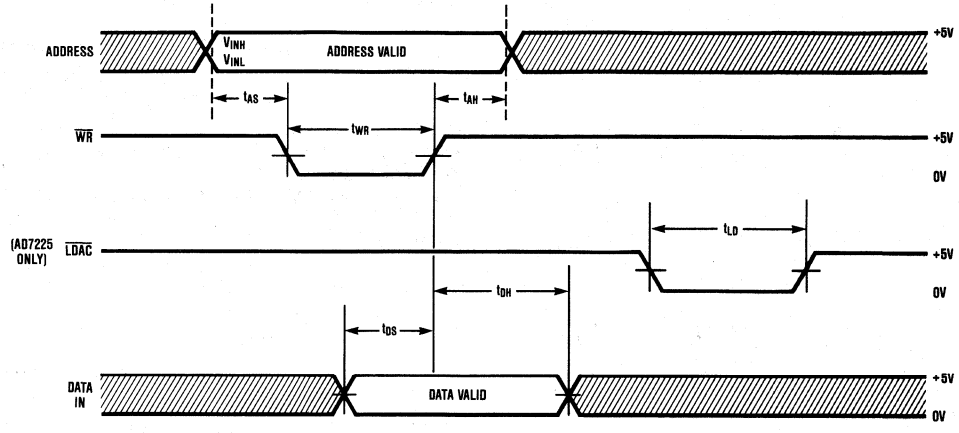
Each DAC output may be configured for bipolar operation using the circuit in Figure 11. One op-amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF}(2D_A - 1),$$

where D_A is a fractional representation of the digital word in register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 11.

CMOS Quad 8-Bit D/A Converters



Notes:
1. All input signal rise and fall times measured from 10% to 90% of +5V $t_r = t_f = 20ns$ over V_{DD} range.
2. Timing measurement reference level is,
$$\frac{V_{INH} + V_{INL}}{2}$$
3. If $\overline{LDAC}$ (AD7225 only) is activated prior to the rising edge of $\overline{WR}$, then it must stay low for t_{LD} (or longer) after $\overline{WR}$ goes high.

Figure 6. Write Cycle Timing Diagram

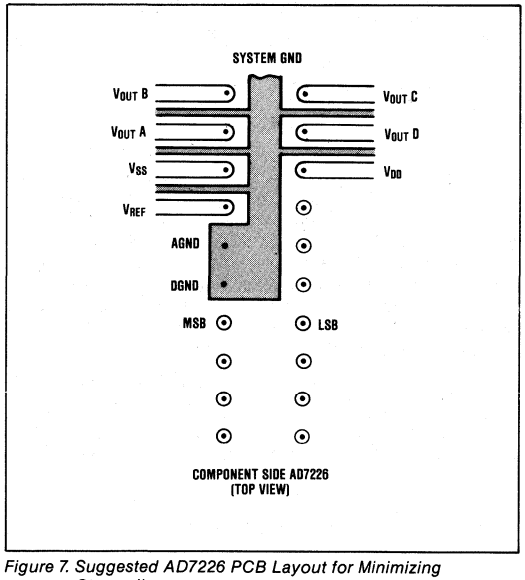


Figure 7. Suggested AD7226 PCB Layout for Minimizing Crosstalk

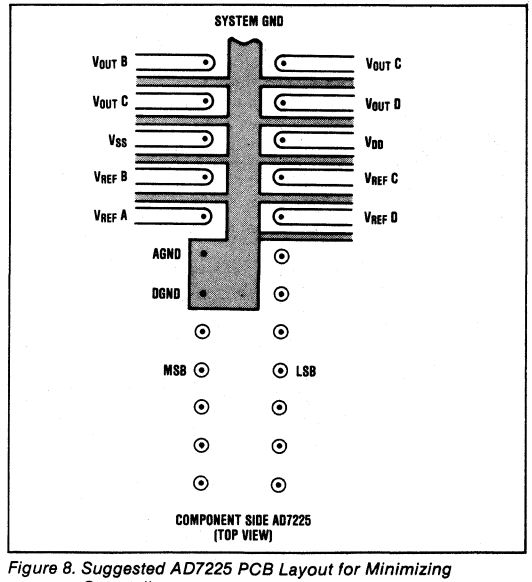


Figure 8. Suggested AD7225 PCB Layout for Minimizing Crosstalk

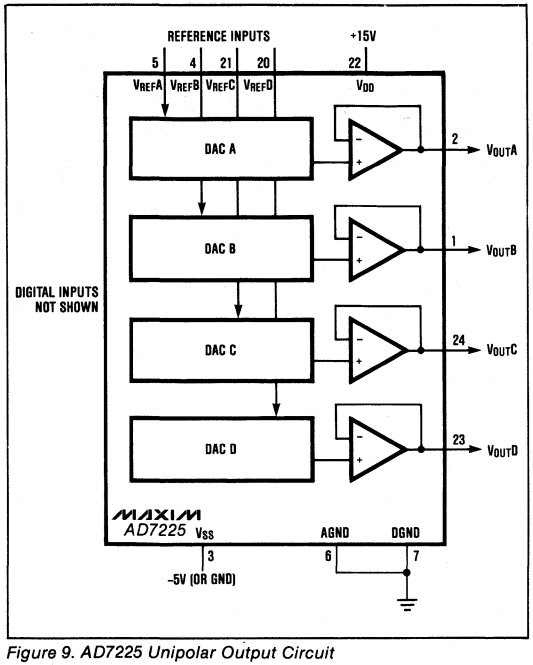


Figure 9. AD7225 Unipolar Output Circuit

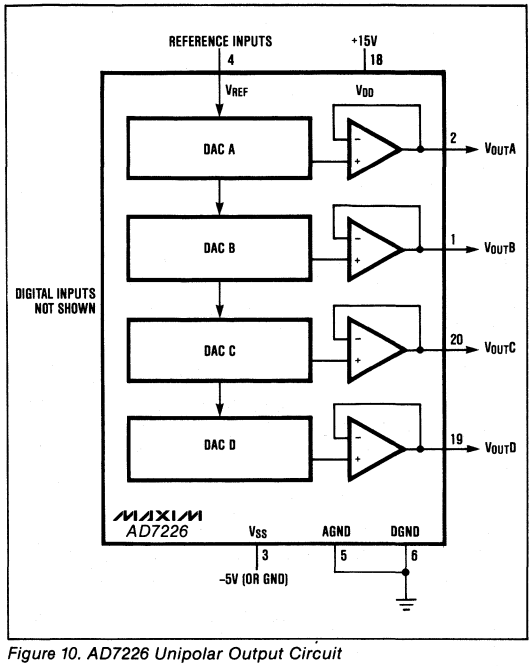


Figure 10. AD7226 Unipolar Output Circuit

Table 3. Unipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

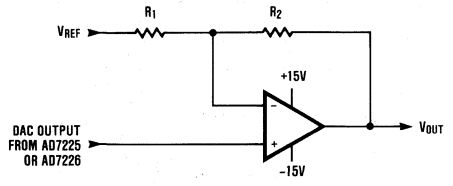
Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Table 4. Bipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

2

CMOS Quad 8-Bit D/A Converters



Note: V_{REF} is the Reference Input for the AD7226, or is the selected Reference Input for the AD7225.

Figure 11. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 12. The output voltage at $V_{OUT}A$ is:

$$V_{OUT}A = V_{BIAS} + D_A V_{IN},$$

where D_A is a fractional representation of the digital input word. Since AGND is common to all four DAC's, all outputs will be offset by V_{BIAS} in the same manner.

Using an AC Reference

In applications where V_{REF} has AC signal components, the AD7225 and AD7226 have multiplying capability within the limits of the V_{REF} input range specifications. Figure 13 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

Generating V_{SS}

The performance of the AD7225/7226 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of figure 14.

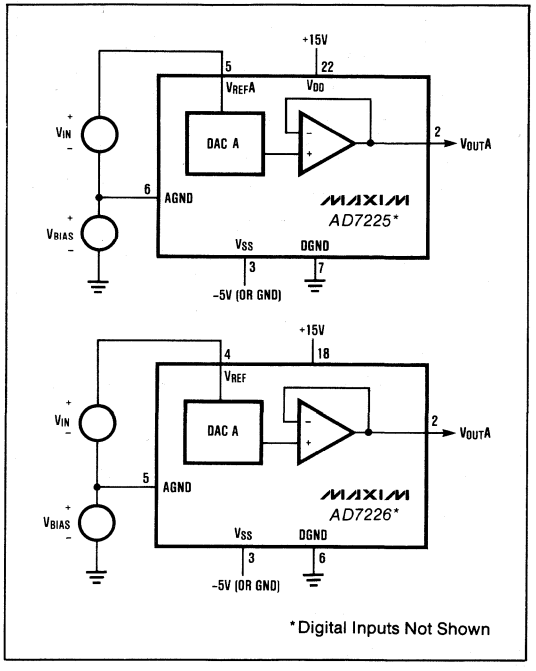


Figure 12. AGND Bias Circuits

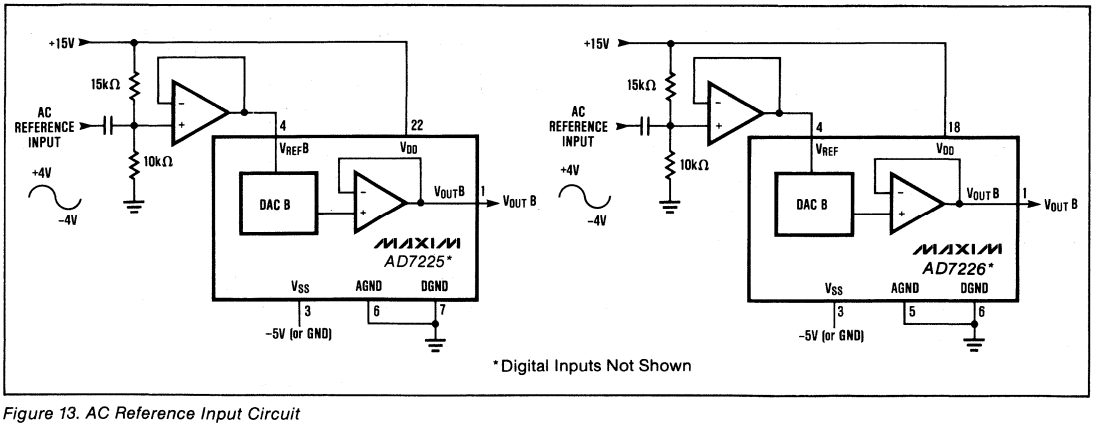


Figure 13. AC Reference Input Circuit

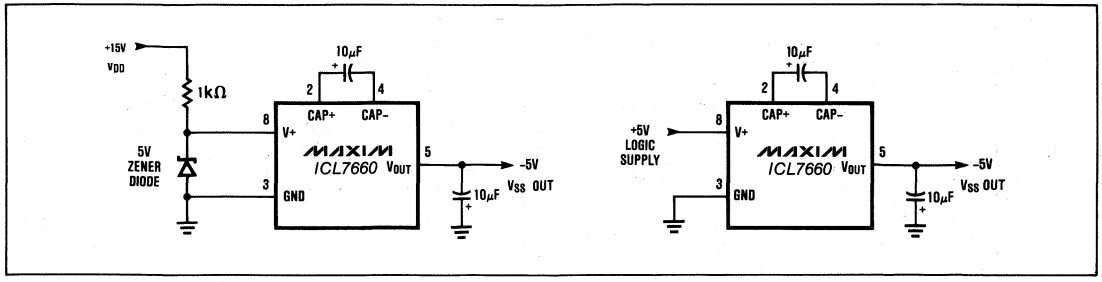


Figure 14. Generating -5V for V_{SS}

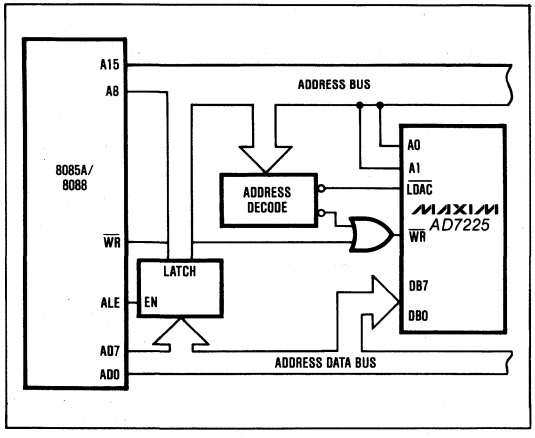


Figure 15. AD7225 to 8085A/8088 Interface, Double-Buffered Mode

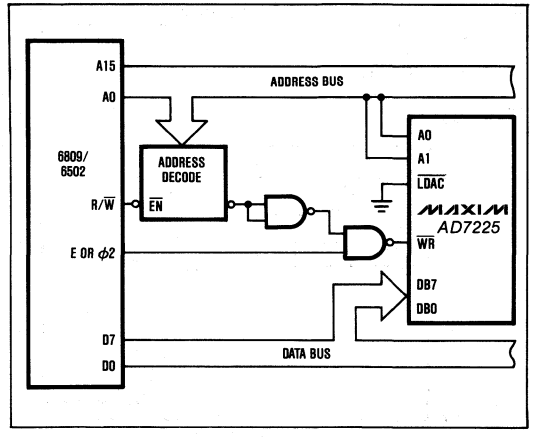


Figure 16. AD7225 to 6089/6502 Interface, Single-Buffered Mode

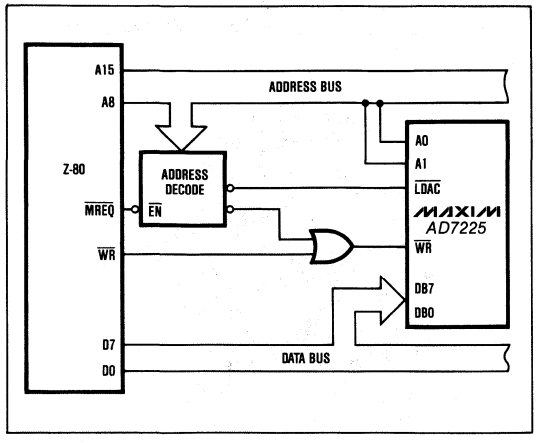


Figure 17. AD7225 to Z-80 Interface Double-Buffered Mode

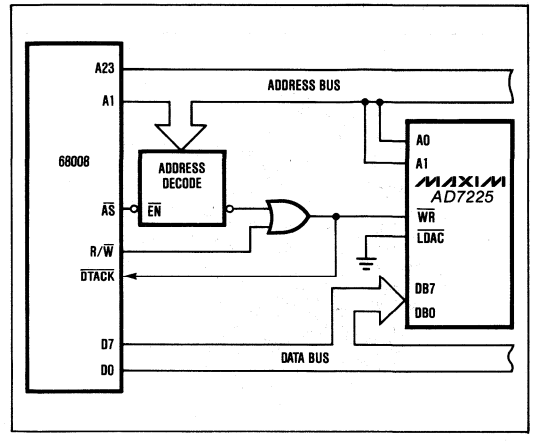


Figure 18. AD7225 to 68008 Interface, Single-Buffered Mode

CMOS Quad 8-Bit D/A Converters

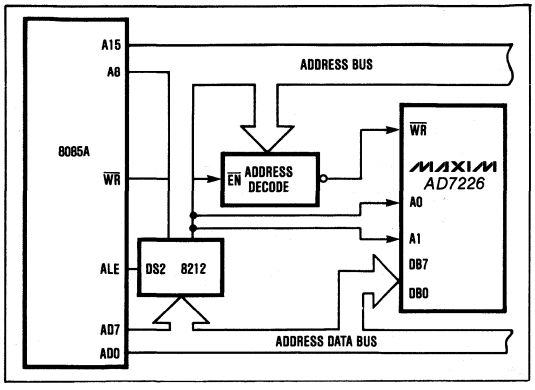


Figure 19. AD7226 to 8085A Interface

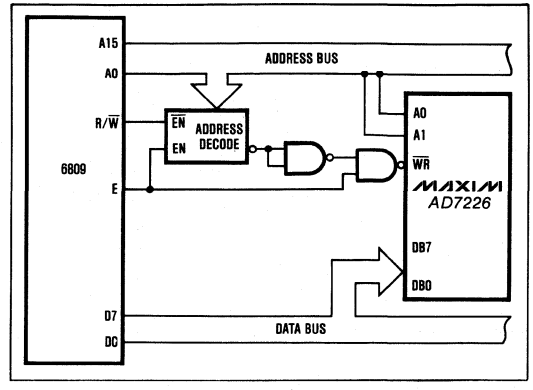


Figure 20. AD7226 to 6809 Interface

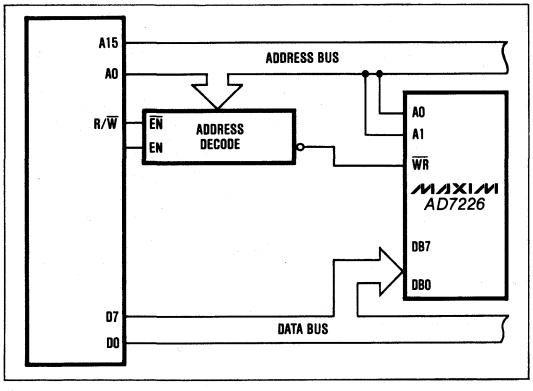


Figure 21. AD7226 to 6502 Interface

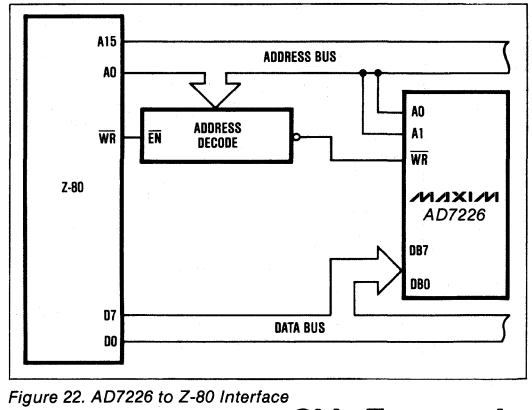
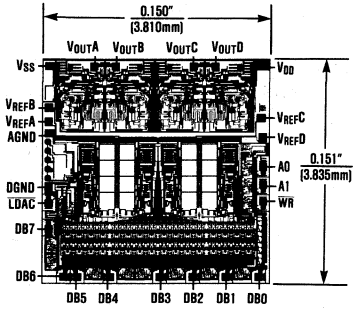
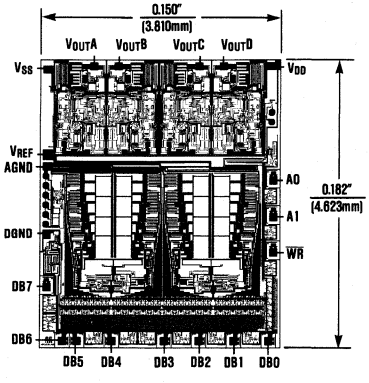


Figure 22. AD7226 to Z-80 Interface

Chip Topography



AD7225



AD7226

MAXIM

CMOS 10 and 12 Bit Multiplying D/A Converters

General Description

The AD7520 and AD7521 are low cost CMOS multiplying digital-to-analog converters (DACs) with 10 and 12 bit resolution respectively. Both DACs operate from a +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C gain temperature coefficient. All digital inputs are compatible with both CMOS and TTL logic levels.

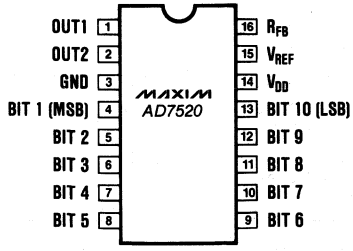
Maxim's AD7520 and AD7521 are electrically and pin compatible with Analog Devices' AD7520 and AD7521. The AD7520 is packaged in a 16-lead DIP while the AD7521 is packaged in an 18-lead DIP. Both devices are also available in small outline (SO) packages.

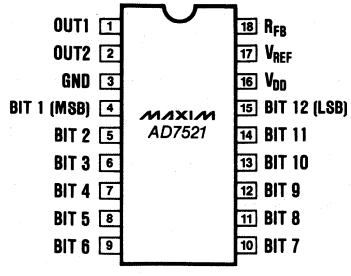
Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Pin Configuration

Top View





Features

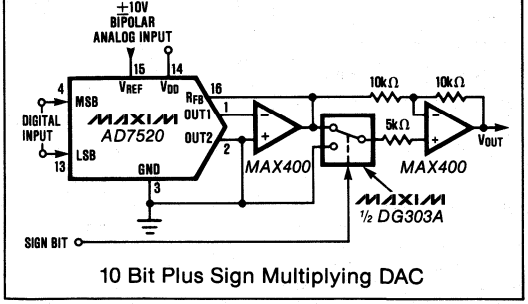
- 10 or 12 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption — 20mW
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7520JN	0°C to +70°C	Plastic DIP	0.2%
AD7520KN	0°C to +70°C	Plastic DIP	0.1%
AD7520LN	0°C to +70°C	Plastic DIP	0.05%
AD7520JCWE	0°C to +70°C	Small Outline	0.2%
AD7520KCWE	0°C to +70°C	Small Outline	0.1%
AD7520LCWE	0°C to +70°C	Small Outline	0.05%
AD7520JC/D	0°C to +70°C	Dice	0.2%
AD7520JQ	-25°C to +85°C	CERDIP**	0.2%
AD7520KQ	-25°C to +85°C	CERDIP**	0.1%
AD7520LQ	-25°C to +85°C	CERDIP**	0.05%
AD7520JD	-25°C to +85°C	Ceramic	0.2%
AD7520KD	-25°C to +85°C	Ceramic	0.1%
AD7520LD	-25°C to +85°C	Ceramic	0.05%
AD7520SQ	-55°C to +125°C	CERDIP**	0.2%
AD7520TQ	-55°C to +125°C	CERDIP**	0.1%
AD7520UQ	-55°C to +125°C	CERDIP**	0.05%
AD7520SD	-55°C to +125°C	Ceramic	0.2%
AD7520TD	-55°C to +125°C	Ceramic	0.1%
AD7520UD	-55°C to +125°C	Ceramic	0.05%

** AD7520 — 16 lead package, AD7521 — 18 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering Information continued on last page.

Typical Operating Circuit



10 Bit Plus Sign Multiplying DAC

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
Commercial (JN/KN/LN/JC/KC/LC) ..... 0°C to +70°C
Industrial (JD/KD/LD/JQ/KQ/LQ) ..... -25°C to +85°C
Military (S/T/U) ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_{DD} =+ 15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

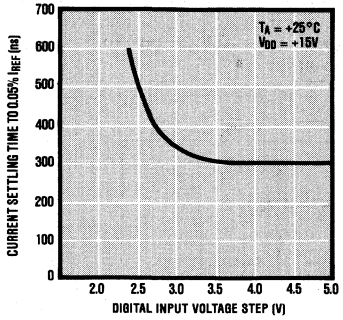
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)						
Resolution		AD7520 AD7521	10 12			Bits
Relative Accuracy (Note 3)		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX} 0.2% FSR = 8 Bits J/S 0.1% FSR = 9 Bits K/T 0.05% FSR = 10 Bits L/U			±0.2 ±0.1 ±0.05	% FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4)			2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V (Note 5)		0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4,5)			10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}		200		nA
Power Supply Rejection	PSRR	(Note 3)		50		ppm/ %V_{DD}
V_{REF} Input Resistance	R_{REF}	R_{REF} tempco = -150ppm/°C typ.	5	10	20	kΩ
AC ACCURACY						
Output Current Settling Time (Note 3)		To 0.05% of FSR, all digital inputs high to low and low to high.		500		ns
Feedthrough Error (Note 3,4,6)		All digital inputs low, V_{REF} = 20V_{P-P}, 100kHz sinewave.		10		mV_{P-P}
ANALOG OUTPUTS						
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high, OUT1 All digital inputs high, OUT2 All digital inputs low, OUT1 All digital inputs low, OUT2		120 37 37 120		pF
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance			10	kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})						
Low State Threshold	V_{INL}				0.8	V
High State Threshold	V_{INH}		2.4			V
Input Current		Low to high state		±1		µA
Input Coding		Unipolar (Table 1), Bipolar (Table 2)	Binary, Offset Binary			
POWER REQUIREMENTS						
Power Supply Range	V_{DD}		+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND Digital inputs high or low		5	 2	nA mA
Total Power Dissipation		Including V_{REF}		20		mW

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: See Test Circuits.
Note 4: Guaranteed by design but not 100% tested.
Note 5: Using internal feedback resistor, R_{FB}.
Note 6: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

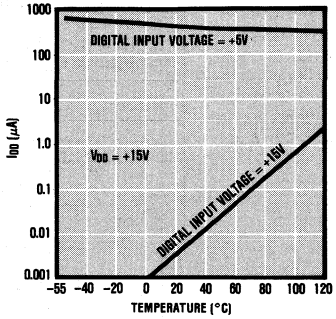
CMOS 10 and 12 Bit Multiplying D/A Converters

Typical Operating Characteristics

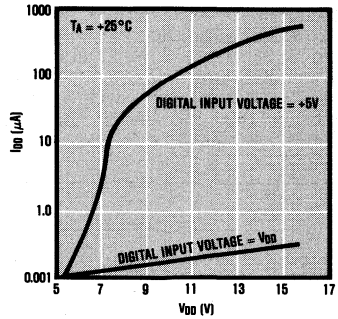
OUTPUT CURRENT SETTLING TIME vs. DIGITAL INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

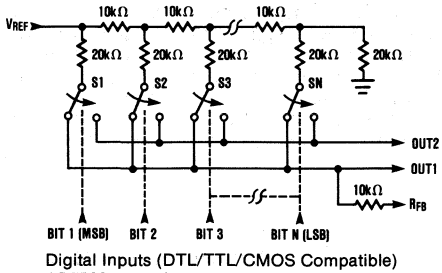


SUPPLY CURRENT vs. SUPPLY VOLTAGE



Detailed Description

The basic AD7520/21 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.



Digital Inputs (DTL/TTL/CMOS Compatible)
AD7520: N = 10
AD7521: N = 12
(Switches shown for inputs HIGH)

Figure 1. AD7520/AD7521 Functional Diagram

Application Information

Unipolar Operation

The most common configuration for the AD7520/21 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 50pF.

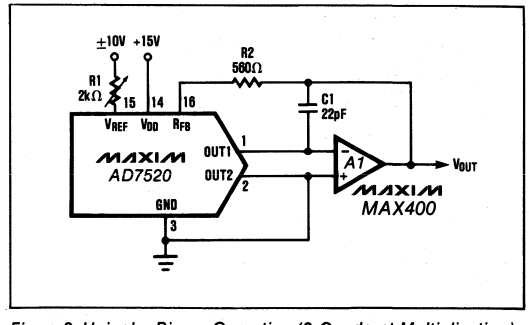


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Table 1: Code Table (AD7520) — Unipolar Binary Operation

DIGITAL INPUT										ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	$-V_{REF}\ (1 - 2^{-10})$
1	0	0	0	0	0	0	0	0	1	$-V_{REF}\ (½ + 2^{-10})$
1	0	0	0	0	0	0	0	0	0	$-V_{REF}/2$
0	1	1	1	1	1	1	1	1	1	$-V_{REF}\ (½ - 2^{-10})$
0	0	0	0	0	0	0	0	0	1	$-V_{REF}\ (2^{-10})$
0	0	0	0	0	0	0	0	0	0	0

Note: 1 LSB = 2^{-10} V_{REF} (AD7520)

CMOS 10 and 12 Bit Multiplying D/A Converters

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7520 and 250nA for the AD7521.

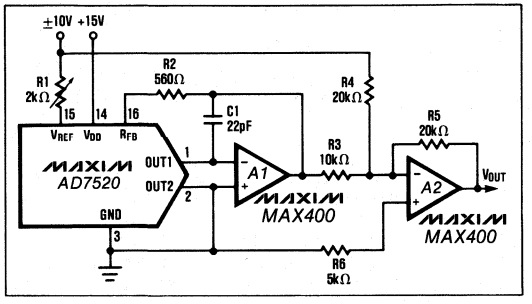


Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2: Code Table (AD7520) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = 2^{-9} V_{REF} (AD7520)

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The AD7520 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.

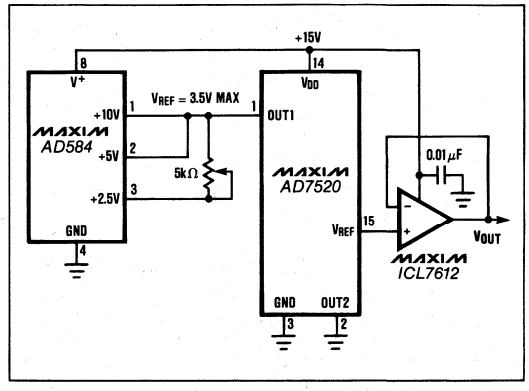


Figure 4. Single Supply Voltage Mode Operation

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

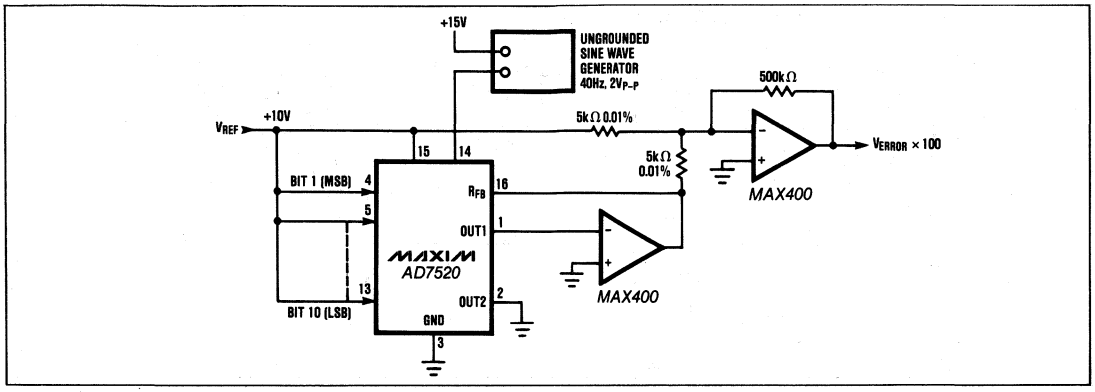


Figure 5. Power Supply Rejection

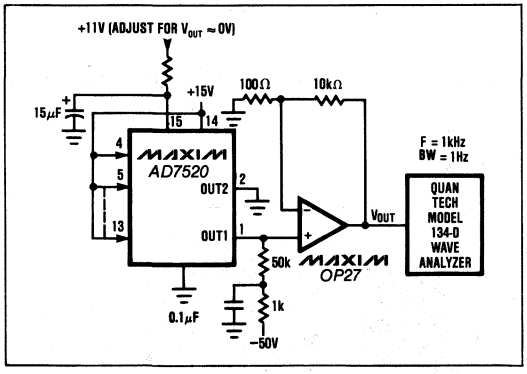


Figure 6. Noise

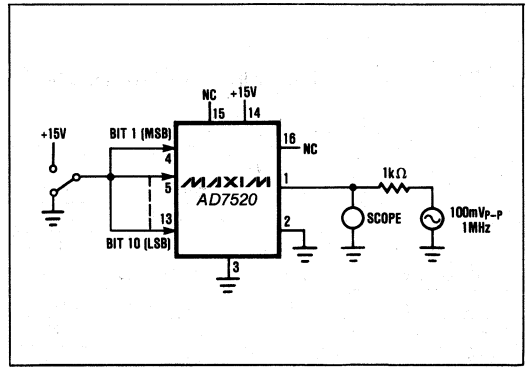


Figure 7. Output Capacitance

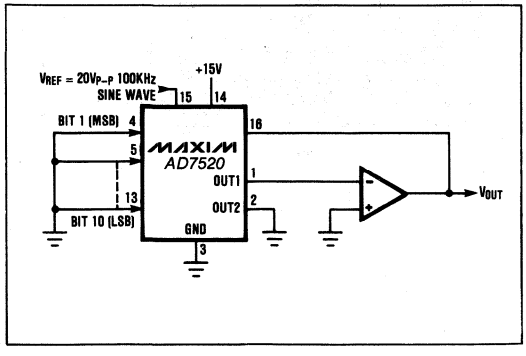


Figure 8. Feedthrough Error

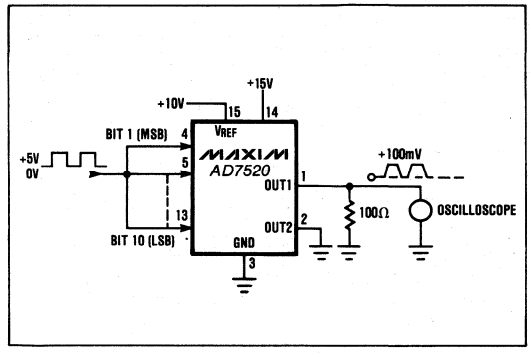


Figure 9. Output Current Settling Time

CMOS 10 and 12 Bit Multiplying D/A Converters

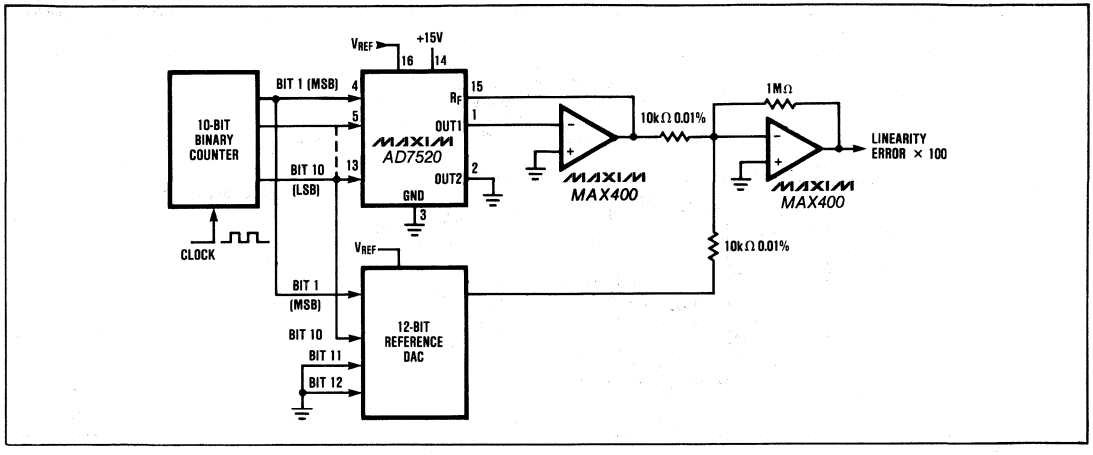


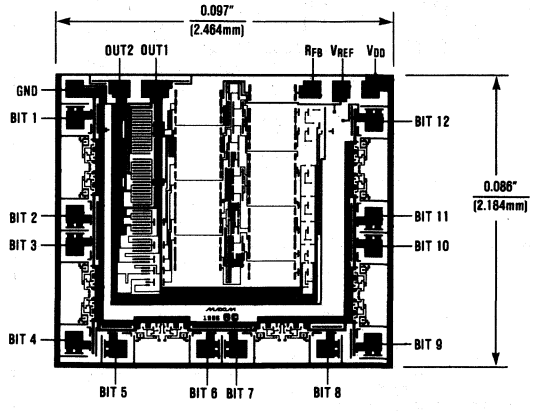
Figure 10. Relative Accuracy

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7521JN	0°C to +70°C	Plastic DIP	0.2%
AD7521KN	0°C to +70°C	Plastic DIP	0.1%
AD7521LN	0°C to +70°C	Plastic DIP	0.05%
AD7521JCWN	0°C to +70°C	Small Outline	0.2%
AD7521KCWN	0°C to +70°C	Small Outline	0.1%
AD7521LCWN	0°C to +70°C	Small Outline	0.05%
AD7521JC/D	0°C to +70°C	Dice	0.2%
AD7521JQ	-25°C to +85°C	CERDIP**	0.2%
AD7521KQ	-25°C to +85°C	CERDIP**	0.1%
AD7521LQ	-25°C to +85°C	CERDIP**	0.05%
AD7521JD	-25°C to +85°C	Ceramic	0.2%
AD7521KD	-25°C to +85°C	Ceramic	0.1%
AD7521LD	-25°C to +85°C	Ceramic	0.05%
AD7521SQ	-55°C to +125°C	CERDIP**	0.2%
AD7521TQ	-55°C to +125°C	CERDIP**	0.1%
AD7521UQ	-55°C to +125°C	CERDIP**	0.05%
AD7521SD	-55°C to +125°C	Ceramic	0.2%
AD7521TD	-55°C to +125°C	Ceramic	0.1%
AD7521UD	-55°C to +125°C	Ceramic	0.05%

** AD7520 — 16 lead package, AD7521 — 18 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography



MAXIM

CMOS 8 Bit Multiplying D/A Converter

General Description

The AD7523 is high performance multiplying 8 bit digital-to-analog converter (DAC). Low power CMOS technology and low cost make it suitable for a wide range of analog data acquisition and control applications.

Thin-film resistors assure 8 bit resolution with up to 10 bit linearity (L grade) over the full operating temperature range. In addition, all digital inputs are compatible with CMOS logic levels.

Maxim's AD7523 is electrically and pin compatible with the Analog Devices AD7523 and is available in a standard width 16-lead DIP as well as small outline package.

Features

- **8, 9 and 10 Bit Linearity**
- **±1.5% Untrimmed Gain Accuracy**
- **Guaranteed Monotonic**
- **Low Feedthrough 1/2LSB at 200kHz**
- **Low Power Consumption**
- **CMOS Compatible Logic Inputs**
- **Widely Second Sourced**

Applications

Automatic Test Equipment
Digital Calibration Systems
Battery Powered Instruments
Audio Gain Control
Digitally Controlled Filters
Programmable Power Supplies
Motion Control Systems

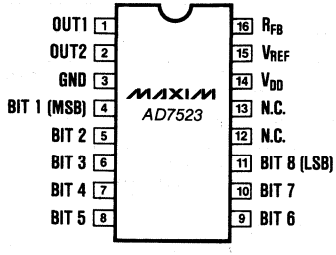
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7523JN	0°C to +70°C	Plastic DIP	½LSB
AD7523KN	0°C to +70°C	Plastic DIP	¼LSB
AD7523LN	0°C to +70°C	Plastic DIP	⅛LSB
AD7523JCWE	0°C to +70°C	Small Outline	½LSB
AD7523KCWE	0°C to +70°C	Small Outline	¼LSB
AD7523LCWE	0°C to +70°C	Small Outline	⅛LSB

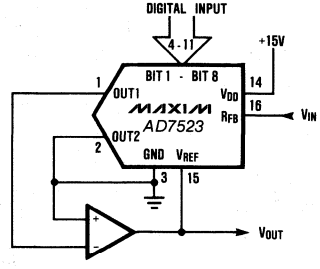
** All devices — 16 lead packages*

Pin Configuration

Top View



Typical Operating Circuit



$$V_{OUT} = \frac{256}{D}$$

D = Digital Input Code

Digitally Controlled Gain

CMOS 8 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C
Power Dissipation to +70°C
Plastic DIP 670mW
Small Outline 450mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				8			Bits
Nonlinearity (Note 2)		0.2% FSR = ½LSB 0.1% FSR = ¼LSB 0.05% FSR = ⅛LSB	J K L			±½ ±¼ ±⅛	LSB
Monotonicity					Guaranteed		
Gain Error (Note 2, 3)		Digital Inputs = V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			±1.5 ±1.8	% FSR
Power Supply Rejection (Note 2)	PSRR	V_{DD} = +14V to +15V	T_A = +25°C T_{MIN} to T_{MAX}			0.02 0.03	%/%V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL}	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
		OUT2, Digital Inputs = V_{INH}	T_A = 25°C T_{MIN} to T_{MAX}			±50 ±200	
V_{REF} Input Resistance	R_{REF}	T_A = +25°C		5	10	20	kΩ
V_{REF} Resistance Tempco		(Note 4)				-500	ppm/°C
AC PERFORMANCE (Note 4)							
Output Current Settling Time to 0.2% of FSR		R_L = 100Ω, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			150 200	ns
Feedthrough Error		Digital Inputs = V_{INL}, V_{REF} = 20V_{P-P}, 200 KHz	T_A = +25°C T_{MIN} to T_{MAX}			±½ ±1	LSB
Output Capacitance	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 30	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			30 100	
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+14.5			V
Logic LOW Threshold	V_{INL}					+0.5	V
Input Leakage Current		Digital inputs = 0V or +15V				±1	μA
Input Capacitance, (Note 4)						4	pF
Input Coding		Unipolar Operation (Table 1) Bipolar Operation (Table 2)		Binary Offset Binary			
POWER REQUIREMENTS							
Power Supply Range	V_{DD}	Accuracy not guaranteed over this range.		+5		+16	V
Power Supply Current	I_{DD}	Digital inputs = V_{INH} or V_{INL}				100	μA

Note 1: $V_{OUT1, 2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.
Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = -(V_{REF} - 1LSB) in unipolar mode.
Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±0.3% FSR.
Note 4: Guaranteed by design but not 100% tested.

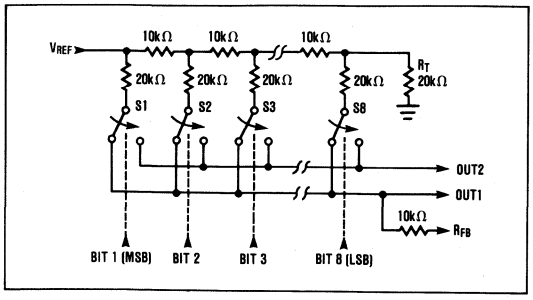
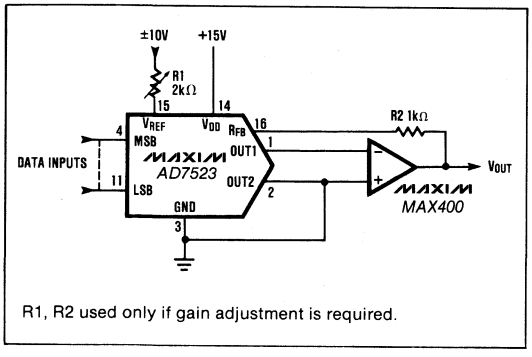
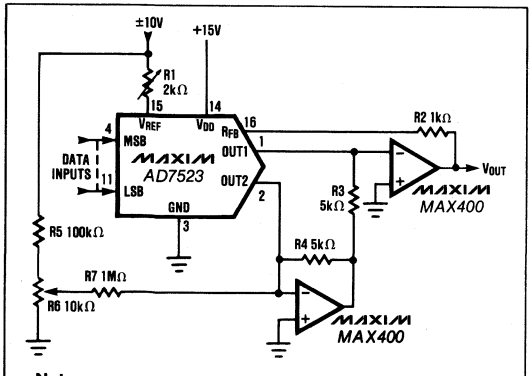


Figure 1. AD7523 Functional Diagram



R1, R2 used only if gain adjustment is required.

Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)



Notes:
1. R3/R4 match 0.1% or better.
2. R1, R2 used only if gain adjustment is required.
3. R5–R7 used to adjust V_{OUT} = 0V at input code 10000000.

Figure 3. Bipolar (4-Quadrant) Operation

Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{225}{256}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

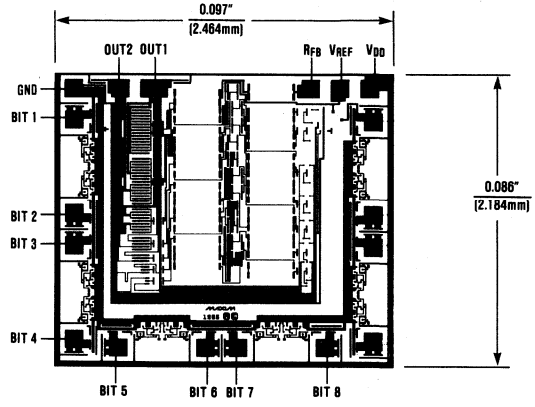
Note: $1LSB = (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Chip Topography



CMOS 8-Bit Buffered Multiplying DACs

General Description

The AD7524 and MAX7624 are CMOS 8-bit digital-to-analog converters (DAC) which will interface directly with most microprocessors. On-chip input latches make the DAC interface similar to a RAM write cycle where CS and WR are the only control inputs required.

Linearity up to ±⅛ LSB is available (AD7524L/C/U grades) and power consumption is less than 10mW. Monotonicity is guaranteed over the full temperature range.

For the AD7524, +5V TTL and CMOS logic compatibility is guaranteed when using +5V power. Over the supply range of +5V to +15V, all logic inputs are high voltage CMOS compatible.

The MAX7624 has +5V TTL/CMOS compatible inputs for a +12V to +15V supply range.

Applications

μP Controlled Gain

Function Generators

Bus Structured Instruments

Automatic Test Equipment

Digital Control Systems

Features

- **Microprocessor Compatible**
- **On-Chip Data Latches**
- **Guaranteed Monotonic Over Temp.**
- **Low Power Consumption**
- **8, 9, and 10-Bit Linearity**
- **AD7524 TTL/CMOS Compatible at +5V**
- **MAX7624 TTL/CMOS Compatible at +12V to +15V**

Ordering Information

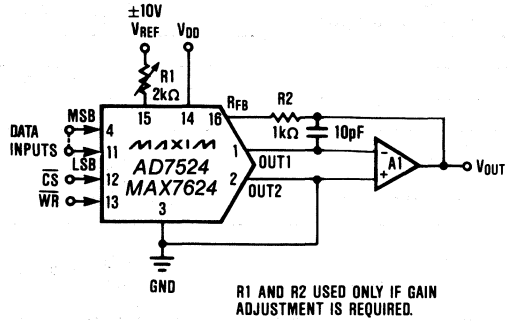
PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524JN	0°C to +70°C	Plastic DIP	±½ LSB
AD7524KN	0°C to +70°C	Plastic DIP	±¼ LSB
AD7524LN	0°C to +70°C	Plastic DIP	±⅛ LSB
AD7524JCSE	0°C to +70°C	Small Outline	±½ LSB
AD7524KCSE	0°C to +70°C	Small Outline	±¼ LSB
AD7524LCSE	0°C to +70°C	Small Outline	±⅛ LSB
AD7524JC/D	0°C to +70°C	Dice	±½ LSB
AD7524AD	-25°C to +85°C	Ceramic	±½ LSB
AD7524BD	-25°C to +85°C	Ceramic	±¼ LSB
AD7524CD	-25°C to +85°C	Ceramic	±⅛ LSB

* *All devices — 16 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

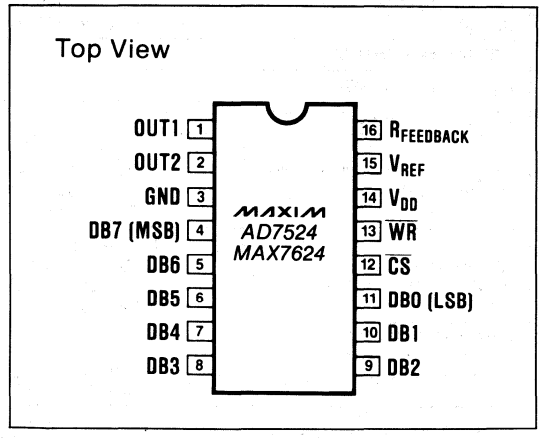
(Ordering Information continued on last page)

Typical Operating Circuit



Unipolar Binary Operation
(2-Quadrant Multiplication)

Pin Configuration



CMOS 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7524, MAX7624

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V to V_{DD} + 0.3V
OUT1, OUT2 to GND ..... -0.3V, V_{DD}
Operating Temperature Ranges
AD7524JN, KN, LN, JCSE, KCSE, LCSE
MAX7624CPE, CSE ..... 0°C to +70°C
Operating Temperature Ranges (continued)
AD7524AD, AQ, BD, BQ, CD, CQ .... -25°C to +85°C
MAX7624EPE ..... -40°C to +85°C
AD7524SD, SQ, TD, TQ, UD, UQ
MAX7624MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1/2 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2½ ±3½	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±40	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.002 0.01	0.08 0.16	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V DAC is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V DAC is 11111111	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} (pin 15 to GND)				5	10	20	kΩ
DYNAMIC PERFORMANCE							
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUT1 Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			400 500	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave DB0-DB7 = $\overline{WR}$ = $\overline{CS}$ = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			0.25 0.5	%FSR
ANALOG OUTPUTS							
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V				30 120	pF

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS—AD7524, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7 WR, CS			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U		170 220 240		ns
Chip Select to Write Hold Time	t_{CH}			0		ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U		170 220 240		ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U		135 170 170		ns
Data Hold Time	t_{DH}			10		ns

ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U			±1/2 ±1/4 ±1/8	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)		T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1¼ ±1½	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	ΔV_{DD} = ±10% T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V T_A = 25°C DAC is 00000000 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V T_A = 25°C DAC is 11111111 T_A = T_{MIN} to T_{MAX}			±50 ±200	nA

CMOS 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—AD7524, +15V Operation (Continued)

(V_{DD} = +15V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V T_A = 25°C OUT1 Load = 100Ω, T_A = T_{MIN} to T_{MAX} C_{EXT} = 13pF;			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V 100kHz Sinewave T_A = 25°C DB0-DB7 = $\overline{WR}$ = T_A = T_{MIN} to T_{MAX} $\overline{CS}$ = 0V			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			120 30	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = V_{DD}; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			30 120	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A= 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$			8 20	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Chip Select to Write Hold Time	t_{CH}		0			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	100 130 150			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} J,K,L,A,B,C T_A = T_{MIN} to T_{MAX} S,T,U	60 80 100			ns
Data Hold Time	t_{DH}		10			ns

Note 1: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 2: Guaranteed, but not tested.
Note 3: Gain error measured from 25°C to T_{MAX} or from 25°C to T_{MIN}.
Note 4: Sample tested at 25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy	INL				±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.			±1	LSB
Gain Error (Note 1)					±2	LSB
Gain Temp. Coefficient (Note 2, 3)				±1	±10	ppm/°C
Supply Rejection (Note 2)	PSR	V_{DD} = +10.8V to +15.75V; T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.005	0.02 0.04	%FSR/%
Output Leakage Current (I_{OUT1})		V_{REF} = ±10V, DAC is 00000000; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (I_{OUT2})		V_{REF} = ±10V, DAC is 11111111; T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT						
R_{IN} (pin 15 to GND)			5	10	20	kΩ
DYNAMIC PERFORMANCE						
Output Current Settling-Time to 1/2 LSB (Note 2)		DB0-DB7 = 0V to +5V to 0V; $\overline{WR}$ = $\overline{CS}$ = 0V; OUT1 Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			250 350	ns
AC Feedthrough (OUT1 or OUT2) (Note 2)		V_{REF} = ±10V, 100kHz Sinewave, DB0-DB7 = $\overline{WR}$ = $\overline{CS}$ = 0V; T_A = 25°C T_A = T_{MIN} to T_{MAX}			0.25 0.5	%FSR
ANALOG OUTPUTS						
OUT1 Capacitance (Note 2)	C_{OUT1}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			60 25	pF
OUT2 Capacitance (Note 2)	C_{OUT2}	DB0-DB7 = +5V; $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB7 = 0V; $\overline{WR}$ = $\overline{CS}$ = 0V			25 60	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C; V_{IN} = 0V or V_{DD} T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB7, $\overline{WR}$, $\overline{CS}$			8	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}			2.5	mA
		Digital inputs 0V or V_{DD}; T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA

CMOS 8-Bit Buffered Multiplying DACs

ELECTRICAL CHARACTERISTICS—MAX7624, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Chip Select to Write Hold Time	t_{CH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	150 170 210			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX} C,E T_A = T_{MIN} to T_{MAX} M	160 160 210			ns
Data Hold Time	t_{DH}		10			ns

Detailed Description

The AD7524/MAX7624 is an 8-bit multiplying digital-to-analog converter (DAC) that consists of a thin-film R-2R resistor array with CMOS current steering switches. In applications requiring a voltage output, an output operational amplifier and reference will be needed. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at either OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The two OUT terminals must be held at the same potential so a constant current is maintained in each ladder leg. This makes the V_{REF} input current independent of switch state and also ensures that the AD7524/MAX7624 maintains its excellent linearity performance.

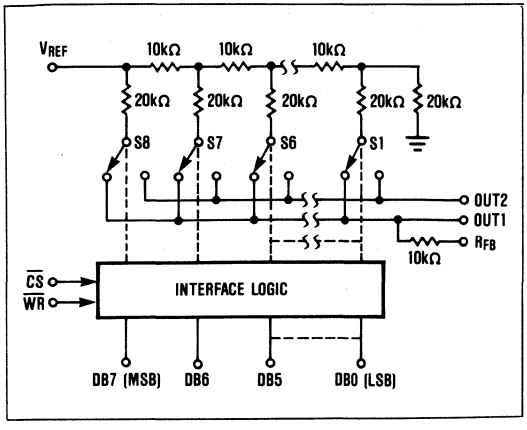


Figure 1. AD7524/MAX7624 Functional Diagram

Equivalent-Circuit Analysis

The equivalent circuit for all digital inputs LOW is shown in figure 2. In this state the reference current is switched to OUT2. The current source, $I_{LEAKAGE}$, is composed of small surface and junction leakages to the substrate which double every 10°C. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. The value of output capacitance at the OUT1 and OUT2 terminals is input code dependent and lies in the range 20pF to 30pF.

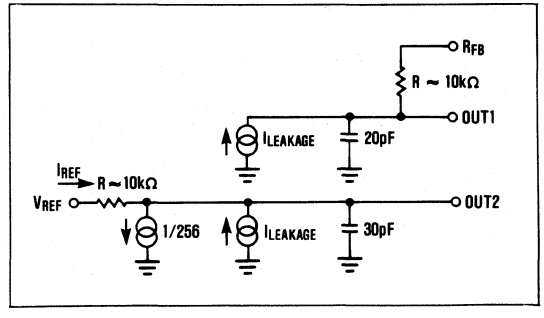


Figure 2. AD7524/MAX7624 DAC Equivalent Circuit—All Digital Inputs LOW

The AD7524's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region 1.5 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The AD7524 may be operated with any supply voltage in the range 5V < V_{DD} < 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The MAX7624's digital inputs are TTL/CMOS compatible for a +12V to +15V supply range. However, when V_{IN} is in the range of 1.5V to V_{DD} - 1.5V the input buffers operate in their linear region and the quiescent current increases (see figure 3).

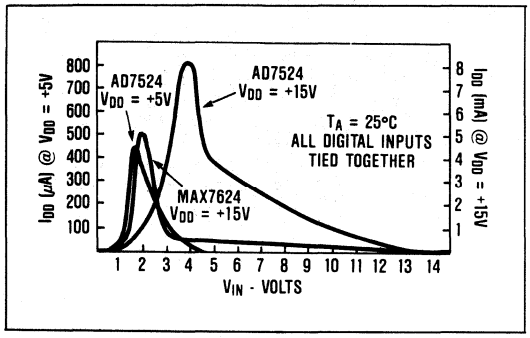


Figure 3. Typical Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V

Interface Logic Information

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the AD7524/MAX7624. See Mode Selection Table.

Mode Selection Table

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0-DB7) inputs
H X	X H	HOLD HOLD	Data bus (DB0-DB7) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed HIGH state

L = Low State, H = High State, X = Don't Care

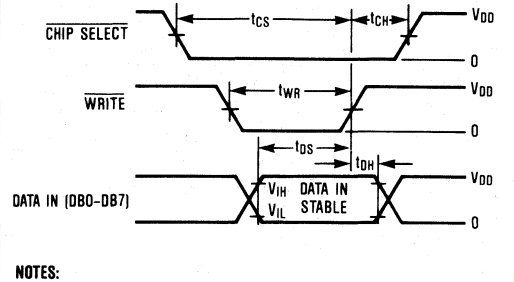
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524/MAX7624 is in the write mode, and the AD7524/MAX7624 analog output responds to data activity at the DB0-DB7 data bus inputs. In this mode, the data latches are transparent.

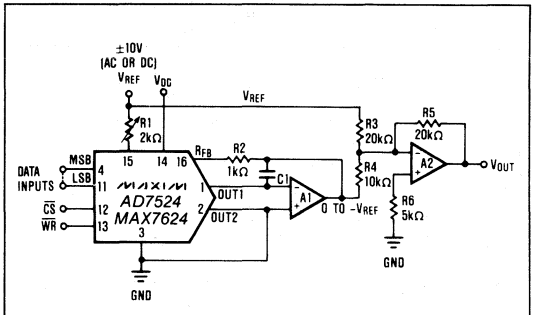
Hold Mode

The AD7524/MAX7624 retains the data that was present on DB0-DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. The analog output remains at the value corresponding to the digital code locked in the data latch.

Write Cycle Timing Diagram



NOTES:
1. FOR THE AD7524 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, t_r = t_f = 20ns; V_{DD} = +15V, t_r = t_f = 40ns.
2. FOR THE MAX7624 ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM 10% TO 90% OF +5V.
3. TIMING MEASUREMENT REFERENCE LEVEL IS (V_{IH} + V_{IL})/2.



NOTES:
1. ADJUST R1 FOR V_{OUT} = 0V AT CODE 10000000.
2. C1 PHASE COMPENSATION (10-15pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER

Figure 4. Bipolar (4-Quadrant) Operation

CMOS 8-Bit Buffered Multiplying DACs

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7524AQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7524BQ	-25°C to +85°C	CERDIP**	±¼ LSB
AD7524CQ	-25°C to +85°C	CERDIP**	±⅛ LSB
AD7524SD	-55°C to +125°C	Ceramic	±½ LSB
AD7524TD	-55°C to +125°C	Ceramic	±¼ LSB
AD7524UD	-55°C to +125°C	Ceramic	±⅛ LSB
AD7524SQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7524TQ	-55°C to +125°C	CERDIP**	±¼ LSB
AD7524UQ	-55°C to +125°C	CERDIP**	±⅛ LSB
MAX7624CPE	0°C to +70°C	Plastic DIP	±½ LSB
MAX7624CSE	0°C to +70°C	Small Outline	±½ LSB
MAX7624C/D	0°C to +70°C	Dice	±½ LSB
MAX7624EPE	-40°C to +85°C	Plastic DIP	±½ LSB
MAX7624MJE	-55°C to +125°C	CERDIP	±½ LSB

* *All devices—16 lead packages*

** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Chip Topography

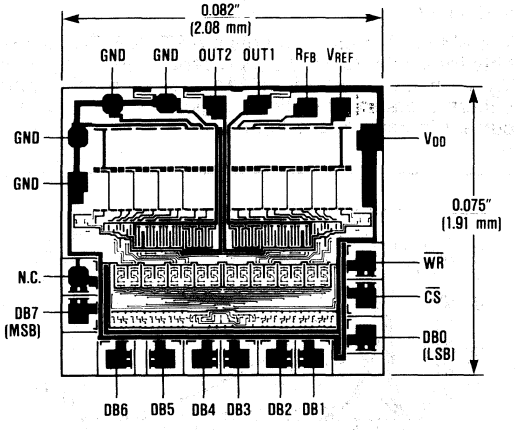


Table 1. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{127}{126}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: 1LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

CMOS Dual 8-Bit Buffered Multiplying DACs

General Description

The AD7528/AD7628 contains two 8-bit multiplying digital-to-analog converters (DACs). Separate on-chip latches hold the input data for each DAC to allow easy interface to microprocessors. The data load operation is similar to a static RAM write cycle. Data is loaded using only CS, WR, and DAC Select (DAC A/DAC B) inputs.

Each DAC has a separate reference input and internal feedback resistor which allow fully independent operation while maintaining excellent DAC-to-DAC matching.

The AD7528 operates from a single +5V to +15V power supply whereas the AD7628 operates from +12V to +15V. The AD7528 has TTL compatible inputs at +5V supply only and the AD7628 has TTL compatible inputs from +12V to +15V supplies.

The AD7528/AD7628 is supplied in 20-lead narrow DIP and Small Outline Packages.

Applications

Programmable Attenuators

Digitally Controlled Filters

X-Y Graphics

Motion Control Systems

Digital-to-Synchro Conversion

Disk Drives

Features

- Data Latches For Both DACs
- AD7528—+5V to +15V Single Supply Operation
- AD7628—+12V to +15V Single Supply Operation With TTL/CMOS Compatible Inputs
- ±½ LSB Linearity
- Microprocessor Compatible
- Four-Quadrant Multiplication
- DACs Matched to 1%

Ordering Information

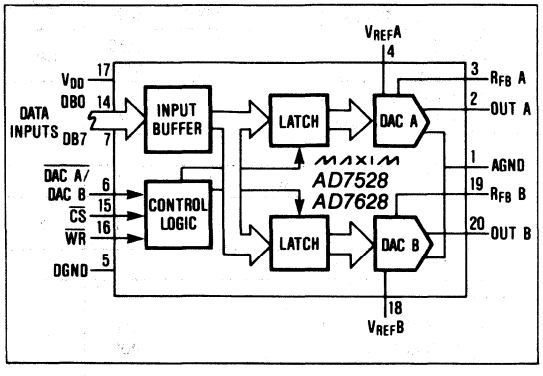
PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7528KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7528JCWP	0°C to +70°C	Small Outline	±1 LSB
AD7528KCWP	0°C to +70°C	Small Outline	±½ LSB
AD7528LCWP	0°C to +70°C	Small Outline	±½ LSB
AD7528JC/D	0°C to +70°C	Dice	±1 LSB
AD7528AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7528BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7528CQ	-25°C to +85°C	CERDIP**	±½ LSB

* *All devices — 20 lead packages*

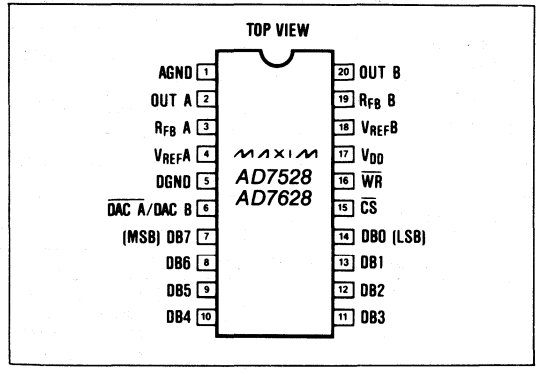
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Ordering Information continued on last page.

Functional Diagram



Pin Configuration



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CMOS Dual 8-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS—AD7528, AD7628

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
Pin 2, Pin 20 to AGND ..... -0.3V, V_{DD}
$V_{REF}A$, $V_{REF}B$ to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V

Operating Temperature Ranges
AD7528JN, KN, LN, JCWP,
KCWP, LCWP; AD7628KN, KCWP ..... 0°C to +70°C
AD7528AQ, BQ, CQ; AD7628BQ ..... -25°C to +85°C
AD7528SD, SQ, TD, TQ,
UD, UQ; AD7628TQ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 450mW
Derate Above +75°C by ..... 6 mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation

(V_{DD} = +5V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	All Grades Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		J,A,S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±6	LSB
		K,B,T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±4	
		L,C,U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±3	
Gain Temp. Coefficient (Note 2, 3)					±2	±70	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.02 0.04	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±400	nA
REFERENCE INPUT							
R_{IN} ($V_{REF}A$, $V_{REF}B$)				8	10	15	kΩ
$V_{REF}A$, $V_{REF}B$ Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns

ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			220 270	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		60		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		30		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 4)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

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ELECTRICAL CHARACTERISTICS—AD7528, +5V Operation (Continued)

(V_{DD} = +5V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	200 230			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	20 30			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	180 200			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	110 130			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation

(V_{DD} = +15V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL	J,A,S K,B,T L,C,U				±1 ±1/2 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		J,A,S	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±4 ±5	LSB
		K,B,T	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±2 ±3	
		L,C,U	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±1	
Gain Temp. Coefficient (Note 2, 3)					±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT							
R_{IN} (V_{REF}A, V_{REF}B)				8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		$\overline{DB0}$-$\overline{DB7}$ = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			180 200	ns

ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
Propagation Delay (from digital input to 90% of final analog output current)		DB0-DB7 = 0V to V_{DD} to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF; T_A = 25°C T_A = T_{MIN} to T_{MAX}			80 100	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111		125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000 DAC latches loaded with 11111111			50 120	pF pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		13.5			V
Input Low Voltage	V_{IL}				1.5	V
Input Current	I_{IN}	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±1 ±10	μA
Input Capacitance (Note 4)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, DAC A/DAC B			10 15	pF
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH} T_A = 25°C T_A = T_{MIN} to T_{MAX}			1 1	mA
		Digital inputs 0V or V_{DD} T_A = 25°C T_A = T_{MIN} to T_{MAX}			100 500	μA
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Chip Select to Write Hold Time	t_{CH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns

Note 1: Specifications apply to both DACs in AD7528.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

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ELECTRICAL CHARACTERISTICS—AD7528, +15V Operation (Continued)

(V_{DD} = +15V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram) (Continued)						
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
DAC Select to Write Hold Time	t_{AH}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	10 15			ns
Write Pulse Width	t_{WR}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Data Setup Time	t_{DS}	T_A = 25°C T_A = T_{MIN} to T_{MAX}	30 40			ns
Data Hold Time	t_{DH}		0			ns

ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation

(V_{DD} = +10.8V to +15.75V; V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				8			Bits
Relative Accuracy	INL					±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.				±1	LSB
Gain Error (Note 2)		T_A = 25°C T_A = T_{MIN} to T_{MAX}				±2 ±3	LSB
Gain Temp. Coefficient (Note 2, 3)					±2	±35	ppm/°C
Supply Rejection (Note 4)	PSR	ΔV_{DD} = ±5%	T_A = 25°C T_A = T_{MIN} to T_{MAX}		0.001 0.001	0.01 0.02	%FSR/%
Output Leakage Current (OUTA)		DAC A is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
Output Leakage Current (OUTB)		DAC B is 00000000	T_A = 25°C T_A = T_{MIN} to T_{MAX}			±50 ±200	nA
REFERENCE INPUT							
R_{IN} (V_{REF}A, V_{REF}B)				8	10	15	kΩ
V_{REF}A, V_{REF}B Input Resistance Match						±1	%
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling-Time to 1/2 LSB		DB0-DB7 = 0V to +5V to 0V $\overline{WR}$ = $\overline{CS}$ = 0V OUTA = OUTB Load = 100Ω, C_{EXT} = 13pF;	T_A = 25°C T_A = T_{MIN} to T_{MAX}			350 400	ns
Digital to Analog Glitch Impulse		For code transition 00000000 to 11111111			125		nV-sec
AC Feedthrough (V_{REF}A to OUTA)		V_{REF}A = ±10V 100kHz Sinewave V_{REF}B = 0V	T_A = 25°C T_A = T_{MIN} to T_{MAX}			-70 -65	dB

Note 1: Specifications apply to both DACs in AD7628.
Note 2: Gain error is measured using internal feedback resistor. Full Scale Range (FSR) = V_{REF}.
Note 3: Guaranteed, but not tested.
Note 4: These characteristics are for design guidance only and are not subject to test.

ELECTRICAL CHARACTERISTICS—AD7628, +12V to +15V Operation (Continued)

(V_{DD} = +10.8V to +15.75V, V_{REF} = +10V; V_{OUTA} = V_{OUTB} = 0V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Note 4) (Continued)						
AC Feedthrough (V_{REF}B to OUTB)		V_{REF}B = ±10V, 100kHz Sinewave, V_{REF}A = 0V; T_A = 25°C			-70	dB
		T_A = T_{MIN} to T_{MAX}			-65	
Channel to Channel Isolation (V_{REF}A to OUTB)		V_{REF}A = ±10V 100kHz Sinewave; V_{REF}B = 0V, both DACs loaded with 11111111		-90		dB
Channel to Channel Isolation (V_{REF}B to OUTA)		V_{REF}B = ±10V 100kHz Sinewave; V_{REF}A = 0V, both DACs loaded with 11111111		-90		dB
Digital Crosstalk		Measured with code transition 0 to FS		60		nV-sec
Harmonic Distortion	THD	V_{IN} = 6V rms @ 1kHz		-85		dB
ANALOG OUTPUTS (Note 4)						
OUTA Capacitance	C_{OUTA}	DAC latches loaded with 00000000			25	pF
		DAC latches loaded with 11111111			60	pF
OUTB Capacitance	C_{OUTB}	DAC latches loaded with 00000000			25	pF
		DAC latches loaded with 11111111			60	pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	T_A = 25°C			±1	μA
		T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 4)	C_{IN}	DB0-DB7			10	pF
		$\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B			15	
POWER REQUIREMENTS						
Supply Current	I_{DD}	Digital inputs V_{IL} or V_{IH}; T_A = 25°C			2	mA
		T_A = T_{MIN} to T_{MAX} K			2	
		T_A = T_{MIN} to T_{MAX} B,T			2.5	
		Digital inputs 0V or V_{DD}; T_A = 25°C			100	μA
		T_A = T_{MIN} to T_{MAX}			500	
SWITCHING CHARACTERISTICS (Note 4) (See Timing Diagram)						
Chip Select to Write Setup Time	t_{CS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
Chip Select to Write Hold Time	t_{CH}		10			ns
DAC Select to Write Setup Time	t_{AS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
DAC Select to Write Hold Time	t_{AH}		10			ns
Write Pulse Width	t_{WR}	T_A = 25°C	150			ns
		T_A = T_{MIN} to T_{MAX} K,B	170			
		T_A = T_{MIN} to T_{MAX} T	210			
Data Setup Time	t_{DS}	T_A = 25°C	160			ns
		T_A = T_{MIN} to T_{MAX} K,B	160			
		T_A = T_{MIN} to T_{MAX} T	210			
Data Hold Time	t_{DH}		10			ns

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Interface Logic Information

DAC Selection

Both DAC latches share a common 8-Bit input port. The control input DAC A/DAC B selects which DAC will accept data from the input port.

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table.

Mode Selection Table

$\overline{DAC\ A}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low state, H = High state, X = Don't care

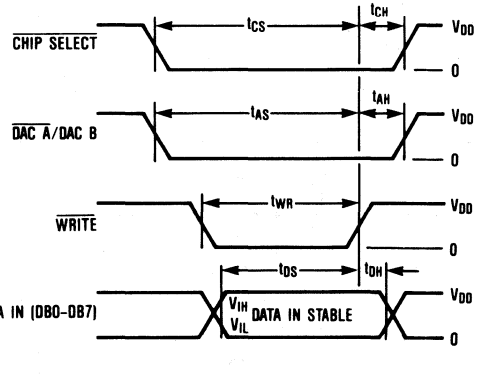
Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both low, the selected DAC is in the write mode. The input latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0–DB7.

Hold Mode

The selected DAC latch retains the data that was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Write Cycle Timing Diagram



Note 1: For the AD7528, all input signal rise and fall times are measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.

Note 2: For the AD7628, all input signal rise and fall times are measured from 10% to 90% of +5V. $t_r = t_f$ = 20ns; V_{DD} = +10.8V to +15.75V.

Note 3: Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Detailed Description

The AD7528/AD7628 contains two identical 8-Bit multiplying digital-to-analog converters (DAC). Each DAC circuit consists of a thin-film R-2R resistor array with CMOS current steering switches. Figure 1 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at the OUT terminal depends on the number of switches selected, and therefore the output is an analog representation of the digital input. The DAC OUT and analog ground terminals must be maintained at the same potential for proper operation.

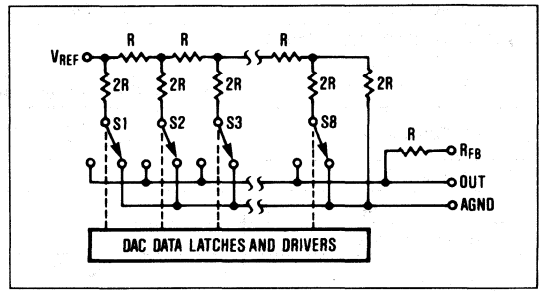


Figure 1. Simplified DAC Schematic

Equivalent-Circuit Analysis

The DAC equivalent-circuit, typical of both DACs, is shown in figure 2. Each DAC shares the analog ground pin 1. When all the digital inputs are high, 255/256 of the reference current flows to OUT A. A small junction leakage current ($I_{LEAKAGE}$), which doubles every 10°C, also flows to the output. The R-2R ladder termination resistor generates a constant 1/256 current which represents 1 LSB of the reference current, I_{REF}. C_{OUT} is the parallel combination of the capacitance associated with the individual NMOS current steering switches. The value of output capacitance is input code dependent and lies in the range 20pF to 30pF. The equivalent output resistance, R_O, also varies with input code in the range 0.8R to 3R, where R is the nominal ladder resistance.

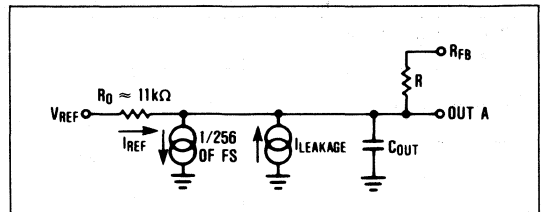


Figure 2. DAC Equivalent Circuit. All Digital Inputs High

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Circuit Information—Digital Section

The AD7528's digital inputs are TTL compatible when operated with a V_{DD} of +5V (V_{IH} = 2.4V, V_{IL} = 0.8V). Internal level shifters convert from TTL to CMOS logic levels. When V_{IN} is in the region of 1.0 to 3.5 volts, the input buffers operate in their linear region and the quiescent current increases as indicated by the graph in figure 3. Therefore to minimize supply current it is recommended that the digital inputs be as close to the supply rails as possible (V_{DD} and DGND).

The AD7528 may be operated with any supply voltage in the range 5V < V_{DD} < 15V. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e. 1.5V and 13.5V.

The AD7628's digital inputs are TTL and CMOS compatible with any supply voltage in the range of +12V to +15V.

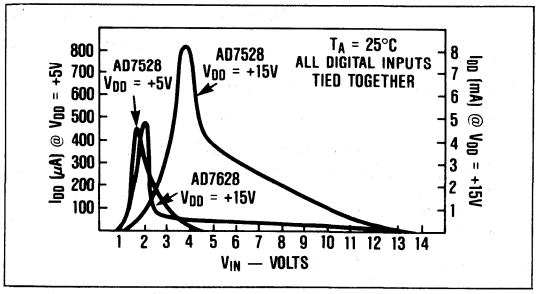
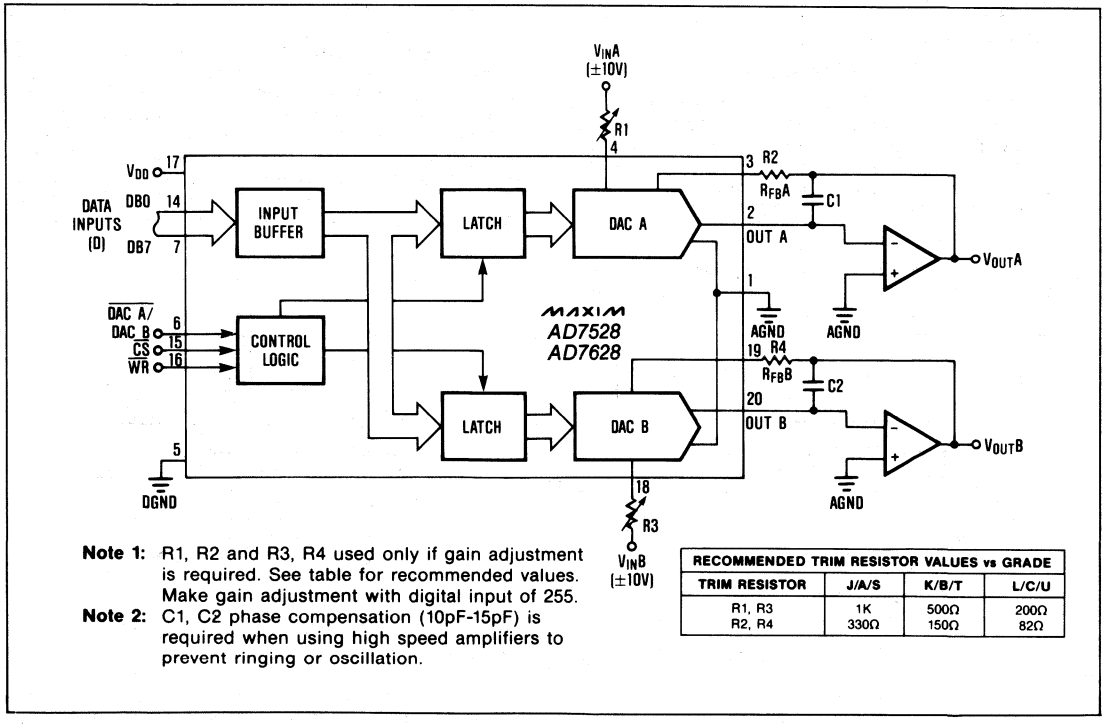


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



Note 1: R1, R2 and R3, R4 used only if gain adjustment is required. See table for recommended values. Make gain adjustment with digital input of 255.

Note 2: C1, C2 phase compensation (10pF-15pF) is required when using high speed amplifiers to prevent ringing or oscillation.

RECOMMENDED TRIM RESISTOR VALUES vs GRADE			
TRIM RESISTOR	J/A/S	K/B/T	L/C/U
R1, R3	1K	500Ω	200Ω
R2, R4	330Ω	150Ω	82Ω

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication)

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Applications Information

To ensure system performance consistent with the AD7528/AD7628 specifications, careful attention must be given to the following points:

1. General Ground Management:

   AC or transient voltages between the AD7528/AD7628 AGND and DGND can cause noise injection into the analog output. Therefore, whenever possible, the analog and digital ground pins should be tied together at the AD7528/AD7628.

2. Output Amplifier Offset:

   CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The result is a code-dependent differential nonlinearity term at the amplifier output which depends on the amplifier's offset voltage, V_{OS}. The offset dependent nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier offset voltage should be no more than 1/10 LSB over the operating temperature range.

3. High Frequency Considerations:

   The combination of DAC output capacitance and the amplifier's feedback resistance adds a pole to the open-loop response which can cause ringing or oscillation in severe cases. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. Dynamic Performance:

   The dynamic performance of the two DACs in the AD7528/AD7628 depends on the gain and phase characteristics of the output amplifiers, together with the stray capacitance contributed by the PC layout, and the power supply decoupling components. A 0.1μF decoupling capacitor is recommended between V_{DD} and DGND.

5. Circuit Layout Suggestions:

   Analog and digital ground traces should be routed between the package pins to reduce coupling between the digital inputs and the analog output. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, and 4-5 to minimize reference feedthrough to the output in multiplying applications.

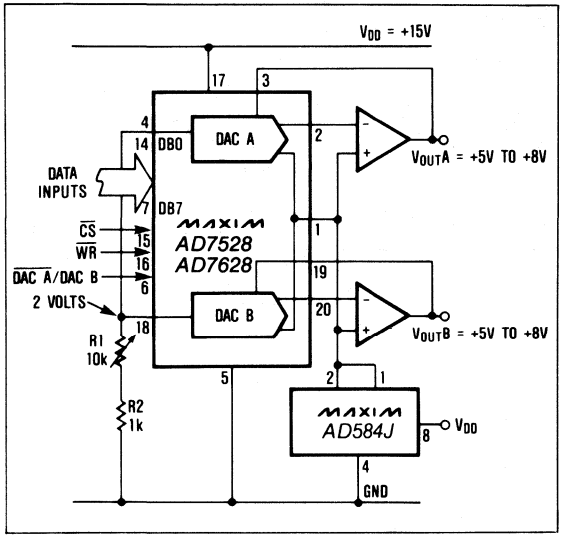


Figure 5. AD7528/AD7628 Single Supply Operation

Single Supply Operation

The AD7528/AD7628 R-2R ladder termination resistors are internally connected to AGND. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between V_{DD} and DGND. Figure 5 shows a circuit which provides dual +5V to +8V analog outputs by biasing AGND 5V above DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the stable matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1, and R1 is adjusted until $V_{REF}A$ and $V_{REF}B$ inputs are at +2V. DAC codes from 00000000 to 11111111 adjust the analog output voltages from +5V to +8V in 11.7mV steps.

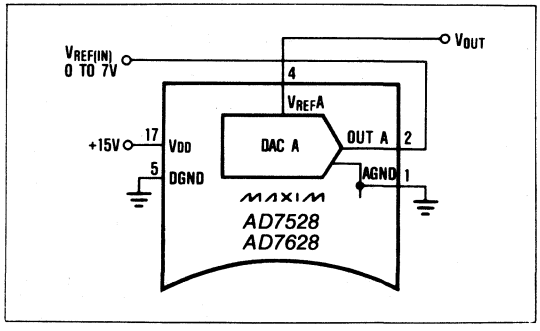
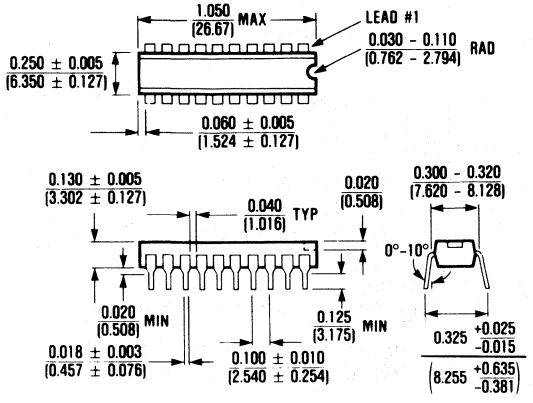


Figure 6. AD7528/AD7628 in Single Supply, Voltage Switching Mode

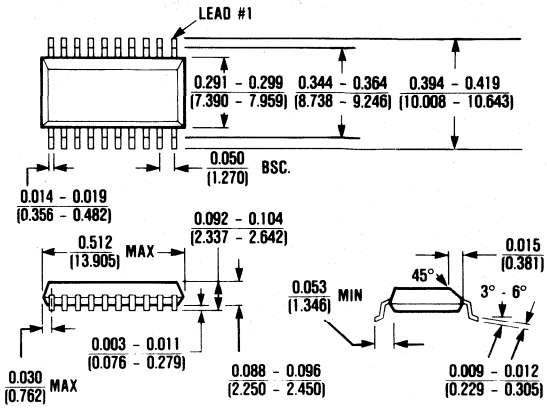
Figure 6 shows one DAC of the AD7528/AD7628 connected in the voltage switching mode which uses a positive reference voltage. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to maintain linearity, V_{IN} must be limited to approximately +7V (V_{DD} = +15V), and the output must be buffered or loaded with a high impedance. In the voltage switching mode, the output resistance is independent of the digital input code and is typically 10kΩ.

Package Information



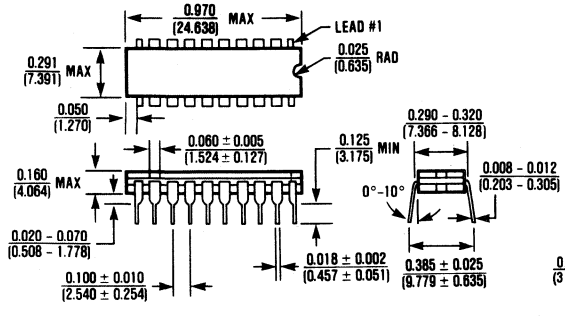
20 Lead Plastic DIP

θ_{JA} = 125°C/W
θ_{JC} = 60°C/W



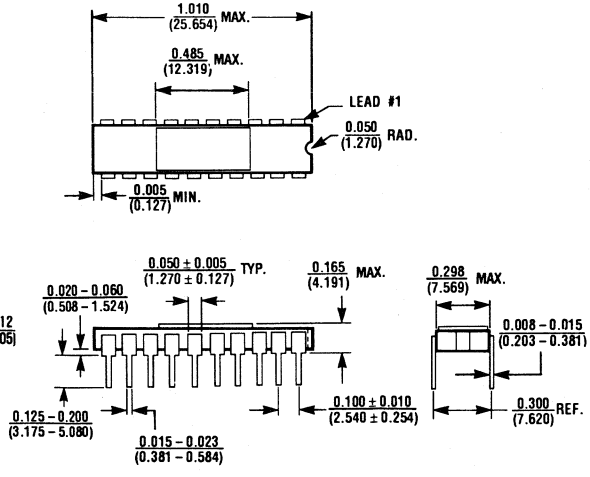
20 Lead Small Outline, Wide

θ_{JA} = 90°C/W
θ_{JC} = 50°C/W



20 Lead CERDIP

θ_{JA} = 90°C/W
θ_{JC} = 40°C/W



20 Lead Ceramic Sidebraze

θ_{JA} = 85°C/W
θ_{JC} = 35°C/W

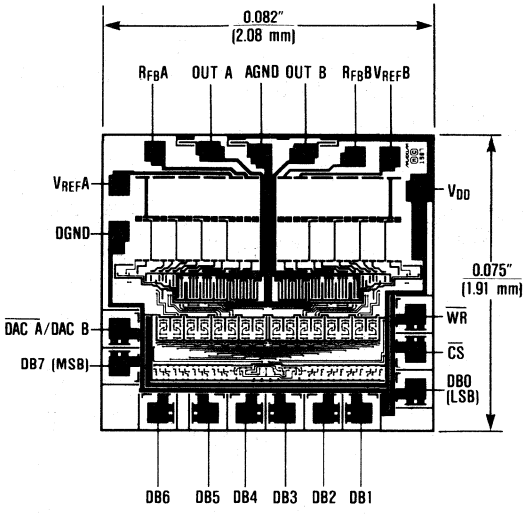
CMOS Dual 8-Bit Buffered Multiplying DACs

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7528SD	-55°C to +125°C	Ceramic	±1 LSB
AD7528TD	-55°C to +125°C	Ceramic	±½ LSB
AD7528UD	-55°C to +125°C	Ceramic	±½ LSB
AD7528SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7528TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7528UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7628KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7628KCWP	0°C to +70°C	Small Outline	±½ LSB
AD7628KC/D	0°C to +70°C	Dice	±½ LSB
AD7628BQ	-25°C to +85°C	CERDIP	±½ LSB
AD7628TQ	-55°C to +125°C	CERDIP	±½ LSB

* *All devices — 20 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Chip Topography



MAXIM

CMOS 10 and 12 Bit Multiplying D/A Converters

General Description

The AD7530 and AD7531 are low cost CMOS multiplying digital-to-analog converters (DAC) with 10 and 12 bit resolution respectively. Both DACs operate from a single +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C maximum gain tempco. All digital inputs are compatible with both CMOS and TTL logic levels.

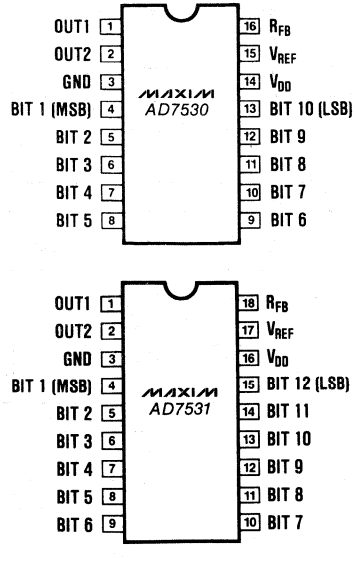
Maxim's AD7530 and AD7531 are electrically and pin compatible with Analog Devices' AD7530 and AD7531. The AD7530 is packaged in a 16-lead DIP and the AD7531 is packaged in an 18-lead DIP. Both parts are available in Small Outline packages as well.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Pin Configurations

Top View



Features

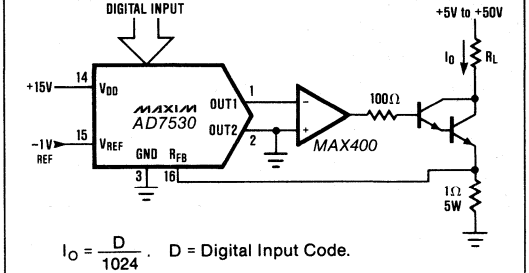
- ♦ 10 or 12 Bit Resolution
- ♦ 8, 9, and 10 Bit End Point Linearity
- ♦ Low Power Consumption - 20mW
- ♦ Four-Quadrant Multiplication
- ♦ TTL and CMOS Compatible
- ♦ Pin-For-Pin Second Source

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7530JN	0°C to +70°C	Plastic DIP	0.2%
AD7530KN	0°C to +70°C	Plastic DIP	0.1%
AD7530LN	0°C to +70°C	Plastic DIP	0.05%
AD7530JCWE	0°C to +70°C	Small Outline	0.2%
AD7530KCWE	0°C to +70°C	Small Outline	0.1%
AD7530LCWE	0°C to +70°C	Small Outline	0.05%
AD7530JC/D	0°C to +70°C	Dice	0.2%
AD7530JD	-25°C to +85°C	Ceramic	0.2%
AD7530KD	-25°C to +85°C	Ceramic	0.1%
AD7530LD	-25°C to +85°C	Ceramic	0.05%
AD7530JQ	-25°C to +85°C	CERDIP**	0.2%
AD7530KQ	-25°C to +85°C	CERDIP**	0.1%
AD7530LQ	-25°C to +85°C	CERDIP**	0.05%

* *AD7530 — 16 lead package, AD7531 — 18 lead package*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*
Ordering information continued on last page.

Typical Operating Circuit



$I_O = \frac{D}{1024}$. D = Digital Input Code.

Digital Current Controller

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
Commercial (JN/KN/LN/JC/KC/LC) ..... 0°C to +70°C
Industrial (JD/KD/LD/JQ/KQ/LQ) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS			MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)								
Resolution		AD7530 AD7531			10 12			Bits
Relative Accuracy		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX}	0.2% FSR = 8 Bits 0.1% FSR = 9 Bits 0.05% FSR = 10 Bits	J K L			±0.2 ±0.1 ±0.05	% FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)					2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V				0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V, (Note 3)					10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}				300		nA
Power Supply Rejection	PSRR					50		ppm/%
V_{REF} Input Resistance	R_{REF}					10		kΩ
Reference Input Range		±10V typical input				±1		mA
AC ACCURACY								
Output Current Settling Time		To 0.05% of FSR, all digital inputs high to low and low to high.				500		ns
Feedthrough Error (Note 3,4)		All digital inputs low, V_{REF} = $20V_{P-P}$, 50kHz sine					10	mV_{P-P}
ANALOG OUTPUTS								
Output Current Range		Both Outputs				±1		mA
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high, All digital inputs low,		OUT1 OUT2 OUT1 OUT2		120 37 37 120		pF
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance				10		kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})								
Low State Threshold	V_{INL}						0.8	V
High State Threshold	V_{INH}				2.4			V
Input Current		Low to high state				1		µA
Input Coding		Unipolar (Table 1) Bipolar (Table 2)			Binary Offset Binary			
POWER REQUIREMENTS								
Power Supply Range	V_{DD}				+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND Digital inputs high or low				5	 2	nA mA
Total Power Dissipation		Including ladder				20		mW

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: Guaranteed by design, but not 100% tested.
Note 4: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

CMOS 10 and 12 Bit Multiplying D/A Converters

Detailed Description

The basic AD7530/31 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

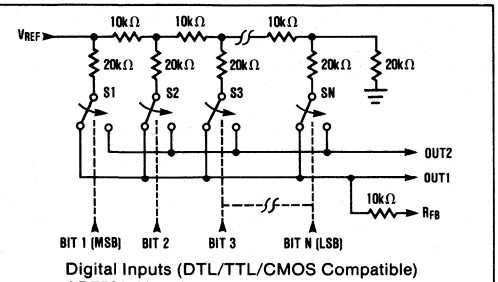


Figure 1. AD7530/AD7531 Functional Diagram

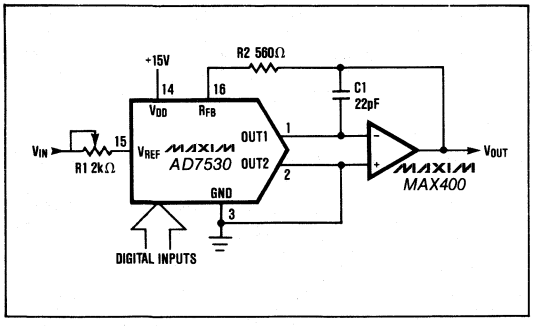


Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the AD7530/31 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 can be used for gain adjustment if desired, if not, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The value depends on the type of op-amp used but typically ranges from 10 to 50pF.

The output op-amp's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7530 and 250nA for the AD7531.

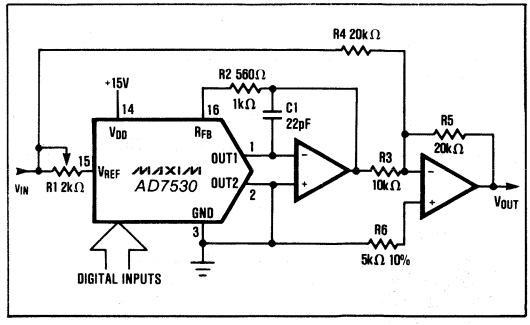


Figure 3. Bipolar Operation (4-Quadrant Multiplicaiton)

Table 1: Code Table (AD7530) — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(½ + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(½ - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Note: 1 LSB = 2^{-10} V_{REF} (AD7530)

Table 2: Code Table (AD7530) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = 2^{-9} V_{REF} (AD7530)

CMOS 10 and 12 Bit Multiplying D/A Converters

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB sets polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

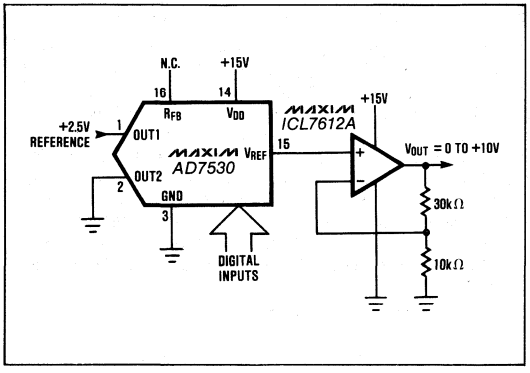


Figure 4. Single Operation Using Voltage Mode

Voltage Mode (Single Supply)

The AD7530 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This outptut is usually buffered with an op-amp.

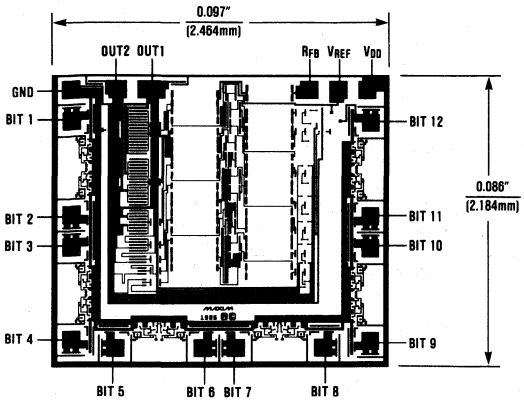
An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted in voltage mode. The reference input (voltage at OUT1) must always be positive and is limited to no more than +3.5V when V_{DD} is +15V. If the reference voltage is greater than +3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

A common error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough from V_{REF} and the digital inputs can be minimized with guard traces to isolate the digital inputs, V_{REF}, and the DAC outputs.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7531JN	0°C to +70°C	Plastic DIP	0.2%
AD7531KN	0°C to +70°C	Plastic DIP	0.1%
AD7531LN	0°C to +70°C	Plastic DIP	0.05%
AD7531JCWN	0°C to +70°C	Small Outline	0.2%
AD7531KCWN	0°C to +70°C	Small Outline	0.1%
AD7531LCWN	0°C to +70°C	Small Outline	0.05%
AD7531KJC/D	0°C to +70°C	Dice	0.2%
AD7531JD	-25°C to +85°C	Ceramic	0.2%
AD7531KD	-25°C to +85°C	Ceramic	0.1%
AD7531LD	-25°C to +85°C	Ceramic	0.05%
AD7531JQ	-25°C to +85°C	CERDIP**	0.2%
AD7531KQ	-25°C to +85°C	CERDIP**	0.1%
AD7531LQ	-25°C to +85°C	CERDIP**	0.05%

** AD7530 — 16 lead package, AD7531 — 18 lead package*

*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

MAXIM

CMOS Low Cost 10 Bit Multiplying D/A Converter

General Description

The AD7533 is a low cost CMOS 4-quadrant multiplying digital-to-analog converter (DAC). An advanced silicon gate CMOS process combines 10 bit linearity, low power consumption, and excellent long term stability. Thin-film resistors provide 1.4% untrimmed gain error and less than 0.1% gain change with temperature over all operating ranges.

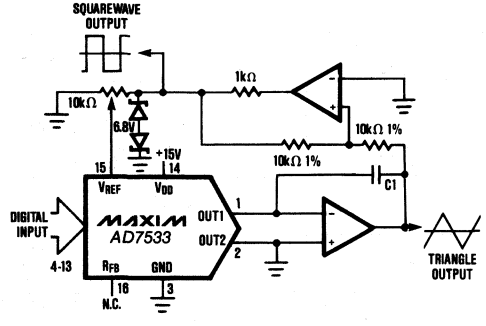
The device operates from a single +5V to +15V supply. All digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7533 is pin and functionally compatible with Analog Devices' AD7533 as well as the AD7520. It is packaged in 16-lead DIP and small outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Programmable Function Generator

Features

- 10 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption - 20mW
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

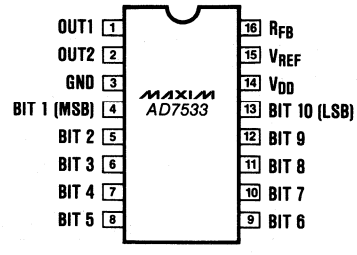
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7533JN	0°C to +70°C	Plastic DIP	0.2%
AD7533KN	0°C to +70°C	Plastic DIP	0.1%
AD7533LN	0°C to +70°C	Plastic DIP	0.05%
AD7533JCWE	0°C to +70°C	Small Outline	0.2%
AD7533KCWE	0°C to +70°C	Small Outline	0.1%
AD7533LCWE	0°C to +70°C	Small Outline	0.05%
AD7533JC/D	0°C to +70°C	Dice	0.2%
AD7533AQ	-25°C to +85°C	CERDIP**	0.2%
AD7533BQ	-25°C to +85°C	CERDIP**	0.1%
AD7533CQ	-25°C to +85°C	CERDIP**	0.05%
AD7533AD	-25°C to +85°C	Ceramic	0.2%
AD7533BD	-25°C to +85°C	Ceramic	0.1%
AD7533CD	-25°C to +85°C	Ceramic	0.05%
AD7533SQ	-55°C to +125°C	CERDIP**	0.2%
AD7533TQ	-55°C to +125°C	CERDIP**	0.1%
AD7533UQ	-55°C to +125°C	CERDIP**	0.05%
AD7533SD	-55°C to +125°C	Ceramic	0.2%
AD7533TD	-55°C to +125°C	Ceramic	0.1%
AD7533UD	-55°C to +125°C	Ceramic	0.05%

* *All devices — 16 lead packages.*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



CMOS Low Cost 10 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation
  Plastic DIP (Derate 8.3mW/° C above +70° C) 670mW
  Ceramic, CERDIP, Small Outline
    (Derate 6mW/° C above +75° C) 450mW

Operating Temperature Range
  Commercial J/K/L ..... 0° C to +70° C
  Industrial A/B/C ..... -25° C to +85° C
  Military S/T/U ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

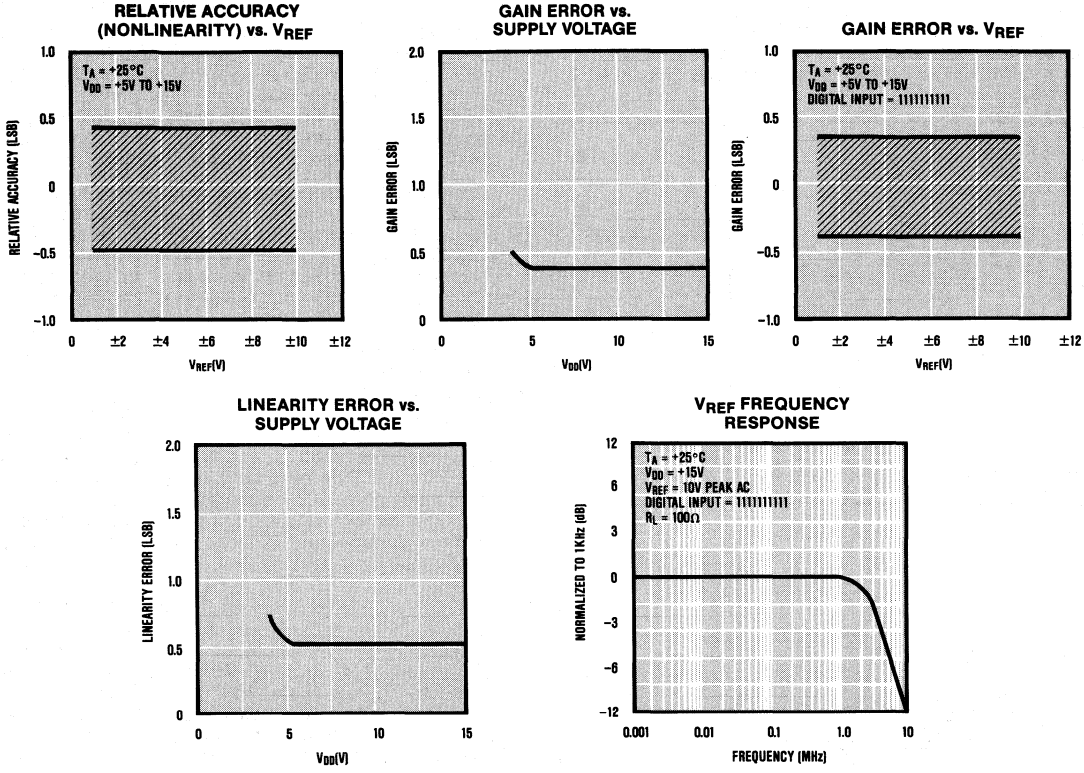
($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				10			Bits
Relative Accuracy (Note 2)		AD7533J/A/S AD7533K/B/T AD7533L/C/U				±0.2 ±0.1 ±0.05	% FSR
Gain Error (Note 2,3)		Digital Inputs = V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			±1.4 ±1.5	% FSR
Power Supply Rejection (Note 4) $\Delta Gain/\Delta V_{DD}$	PSRR	V_{DD} = +14V to +17V	T_A = +25°C T_{MIN} to T_{MAX}			0.005 0.008	%/%V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
		OUT2, Digital Inputs = V_{INH}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
V_{REF} Input Resistance	R_{REF}	T_A = +25°C		5	10	20	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DYNAMIC PERFORMANCE							
Output Current Settling Time (Note 5)		To 0.05% of FSR, R_L = 100Ω, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH}.	T_A = +25° C T_{MIN} to T_{MAX}			600 800	ns
Feedthrough Error (Note 4)		Digital Inputs = V_{INL}, V_{REF} = ±10V, 100KHz Sinewave	T_A = +25° C T_{MIN} to T_{MAX}			±0.05 ±0.1	% FSR
Output Capacitance (Note 4)	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 35	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			35 100	pF
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}				±1	μA
Input Capacitance (Note 4)						5	pF
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	+15V ±10% for Rated Accuracy		+13.5		+16.5	V
		Accuracy Not Guaranteed (Note 4)		+5		+16.5	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA

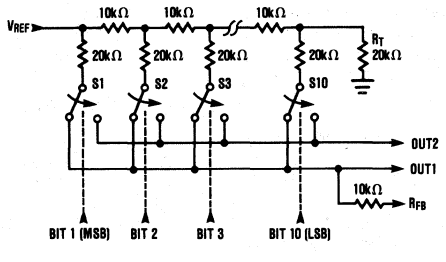
Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.
Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = -(V_{REF} - 1LSB) in unipolar mode.
Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
Note 4: Guaranteed by design but not 100% tested.
Note 5: Guaranteed by design and sample tested at +25°C to ensure compliance.

CMOS Low Cost 10 Bit Multiplying D/A Converter

Typical Operating Characteristics



Detailed Description



Digital Inputs (DTL/TTL/CMOS Compatible)
(Switches Shown for Inputs HIGH)

Figure 1. AD7533 Functional Diagram

The basic AD7533 DAC circuit consists of a thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and an external reference. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 10kΩ and does not change with digital input code. The $I_{REF}/1024$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

CMOS Low Cost 10 Bit Multiplying D/A Converter

Capacitors COUT1 and COUT2 represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from 35pF to 100pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

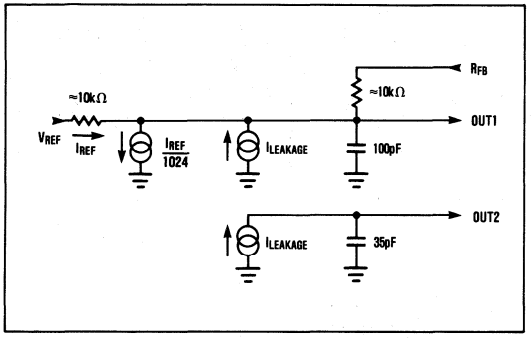


Figure 2. Equivalent DAC Circuit (All digital inputs HIGH)

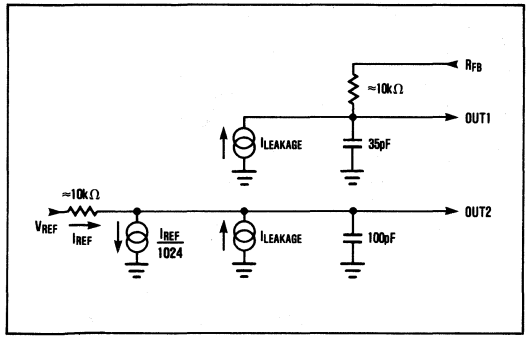


Figure 3. Equivalent DAC Circuit (All digital inputs LOW)

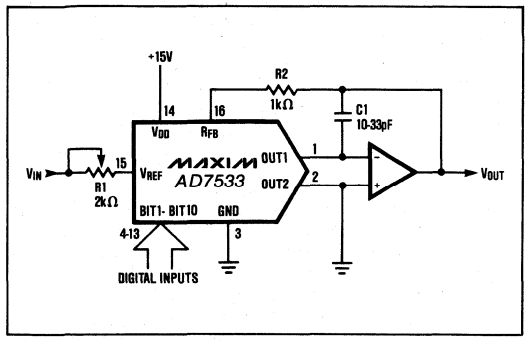


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the AD7533 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 33pF.

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the AD7533.

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 5. A second amplifier and three matched resistors are required. R3, R4, and R5 should be matched or trimmed to 0.05% to maintain 10 bit performance. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines output polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 10000 00000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The AD7533 is connected as a voltage output DAC in Figure 6. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must

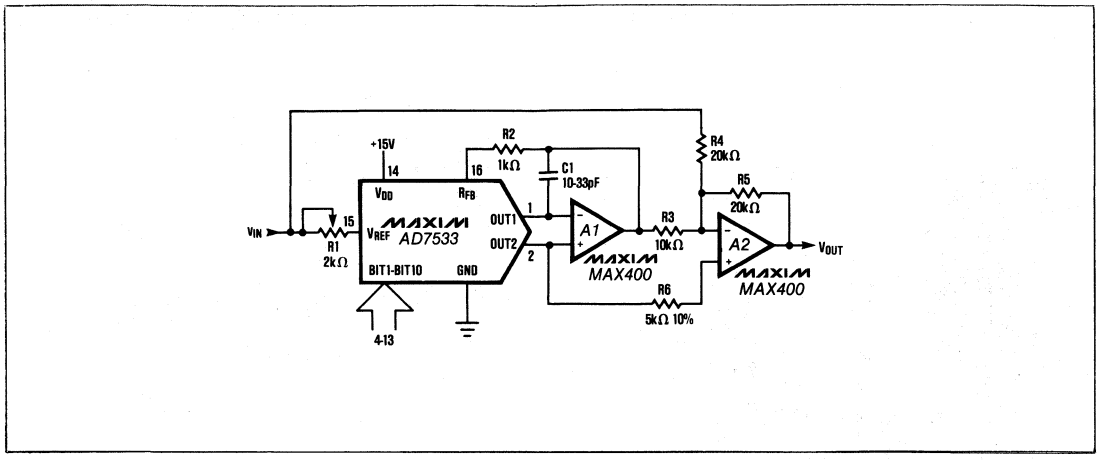


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

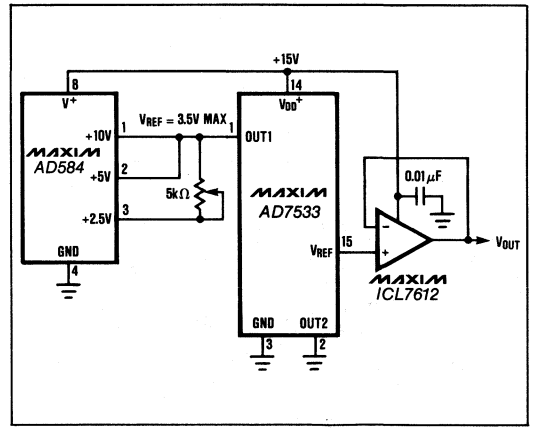


Figure 6. Voltage Mode Operation

Table 1: Code Table — Unipolar Binary Operation

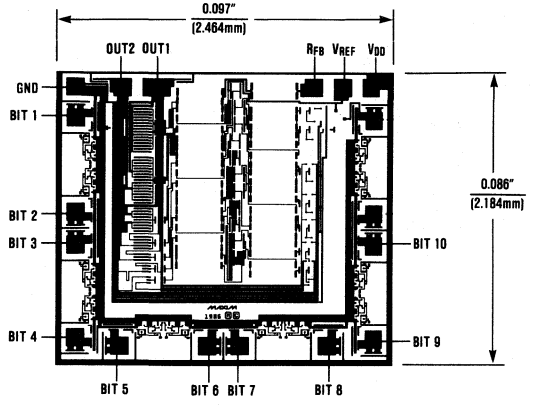
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(½+2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(½-2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Table 2: Code Table — Bipolar (Offset Binary) Operation

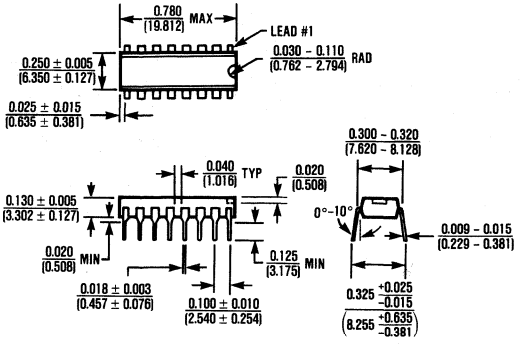
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1-2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1-2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

CMOS Low Cost 10 Bit Multiplying D/A Converter

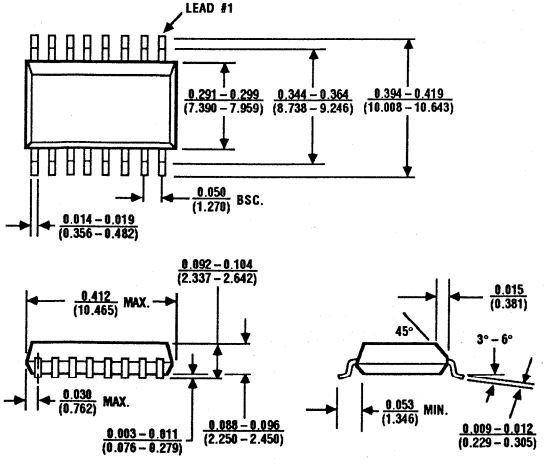
Chip Topography



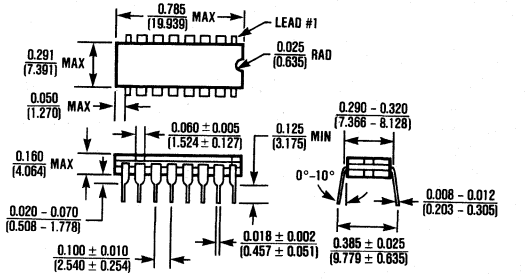
Package Information



16 Lead Plastic DIP (PE)
θ_{JA} = 135°C/W
θ_{JC} = 65°C/W



16 Lead Small Outline, Wide (WE)
θ_{JA} = 105°C/W
θ_{JC} = 60° C/W



16 Lead CERDIP (JE)
θ_{JA} = 100°C/W
θ_{JC} = 50°C/W

MAXIM

CMOS 12 Bit Multiplying D/A Converter

General Description

The AD7541 is a high performance CMOS multiplying 12 bit digital-to-analog converter (DAC). Low power operation and 12-bit linearity (0.012%) make it suitable for a wide range of precision data acquisition and control applications.

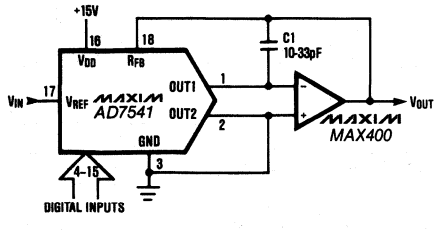
Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7541 is electrically and pin compatible with the Analog Devices AD7541. It is available in standard width 18-lead DIP and Small Outline (SO) packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Unipolar Operation

Features

- 12 Bit Linearity (1/2 LSB)
- 1 LSB Gain Accuracy
- Guaranteed Monotonic
- Low Power Consumption
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

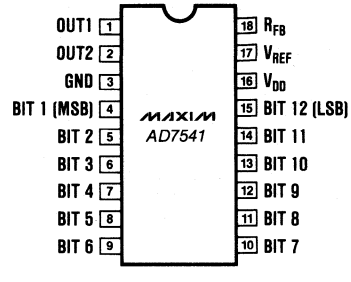
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7541JN	0°C to +70°C	Plastic DIP	1 LSB
AD7541KN	0°C to +70°C	Plastic DIP	½ LSB
AD7541JCWN	0°C to +70°C	Small Outline	1 LSB
AD7541KCWN	0°C to +70°C	Small Outline	½ LSB
AD7541JC/D	0°C to +70°C	Dice	1 LSB
AD7541AQ	-25°C to +85°C	CERDIP**	1 LSB
AD7541BQ	-25°C to +85°C	CERDIP**	½ LSB
AD7541AD	-25°C to +85°C	Ceramic	1 LSB
AD7541BD	-25°C to +85°C	Ceramic	½ LSB
AD7541SQ	-55°C to +125°C	CERDIP**	1 LSB
AD7541TQ	-55°C to +125°C	CERDIP**	½ LSB
AD7541SD	-55°C to +125°C	Ceramic	1 LSB
AD7541TD	-55°C to +125°C	Ceramic	½ LSB

** All devices — 18 lead package.*
*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



CMOS 12 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial AD7541J/K ..... 0°C to +70°C
Industrial AD7541A/B ..... -25°C to +85°C
Military AD7541S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, $V_{OUT1} = V_{OUT2}$ = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC ACCURACY						
Resolution			12			Bits
Nonlinearity		AD7541J/A/S (Note 2) AD7541K/B/T (Note 3)			±1 ±0.5	LSB
Gain Error (Note 4)		Using R_{FB}; T_A = +25°C T_{MIN} to T_{MAX}			±12.5 ±16.7	LSB
Power Supply Rejection	PSRR	V_{DD} = +14.5V to +15.5V; T_A = 25°C T_{MIN} to T_{MAX}			0.01 0.02	%/%V_{DD}
Output Leakage Current		V_{REF} = ±10V; T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
Reference Input Resistance	R_{REF}	T_A = 25°C	5		20	kΩ
DYNAMIC PERFORMANCE (Note 5)						
Output Current Settling Time		To 1/2LSB			1	µs
Feedthrough Error		V_{REF} = 20V_{P-P} at 10kHz			1	mV_{P-P}
DIGITAL INPUTS						
Logic HIGH Threshold	V_{INH}		+2.4			V
Logic LOW Threshold	V_{INL}				+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 5)			8	pF
Input Coding		Binary, Offset Binary				
ANALOG OUTPUTS						
Output Capacitance (Note 5)	C_{OUT}	Digital Inputs = V_{INH} OUT1 OUT2 Digital Inputs = V_{INL} OUT1 OUT2			200 60 60 200	pF
POWER REQUIREMENTS						
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed	+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}			2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: AD7541J/A/S are monotonic to 11 bits.
Note 3: AD7541K/B/T are monotonic to 12 bits.
Note 4: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±4.2 LSBs using internal feedback resistor.
Note 5: Guaranteed by design but not 100% tested.

Detailed Description

The basic AD7541 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and reference source. The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs.

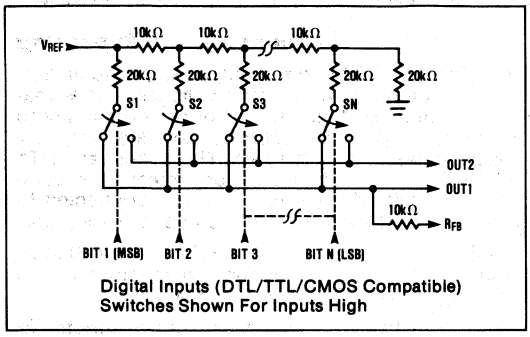
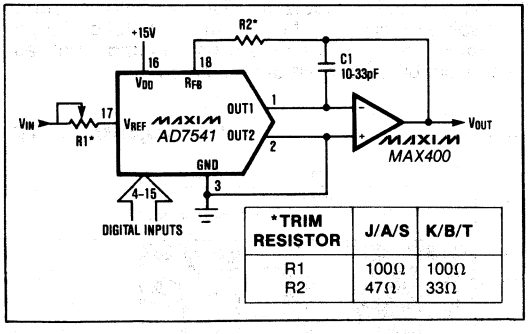


Figure 1. AD7541 Functional Diagram



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 2. Unipolar Binary Operation

Table 1. Code Table — Unipolar Binary

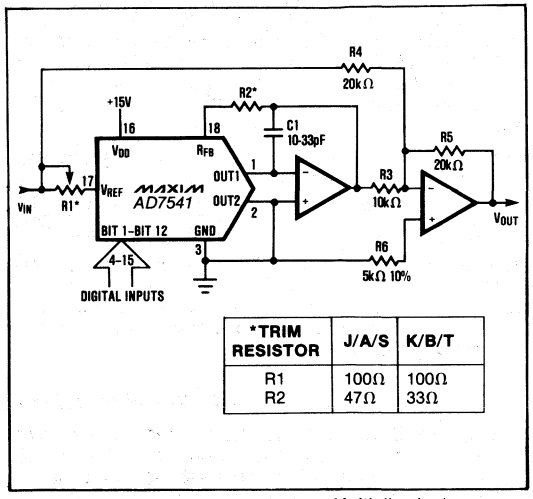
DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0V

Application Information

Unipolar Operation

The most common configuration for the AD7541 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7541 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 2 can be omitted. However, if the trims are required and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

CMOS 12 Bit Multiplying D/A Converter

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications, OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

An output amplifier's input bias current (I_B) can also limit the DAC's performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

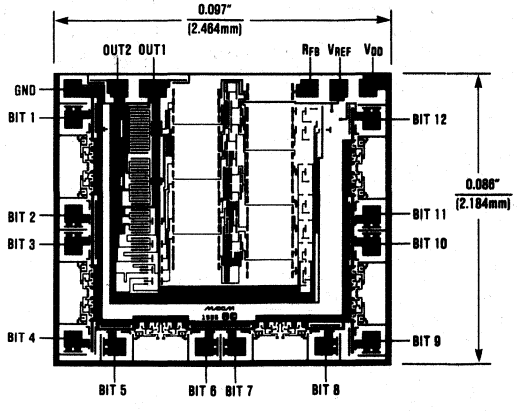
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The AD7541 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



CMOS 12 Bit Multiplying D/A Converter

General Description

The AD7541A is high performance CMOS multiplying 12-bit digital-to-analog converter (DAC). Low power operation and 12 bit (0.012%) linearity make it suitable for a wide range of precision data acquisition and control applications.

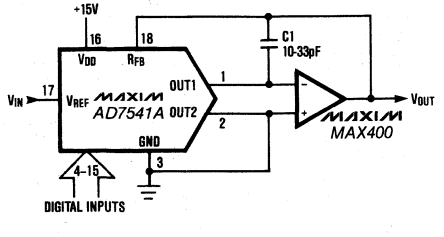
Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure true 12-bit performance over the full operating temperature range. In addition, all digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's AD7541A is electrically and pin compatible with the Analog Devices AD7541A and AD7541. Package types include 18-lead standard width DIP and Small Outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Unipolar Operation

Features

- **12 Bit Linearity (1/2 LSB)**
- **1 LSB Gain Accuracy**
- **Guaranteed Monotonic**
- **Low Power Consumption**
- **Four-Quadrant Multiplication**
- **TTL and CMOS Compatible**
- **Pin-For-Pin Second Source**

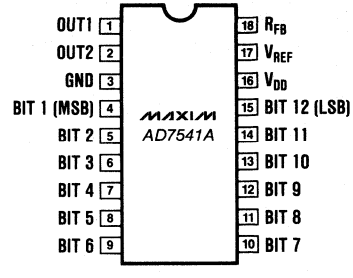
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7541AJN	0° C to +70° C	Plastic DIP	1 LSB
AD7541AKN	0° C to +70° C	Plastic DIP	½ LSB
AD7541AJCWN	0° C to +70° C	Small Outline	1 LSB
AD7541AKCWN	0° C to +70° C	Small Outline	½ LSB
AD7541AJC/D	0° C to +70° C	Dice	1 LSB
AD7541AAQ	-25° C to +85° C	CERDIP**	1 LSB
AD7541ABQ	-25° C to +85° C	CERDIP**	½ LSB
AD7541AAD	-25° C to +85° C	Ceramic	1 LSB
AD7541ABD	-25° C to +85° C	Ceramic	½ LSB
AD7541ASQ	-55° C to +125° C	CERDIP**	1 LSB
AD7541ATQ	-55° C to +125° C	CERDIP**	½ LSB
AD7541ASD	-55° C to +125° C	Ceramic	1 LSB
AD7541ATD	-55° C to +125° C	Ceramic	½ LSB

* *All devices — 18 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Pin Configuration

Top View



CMOS 12 Bit Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature Range
Commercial 7541AJ/AK ..... 0° C to +70° C
Industrial 7541AA/AB ..... -25° C to +85° C
Military 7541AS/AT ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 3)							
Resolution				12			Bits
Relative Accuracy		1 LSB = 0.024% FSR 1/2 LSB = 0.012% FSR	AD7541AJ/AA/AS AD7541AK/AB/AT			±1 ±1/2	LSB
Differential Nonlinearity		12 Bit Monotonicity Guaranteed	AD7541AJ/AA/AS AD7541AK/AB/AT			±1 ±1/2	LSB
Gain Error (Note 3)		AD7541AJ/AA/AS AD7541AK/AB/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±6 ±8 ±1 ±3	LSB
Gain Temperature Coefficient					2	5	ppm/° C
Output Leakage Current (OUT1 with Digital Inputs = 0V, and OUT2 with Digital Inputs = V_{DD})		AD7541AJ/AK/AA/AB AD7541AS/AT	T_A = +25° C T_{MIN} to T_{MAX} T_A = +25° C T_{MIN} to T_{MAX}			±5 ±10 ±5 ±200	nA
Power Supply Rejection	PSRR	V_{DD} = 15V ±5%	T_A = +25° C T_{MIN} to T_{MAX}			±0.01 ±0.02	%/%V_{DD}
V_{REF} Input Resistance	R_{REF}			7	11	18	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	
Input Leakage Current	I_{IN}	Digital Inputs = 0V or V_{DD}	T_A = +25° C T_{MIN} to T_{MAX}		±0.001	±1	μA
Input Capacitance	C_{IN}	(Note 2)				8	pF
DYNAMIC PERFORMANCE (Note 2)							
Propagation Delay to 90% of Final Analog Output		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			100		ns
Digital to Analog Glitch Impulse		V_{REF} = 0V, Dig. Inputs = 0V to V_{DD} or V_{DD} to 0V			1000		nV-sec
Multiplying Feedthrough Error		V_{REF} = ±10V, 10kHz Sinewave, T_A = +25° C			1		mVp-p
Output Current Settling Time to 0.01% of FSR		Digital Input Change 0V to V_{DD} and V_{DD} to 0V, OUT1 Load = 100Ω, C_{EXT} = 13pF, T_A = +25° C			600		ns
Output Capacitance	C_{OUT}	Digital Inputs = V_{INH} Digital Inputs = V_{INL}	OUT1 OUT2 OUT1 OUT2			200 70 70 200	pF

ELECTRICAL CHARACTERISTICS (continued)

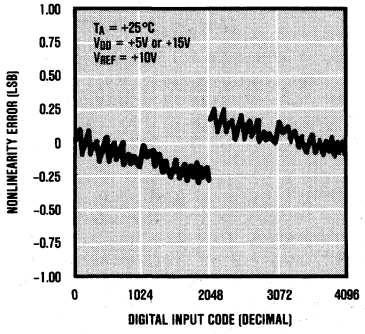
(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	Accuracy Not Guaranteed		+5		+16	V
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA
		Digital Inputs = 0V or V_{DD}	T_A = +25°C			100	μA
			T_{MIN} to T_{MAX}			500	

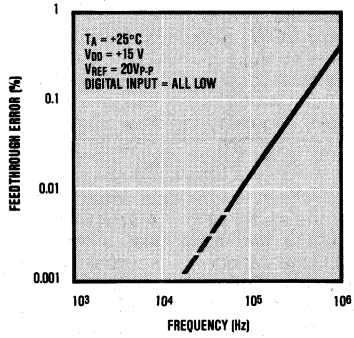
Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum Voltage rating if the current is limited to 30mA or less.
Note 2: Guaranteed by design but not 100% tested.
Note 3: Measured using internal R_{FB} and includes effect of Leakage Current and Gain Tempco. Gain Error can be trimmed to zero.

Typical Operating Characteristics

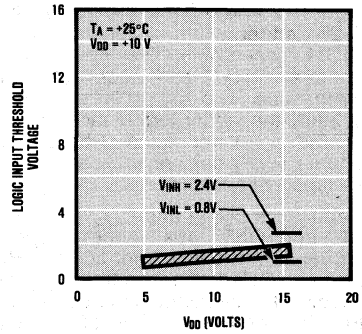
NONLINEARITY ERROR vs. DIGITAL CODE



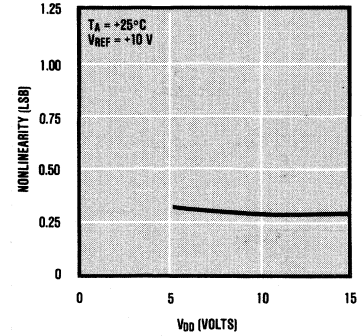
FEEDTHROUGH ERROR vs. FREQUENCY



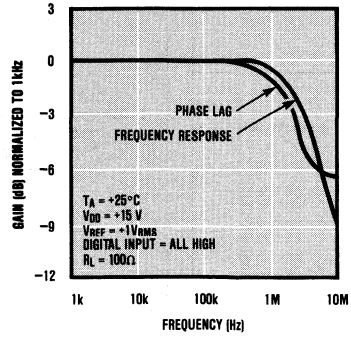
LOGIC INPUT THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE (V_{DD})



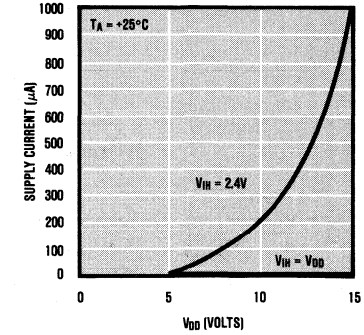
NONLINEARITY vs. SUPPLY VOLTAGE



V_{REF} PHASE LAG AND FREQUENCY RESPONSE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



CMOS 12 Bit Multiplying D/A Converter

Detailed Description

The basic AD7541A DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

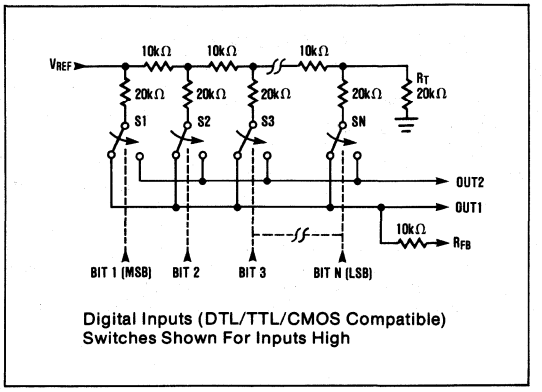


Figure 1. AD7541A Functional Diagram

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 11kΩ and does not change with digital input code. The I_{REF}/4096 current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 70pF to 200pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7541A is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7541A will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

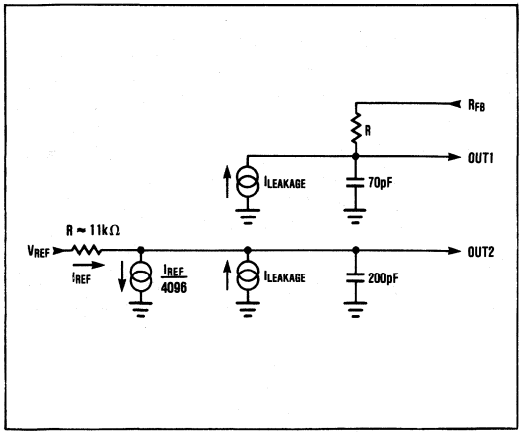


Figure 2. AD7541A DAC Equivalent Circuit, All Digital Inputs LOW

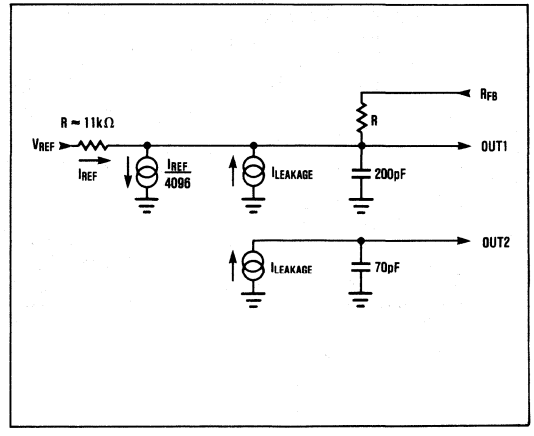
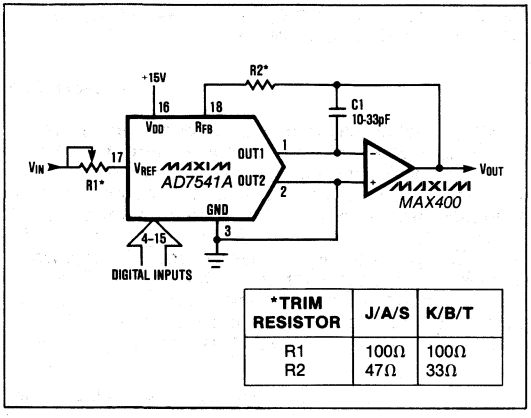
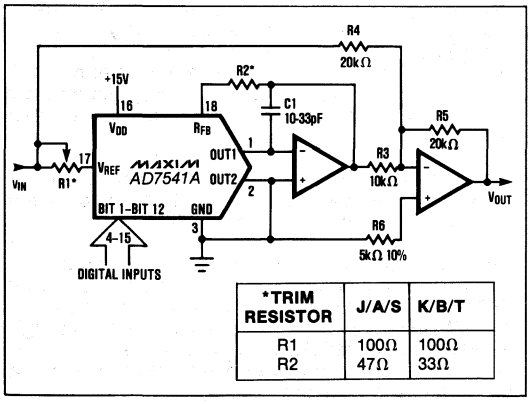


Figure 3. AD7541A DAC Equivalent Circuit, All Digital Inputs HIGH



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 4. Unipolar Binary Operation



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

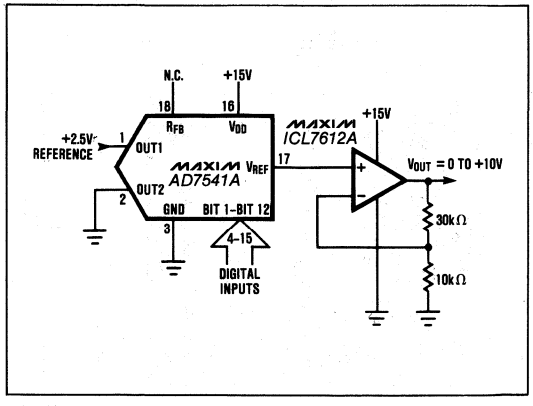


Figure 6. Single Supply Operation Using Voltage Mode

Table 1. Code Table — Unipolar Binary

DIGITAL INPUT MSB											LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2V_{REF}$
0	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{1}{4096}\right)$
0	0	0	0	0	0	0	0	0	0	0	0	0V

Table 2. Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB											LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{2048}\right)$
1	0	0	0	0	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{2048}\right)$
0	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7541A operates in the bipolar, or four-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

Voltage Mode (Single Supply)

The AD7541A is connected as a voltage output DAC in Figure 6. OUT1 is connected to the reference input and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). This output is usually buffered with an op-amp.

CMOS 12 Bit Multiplying D/A Converter

Two advantages of voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal switches degrade linearity.

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 10kΩ to 30kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF}=10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

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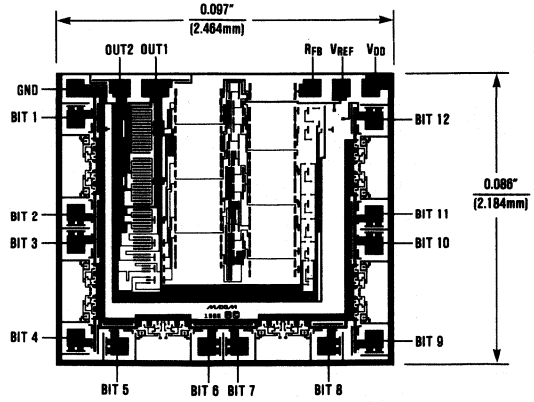
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting input are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The 7541A has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either VDD or GND when not used. It is also good practice to connect active inputs to VDD or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography



CMOS µP-Compatible 12-Bit DAC

General Description

The AD7542 is a CMOS 12-Bit digital-to-analog converter (DAC) which directly interfaces to both 8-bit and 4-bit microprocessors. Input data is loaded as three 4-bit bytes, and is then transferred to an internal 12-bit DAC register. Data load and transfer interface timing is similar to that of a static RAM write cycle.

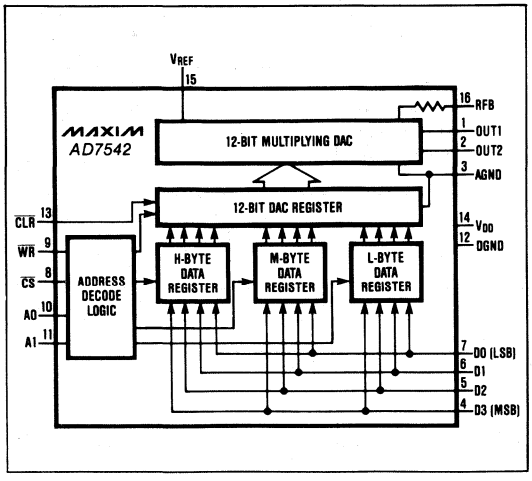
A clear input is also provided which resets the DAC register to all zeros. This can be used to initialize the device on power up or during software calibration routines.

Low power consumption, +5V operation, and multiplying capability make the AD7542 suitable for numerous high precision processor controlled DAC applications. The AD7542 is supplied in 16-lead DIP and Small Outline packages.

Applications

Programmable Power Sources
Portable Test Equipment
Digitally Controlled Filters
Auto-Calibration Circuitry
Motion Control Systems

Functional Diagram



Features

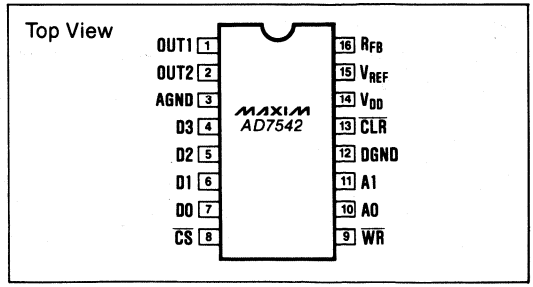
- 12-Bit Resolution
- ±1/2 LSB Linearity Over Temperature
- ±1 LSB Gain Accuracy (AD7542G)
- 5ppm/°C Max. Gain Drift
- Microprocessor Compatible
- 40mW Max. Power Dissipation
- +5V Operation

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7542JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7542KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7542GKN	0°C to +70°C	Plastic DIP	±½ LSB
AD7542JCWE	0°C to +70°C	Small Outline	±1 LSB
AD7542KCWE	0°C to +70°C	Small Outline	±½ LSB
AD7542GKCWE	0°C to +70°C	Small Outline	±½ LSB
AD7542JC/D	0°C to +70°C	Dice	±1 LSB
AD7542AD	-25°C to +85°C	Ceramic	±1 LSB
AD7542BD	-25°C to +85°C	Ceramic	±½ LSB
AD7542GBD	-25°C to +85°C	Ceramic	±½ LSB
AD7542AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7542BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7542GBQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7542SD	-55°C to +125°C	Ceramic	±1 LSB
AD7542TD	-55°C to +125°C	Ceramic	±½ LSB
AD7542GTD	-55°C to +125°C	Ceramic	±½ LSB
AD7542SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7542TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7542GTQ	-55°C to +125°C	CERDIP**	±½ LSB

* *All devices — 16 lead packages*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages*

Pin Configuration



CMOS µP-Compatible 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 4-11, 13)
V_{PIN1}, V_{PIN2} to AGND ..... -0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V

Power Dissipation 450mW
(derate 6mW/°C above +70°C)
Operating Temperature Range
Commercial AD7542JN, KN, GKN ..... 0°C to +70°C
Industrial AD7542AD, BD, GBD,
AQ, BQ, GBQ ..... -25°C to +85°C
Military AD7542SD, TD, GTD,
SQ, TQ, GTQ ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				12			Bits
Non-Linearity		AD7542J/A/S AD7542K/B/T AD7542GK/GB/GT				±1 ±0.5 ±0.5	LSB
Differential Non-Linearity		AD7542J/A/S (Note 1) AD7542K/B/T (Note 2) AD7542GK/GB/GT (Note 2)				±2 ±1 ±1	LSB
Gain Error		AD7542J/K/A/B/S/T AD7542J/K/A/B AD7542S/T	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±12.3 ±13.5 ±14.5	LSB
		AD7542GK/GB/GT AD7542GK/GB AD7542GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±1 ±1 ±2	
Gain Temperature Coefficient ΔGain/ΔTemperature (Note 4)					2	5	ppm/°C
Power Supply Rejection	PSRR	V_{DD} = +4.75V to +5.25V	T_A = 25°C T_{MIN} to T_{MAX}			0.005 0.01	%/%V_{DD}
Output Leakage Current I_{OUT1}, I_{OUT2} (Note 3)		AD7542J/K/GK AD7542A/B/GB AD7542S/T/GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			1 10 10 200	nA
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling Time		To 1/2 LSB, Out1 Load = 100Ω				2	µs
Feedthrough Error		V_{REF} = ±10V 10kHz sine wave				2.5	mVpp
REFERENCE INPUT							
Input Resistance (pin 15)	R_{REF}			8	15	25	kΩ
ANALOG OUTPUT (Note 4)							
Output Capacitance	C_{OUT1} C_{OUT1} C_{OUT2} C_{OUT2}	DAC Register 0000 0000 0000 DAC Register 1111 1111 1111 DAC Register 1111 1111 1111 DAC Register 0000 0000 0000				75 260 75 260	pF

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Logic HIGH Voltage	V_{INH}		+3.0			V
Logic LOW Voltage	V_{INL}				+0.8	V
Logic Input Current	I_{IN}	0V or V_{DD}			1	µA
Input Capacitance (Note 4)	C_{IN}				8	pF
SWITCHING CHARACTERISTICS (see Figure 6) (Note 5)						
Write Pulse Width	t_{WR}	T_A = 25°C T_{MIN} to T_{MAX}	120 220			ns
Address-to-Write Hold Time	t_{AWH}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
Chip Select-to-Write Hold	t_{CWH}	T_A = 25°C T_{MIN} to T_{MAX}	50 100			ns
Minimum CLEAR Pulse Width	t_{CLR}	T_A = 25°C T_{MIN} to T_{MAX}	200 300			ns
BYTE LOADING						
Chip Select-to-WRITE Setup	t_{CWS}	T_A = 25°C T_{MIN} to T_{MAX}	60 130			ns
Address Valid-to-Write Setup	t_{AWS}	T_A = 25°C T_{MIN} to T_{MAX}	80 180			ns
Data Setup Time	t_{DS}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
Data Hold Time	t_{DH}	T_A = 25°C T_{MIN} to T_{MAX}	50 65			ns
DAC LOADING						
Chip Select-to-WRITE Setup	t_{CWS}	T_A = 25°C T_{MIN} to T_{MAX}	60 150			ns
Address valid-to-Write Setup	t_{AWS}	T_A = 25°C T_{MIN} to T_{MAX}	120 240			ns
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ± 5%	4.75		5.25	V
Supply Current	I_{DD}				2.5	mA

Note 1: Monotonic to 11 bits from T_{MIN} to T_{MAX}
Note 2: Monotonic to 12 bits from T_{MIN} to T_{MAX}
Note 3: I_{OUT1} tested with DAC register loaded to all 0's.
I_{OUT2} tested with DAC register loaded to all 1's.
Note 4: Guaranteed by design but not tested.
Note 5: Sample tested at +25°C to ensure compliance.

CMOS μP-Compatible 12-Bit DAC

Detailed Description

The basic AD7542 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 15kΩ and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 75pF to 260pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

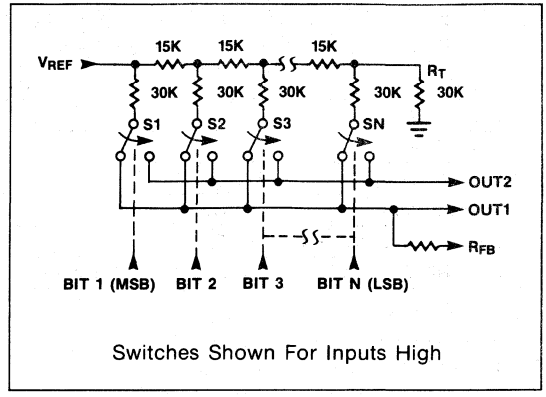


Figure 1. AD7542 Functional Diagram

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7542 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7542 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

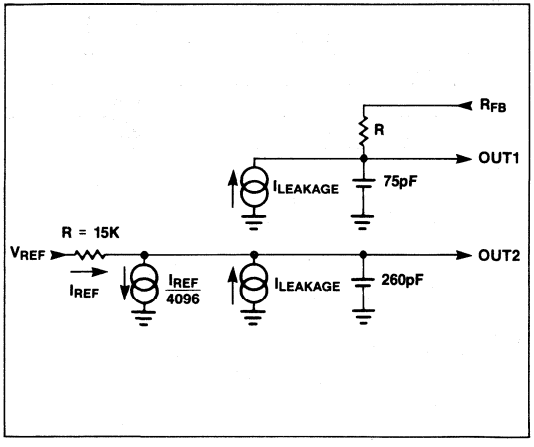


Figure 2. AD7542 DAC Equivalent Circuit, All Digital Inputs LOW

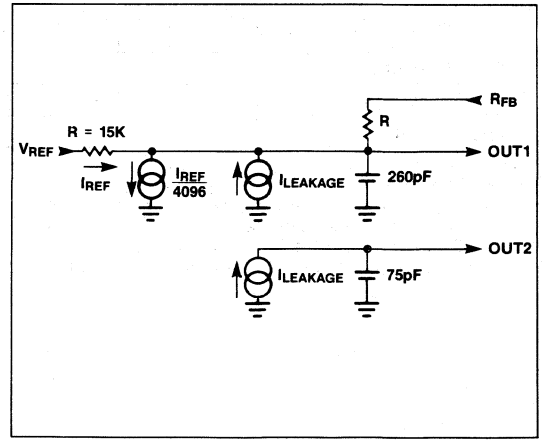
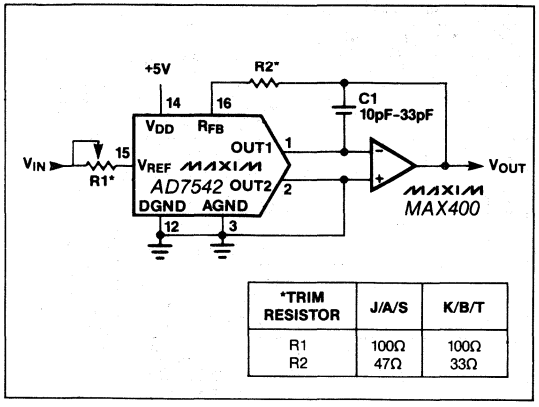


Figure 3. AD7542 DAC Equivalent Circuit, All Digital Inputs HIGH

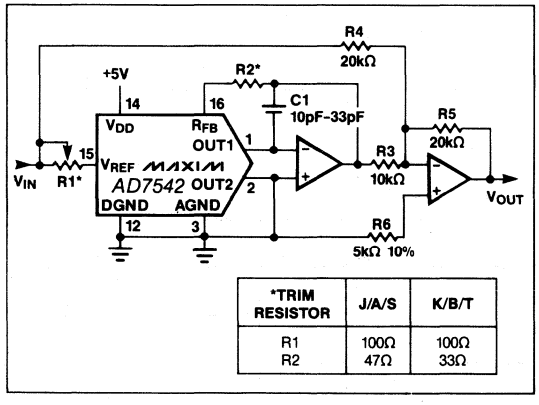


*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 4. Unipolar Binary Operation

Table 1. Code Table—Unipolar Binary

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V



*TRIM RESISTOR	J/A/S	K/B/T
R1	100Ω	100Ω
R2	47Ω	33Ω

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table—Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7542 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

CMOS µP-Compatible 12-Bit DAC

Interface Logic

Interface Logic Information

The AD7542 Truth Table is shown in Table 3. The high, middle and low byte, 4 bit data registers are loaded separately. The 12-bit DAC register is then loaded with the contents of the 3 data registers. The interface timing (Figure 6) is the same as writing to static RAM.

The CLR input asynchronously resets the 12-Bit DAC Register to Code 0000 0000 0000. In a unipolar mode the DAC output will be set to 0 volts. In the bipolar mode a CLR input resets the DAC output to $-V_{REF}$.

Notes:
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ⌐ indicates LOW to HIGH transition
5. MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB
6. These control signals are level triggered.

Table 3. AD7542 Truth Table

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	⌐	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At D_0-D_3
0	1	0	⌐	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	⌐	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⌐	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

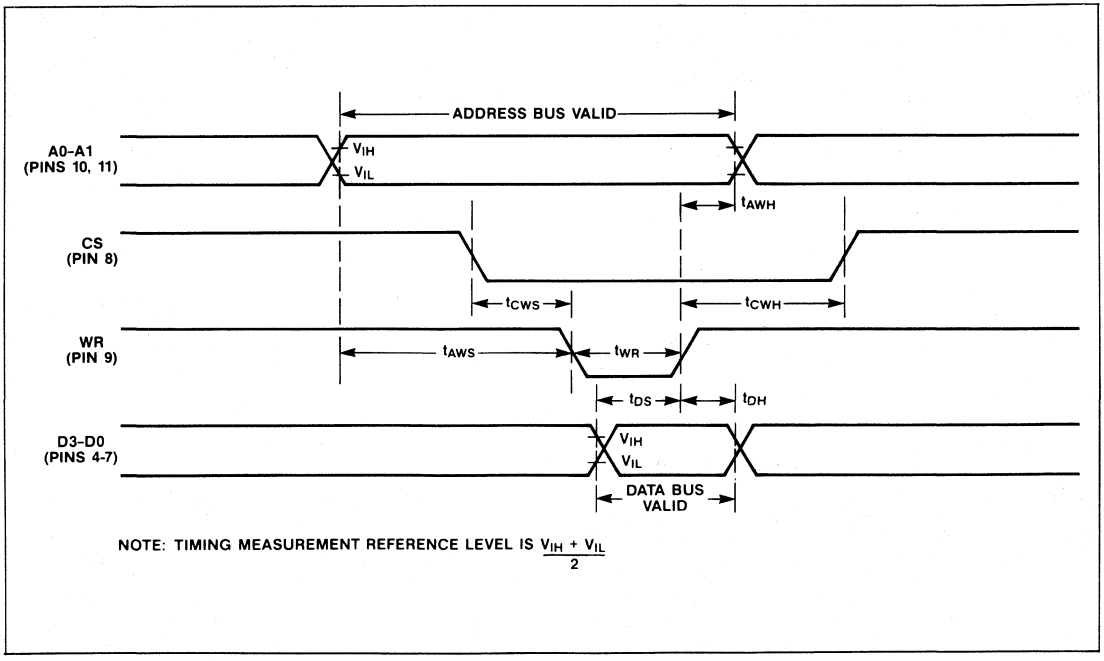


Figure 6. AD7542 Timing Diagram

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 15kΩ to 45kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error, I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensations

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

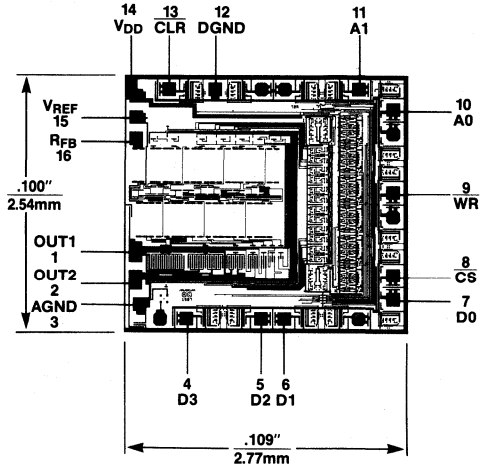
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting inputs are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1µF bypass capacitor, in parallel with a 0.01µF ceramic cap, should be connected as close to the DAC's V_{DD} and GND pins as possible.

The AD7542 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

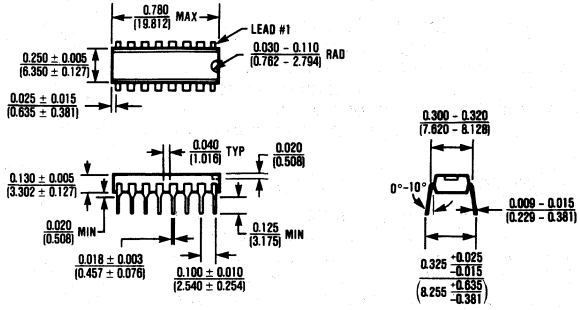
Chip Topography



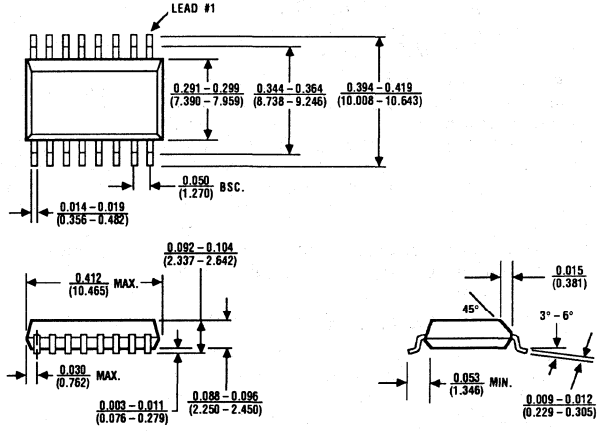
CMOS μP-Compatible 12-Bit DAC

Package Information

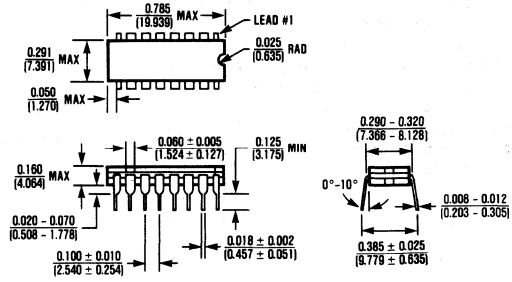
16 Lead Plastic DIP
θ_{JA} = 135°C/W
θ_{JC} = 65°C/W



16 Lead Small Outline, Wide (WE)
θ_{JA} = 105°C/W
θ_{JC} = 60° C/W



16 Lead CERDIP
θ_{JA} = 100°C/W
θ_{JC} = 50°C/W



MAXIM

CMOS Serial Input 12-Bit DAC

General Description

The AD7543 is a high precision 12-bit digital-to-analog converter (DAC) which uses a serial rather than parallel input scheme for loading data. Included are a serial-to-parallel shift register, a separate DAC register, and a multiplying DAC.

Serial data is clocked in at the SRI pin on the rising or falling edge (user selected) of the strobe input. When the input register is full, the contents are transferred to the DAC register using the load input. A clear input is provided to initialize the part asynchronously.

The AD7543 features excellent gain stability (5ppm/°C max.) and operates from a single +5V power supply while dissipating about 10mW.

Applications

Remote Analog Systems

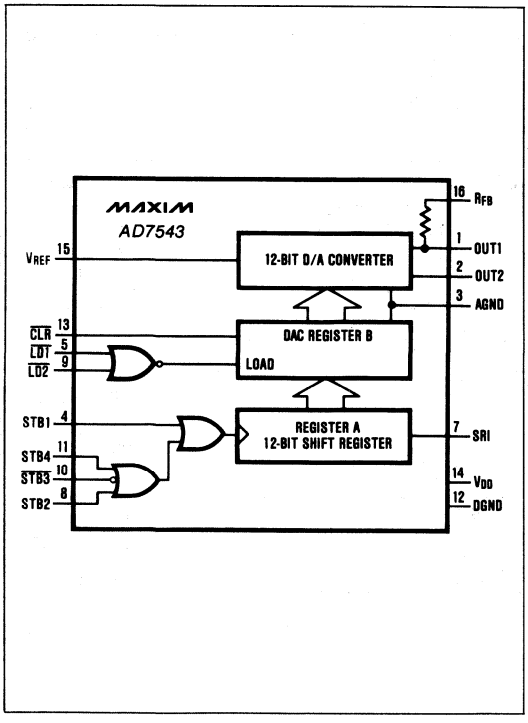
Robotics

Programmable Attenuators

Automatic Test Equipment

Auto-Calibration Systems

Functional Diagram



Features

- Serial Interface
- ±½ and ±1 LSB Linearity
- CLEAR Input For Initialization
- Single +5V Supply Operation
- 5ppm/°C Gain Stability
- 1 LSB Max. Feedthrough At 10kHz
- Small Size: 16-Lead DIP

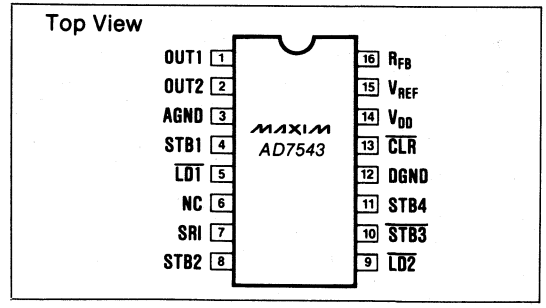
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7543JN	0°C to +70°C	Plastic DIP	±1 LSB
AD7543KN	0°C to +70°C	Plastic DIP	±½ LSB
AD7543GKN	0°C to +70°C	Plastic DIP	±½ LSB
AD7543JCWE	0°C to +70°C	Small Outline	±1 LSB
AD7543KCWE	0°C to +70°C	Small Outline	±½ LSB
AD7543GKCWE	0°C to +70°C	Small Outline	±½ LSB
AD7543JC/D	0°C to +70°C	Dice	±1 LSB
AD7543AD	-25°C to +85°C	Ceramic	±1 LSB
AD7543BD	-25°C to +85°C	Ceramic	±½ LSB
AD7543GBD	-25°C to +85°C	Ceramic	±½ LSB
AD7543AQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7543BQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7543GBQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7543SD	-55°C to +125°C	Ceramic	±1 LSB
AD7543TD	-55°C to +125°C	Ceramic	±½ LSB
AD7543GTD	-55°C to +125°C	Ceramic	±½ LSB
AD7543SQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7543TQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7543GTQ	-55°C to +125°C	CERDIP**	±½ LSB

** All devices—16-pin packages*

*** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration



CMOS Serial Input 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 4-11, 13)
V_{PIN1}, V_{PIN2} to AGND ..... -0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... ±25V
V_{RFB} to AGND ..... ±25V

Power Dissipation 450mW
(derate 6mW/°C above +70°C)
Operating Temperature Range
Commercial AD7543JN, KN, GKN ..... 0°C to +70°C
Industrial AD7543AD, BD, GBD,
AQ, BQ, GBQ ..... -25°C to +85°C
Military AD7543SD, TD, GTD,
SQ, TQ, GTQ ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				12			Bits
Non-Linearity		AD7543J/A/S AD7543K/B/T AD7543GK/GB/GT				±1 ±0.5 ±0.5	LSB
Differential Non-Linearity		AD7543J/A/S (Note 1) AD7543K/B/T (Note 2) AD7543GK/GB/GT (Note 2)				±2 ±1 ±1	LSB
Gain Error		AD7543J/K/A/B/S/T AD7543J/K/A/B AD7543S/T	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±12.3 ±13.5 ±14.5	LSB
		AD7543GK/GB/GT AD7543GK/GB AD7543GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			±1 ±1 ±2	
Gain Temperature Coefficient ΔGain/ΔTemperature (Note 4)					2	5	ppm/°C
Power Supply Rejection	PSRR	V_{DD} = +4.75V to +5.25V	T_A = 25°C T_{MIN} to T_{MAX}			0.005 0.01	%/%V_{DD}
Output Leakage Current I_{OUT1}, I_{OUT2} (Note 3)		AD7543J/K/GK AD7543A/B/GB AD7543S/T/GT	T_A = 25°C T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}			1 10 10 200	nA
DYNAMIC PERFORMANCE (Note 4)							
Output Current Settling Time		To 1/2 LSB, Out1 Load = 100Ω				2	μs
Feedthrough Error		V_{REF} = ±10V 10kHz sine wave				2.5	mVpp
REFERENCE INPUT							
Input Resistance (pin 15)	R_{REF}			8	15	25	kΩ
ANALOG OUTPUT (Note 4)							
Output Capacitance	C_{OUT1} C_{OUT1} C_{OUT2} C_{OUT2}	DAC Register 0000 0000 0000 DAC Register 1111 1111 1111 DAC Register 1111 1111 1111 DAC Register 0000 0000 0000				75 260 75 260	pF

Note 1: Monotonic to 11 bits from T_{MIN} to T_{MAX}
Note 2: Monotonic to 12 bits from T_{MIN} to T_{MAX}
Note 3: I_{OUT1} tested with DAC register loaded to all 0's.
I_{OUT2} tested with DAC register loaded to all 1's.
Note 4: Guaranteed by design but not tested.
Note 5: Sample tested at +25°C to ensure compliance.

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Logic HIGH Voltage	V_{INH}		+3.0			V
Logic LOW Voltage	V_{INL}				+0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			1	μA
Input Capacitance (Note 4)	C_{IN}				8	pF
SWITCHING CHARACTERISTICS (see Figure 6) (Note 5)						
Serial Input to Strobe Setup Time	t_{DS1}	T_A = 25°C T_{MIN} to T_{MAX}	50 100			ns
	t_{DS2}	T_A = 25°C T_{MIN} to T_{MAX}	20 40			ns
	t_{DS3}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
	t_{DS4}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
Serial Input to Strobe Hold Time	t_{DH1}	T_A = 25°C T_{MIN} to T_{MAX}	30 60			ns
	t_{DH2}	T_A = 25°C T_{MIN} to T_{MAX}	60 120			ns
	t_{DH3}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
	t_{DH4}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
SRI data pulse width	t_{SRI}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
STB1 pulse width	t_{STB1}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
STB2 pulse width	t_{STB2}	T_A = 25°C T_{MIN} to T_{MAX}	80 160			ns
$\overline{STB3}$ pulse width	t_{STB3}	T_A = 25°C T_{MIN} to T_{MAX}	100 200			ns
STB4 pulse width	t_{STB4}	T_A = 25°C T_{MIN} to T_{MAX}	100 200			ns
Load 1 pulse width	t_{LD1}	T_A = 25°C T_{MIN} to T_{MAX}	150 300			ns
Load 2 pulse width	t_{LD2}	T_A = 25°C T_{MIN} to T_{MAX}	150 300			ns
Time between strobing LSB into Register A and loading Register B	t_{ASB}	T_A = 25°C T_{MIN} to T_{MAX}	0 0			ns
Clear pulse width	t_{CLR}	T_A = 25°C T_{MIN} to T_{MAX}	200 400			ns
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ± 5%	4.75		5.25	V
Supply Current	I_{DD}				2.5	mA

CMOS Serial Input 12-Bit DAC

Detailed Description

The basic AD7543 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Although the current at OUT1 or OUT2 will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF} minus the termination resistor current (R_T).

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 4). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 15kΩ and does not change with digital input code. The $I_{REF}/4096$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors C_{OUT1} and C_{OUT2} represent the switches ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from approximately 75pF to 260pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

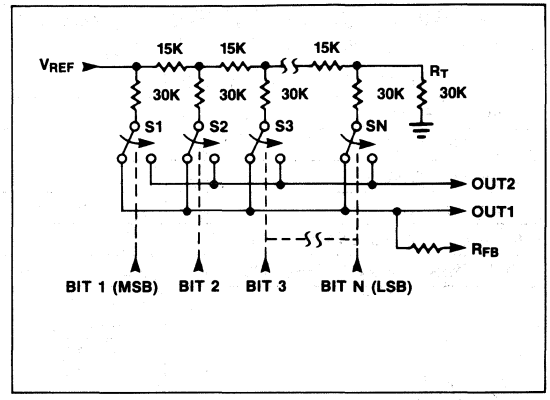


Figure 1. AD7543 Functional Diagram

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7543 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. The code table is given in Table 1. Note that the polarity of the output is the inverse of the reference input.

In many applications, gain adjustment of the AD7543 will not be necessary. In those cases, and also when gain is trimmed but only at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However, if the trims are desired and the DAC is to operate over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used at R1 and R2.

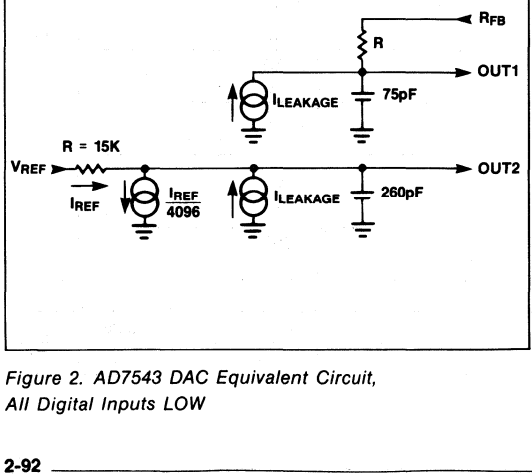


Figure 2. AD7543 DAC Equivalent Circuit, All Digital Inputs LOW

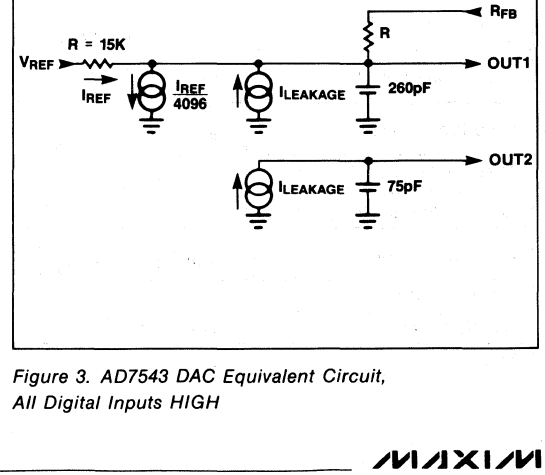
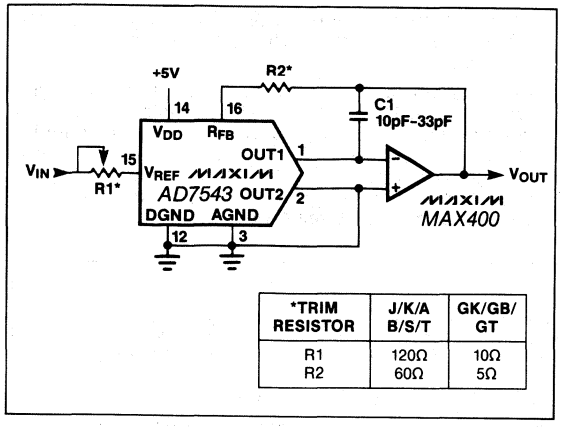


Figure 3. AD7543 DAC Equivalent Circuit, All Digital Inputs HIGH

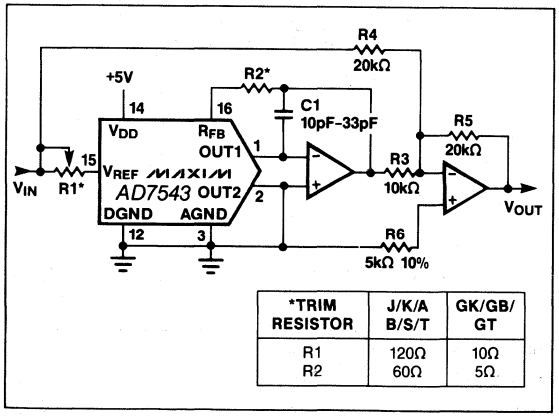


*TRIM RESISTOR	J/K/A B/S/T	GK/GB/ GT
R1	120Ω	10Ω
R2	60Ω	5Ω

Figure 4. Unipolar Binary Operation

Table 1. Code Table—Unipolar Binary

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0V



*TRIM RESISTOR	J/K/A B/S/T	GK/GB/ GT
R1	120Ω	10Ω
R2	60Ω	5Ω

Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 2. Code Table— Bipolar (Offset Binary) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0V
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Bipolar Operation

With the circuit configuration in Figure 5, the AD7543 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors are required. Matching to 0.01% is recommended for 12 bit performance. The code table for the output, which is "offset binary", is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. If gain and offset trims are not required, R1 and R2 in Figure 5 can be omitted.

CMOS Serial Input 12-Bit DAC

Interface Logic

Serial data is first loaded into the 12-bit Shift Register A, shown in the AD7543 functional diagram. Each bit of serial data appearing at pin SRI is clocked into Register A MSB first, by any one of the four strobe inputs. STB1, STB2, and STB4 all clock data into Shift Register A on the rising edge of the strobe pulse. $\overline{STB3}$ clocks data into Register A on its falling edge. Table 3 illustrates the logic states for the control inputs. Figure 6 shows the timing diagram for the loading sequence.

Data is then transferred from Shift Register A into Register B by momentarily moving both LD1 and LD2, low.

Bringing $\overline{CLR}$ input low asynchronously resets Register B to 0000 0000 0000. This initializes the DAC output voltage to a known condition. With the unipolar circuit of Figure 4, a $\overline{CLR}$ results in a DAC output voltage of 0 volts. Using the bipolar circuit of Figure 5, momentarily bringing $\overline{CLR}$ low sets the DAC output voltage to its lowest value of $-V_{REF}$.

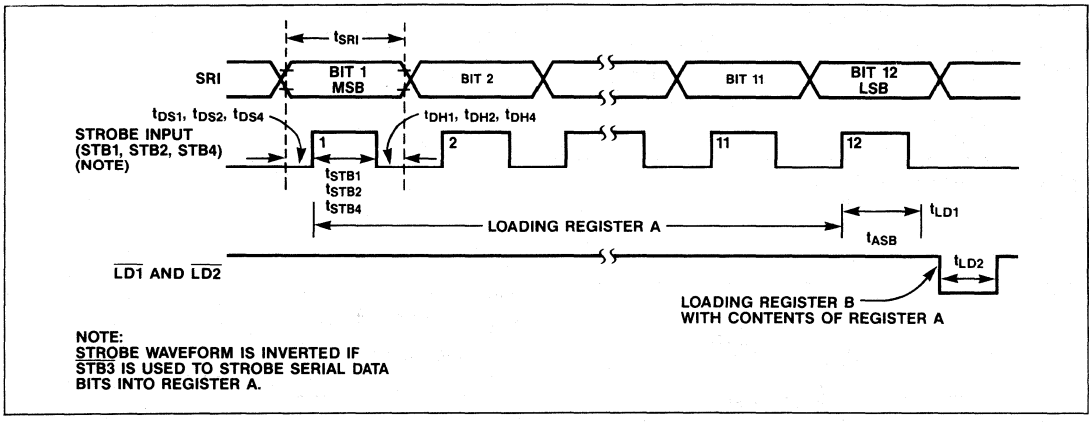


Figure 6. Timing Diagram

Table 3. AD7543 Truth Table

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↓	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
0	1	↓	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
0	↓	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
↓	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2, 3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

Notes:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↓ is positive edge ↓ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Application Information

Output Amplifier Offset

For best linearity, OUT1 and OUT2 should be terminated exactly at 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The amplifier's input offset voltage can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB}/R_O),$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 15kΩ to 45kΩ. The error voltage range is then typically $4/3V_{OS}$ to $2V_{OS}$, a change of $2/3V_{OS}$. An amplifier with 3mV of offset will therefore degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 of an LSB's value.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error, I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a "bias current compensation resistor". This resistor adds to offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op-amp used but typical values range from 10 to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at OUT1 as small as possible.

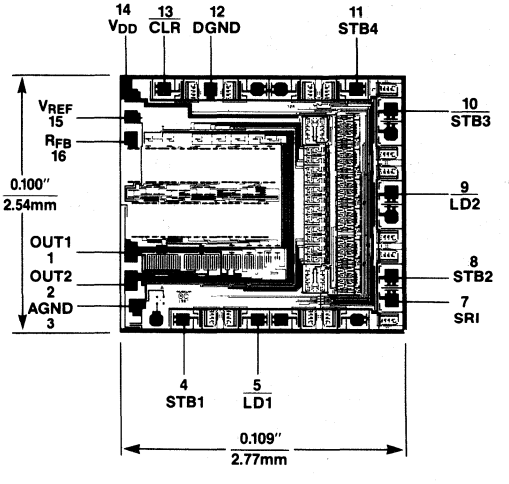
Grounding and Bypassing

Since OUT1, OUT2 and the output amp's noninverting inputs are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, very low resistance (less than 0.2Ω) path. The current at OUT1 and OUT2 varies with input code, creating a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC's V_{DD} and GND pins as possible.

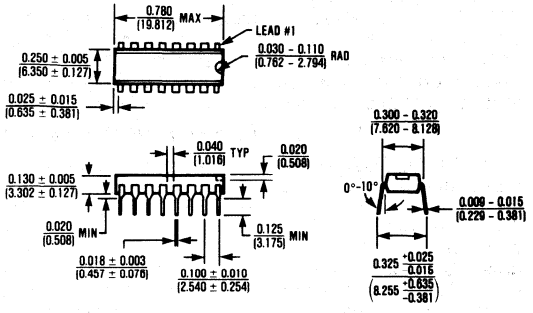
The AD7543 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

Chip Topography

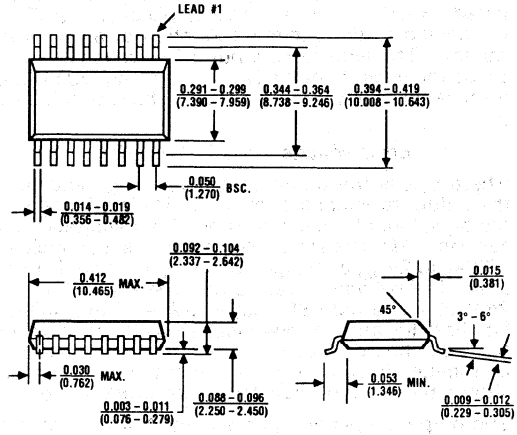


CMOS Serial Input 12-Bit DAC

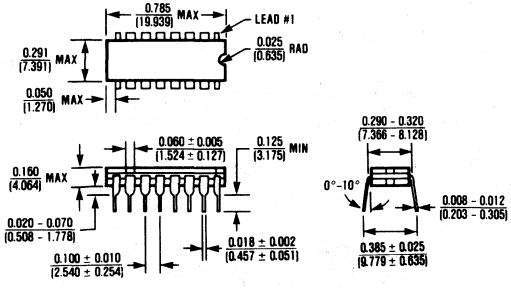
Package Information



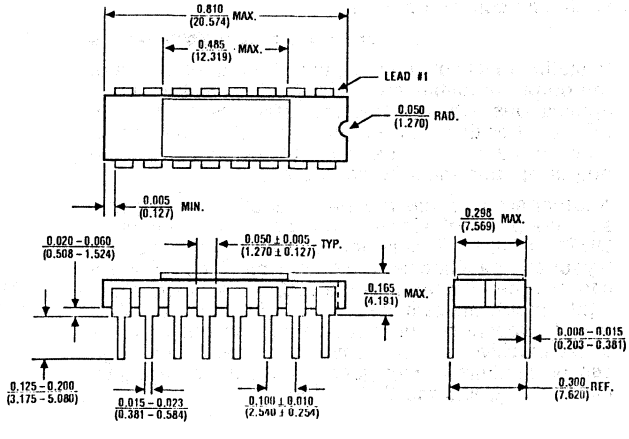
16 Lead Plastic DIP
θ_{JA} = 135°C/W
θ_{JC} = 65°C/W



16 Lead Small Outline, Wide (WE)
θ_{JA} = 105°C/W
θ_{JC} = 60° C/W



16 Lead CERDIP
θ_{JA} = 100°C/W
θ_{JC} = 50°C/W



16 Lead Ceramic Sidebraze
θ_{JA} = 95°C/W
θ_{JC} = 45°C/W

CMOS 12-Bit Buffered Multiplying DAC

General Description

The AD7545 is a 12-bit CMOS multiplying digital-to-analog converter (DAC) with internal data latches. Input data is loaded as a single 12-bit word and latched under the control of CS and WR inputs. When CS and WR are low, the input data latches are transparent and the DAC output responds to any changes in the digital input.

AD7545 works with a single +5V or +15V power supply. Electrical characteristics are specified at both of these supply voltages. With a +5V supply, the digital inputs are +5V TTL and CMOS compatible while high voltage CMOS compatibility is maintained at +15V supply range.

Maxim AD7545 uses low tempco thin-film resistors which are laser-trimmed to result in linearity errors that are typically ±¼ LSB and gain errors of maximum ±1 LSB (G grade).

The digital inputs are designed with improved protection against electrostatic discharge (ESD) damage and can typically withstand to over 6,000V of ESD voltages.

The AD7545 is supplied in 20-lead narrow DIP and Small Outline packages.

Applications

Motion Control Systems

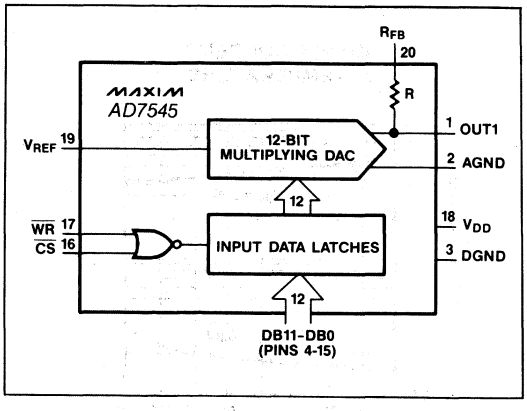
Automatic Test Equipment

μP Controlled Calibration Circuitry

Programmable Gain Amplifiers

Programmable Power Supplies

Functional Diagram



Features

- 12-Bit Resolution
- ±1 LSB Gain Accuracy (G Grade)
- Single Supply Operation
- Improved ESD Protection
- CMOS/TTL Compatible for V_{DD} = +5V
- CMOS Compatible for V_{DD} = +15V

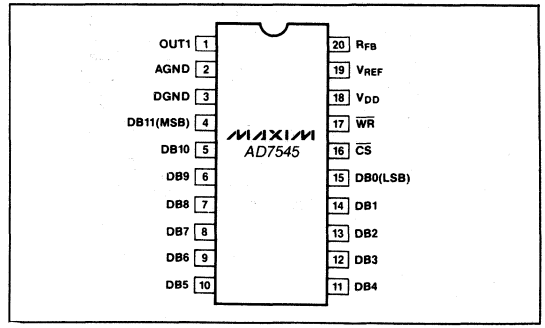
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
AD7545JN	0°C to +70°C	Plastic DIP	±2 LSB
AD7545KN	0°C to +70°C	Plastic DIP	±1 LSB
AD7545LN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545GLN	0°C to +70°C	Plastic DIP	±½ LSB
AD7545JCWP	0°C to +70°C	Small Outline	±2 LSB
AD7545KCWP	0°C to +70°C	Small Outline	±1 LSB
AD7545LCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545GLCWP	0°C to +70°C	Small Outline	±½ LSB
AD7545JC/D	0°C to +70°C	Dice	±2 LSB
AD7545AQ	-25°C to +85°C	CERDIP**	±2 LSB
AD7545BQ	-25°C to +85°C	CERDIP**	±1 LSB
AD7545CQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545GCQ	-25°C to +85°C	CERDIP**	±½ LSB
AD7545SD	-55°C to +125°C	Ceramic	±2 LSB
AD7545TD	-55°C to +125°C	Ceramic	±1 LSB
AD7545UD	-55°C to +125°C	Ceramic	±½ LSB
AD7545GUD	-55°C to +125°C	Ceramic	±½ LSB
AD7545SQ	-55°C to +125°C	CERDIP**	±2 LSB
AD7545TQ	-55°C to +125°C	CERDIP**	±1 LSB
AD7545UQ	-55°C to +125°C	CERDIP**	±½ LSB
AD7545GUQ	-55°C to +125°C	CERDIP**	±½ LSB

** All devices—20 lead packages*

***Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration



CMOS 12-Bit Buffered Multiplying DAC

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise stated.)

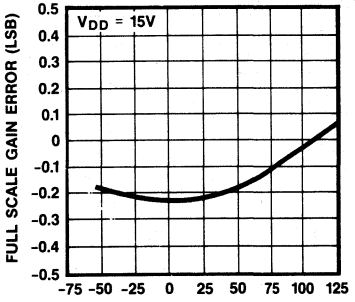
V_{DD} to DGND ..... -0.3 to +17V
Digital Input Voltage to DGND ..... -0.3 to V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
V_{OUT1} to DGND ..... -0.3 to V_{DD}
AGND to DGND ..... -0.3 to V_{DD}
Power dissipation to +75°C (any package) 450mW
Derate above 75°C by ..... 6mW/°C

Operating Temperature Ranges
JN, KN, LN, GLN ..... 0°C to +70°C
AQ, BQ, CQ, GCQ ..... -25°C to +85°C
SD, TD, UD, GUD ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

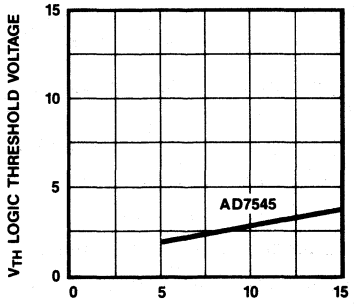
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

Typical Performance Characteristics

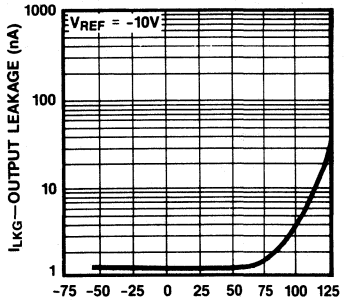
FULL-SCALE GAIN ERROR vs TEMPERATURE



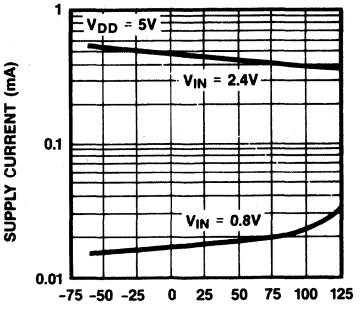
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N						12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU				±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU				±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T				±20 ±10	LSB LSB
			L,C,U	T_A = +25°C Over Temp.			±5 ±6	LSB LSB
			GL,GC,GU	T_A = +25°C Over Temp.			±1 ±2	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS					±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%		T_A = +25°C Over Temp.			0.015 0.03	%/% %/%
DYNAMIC PERFORMANCE								
Current Settling Time (Note 2)	t_S	To ±1/2 LSB. OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.					2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 load is: R = 100ohms/C = 13pF.		T_A = +25°C			300	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND		T_A = +25°C		400		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.				5		mVp-p
REFERENCE INPUT								
Input Resistance	R_{REF}	V_{REF} pin to AGND			7	11	25	kohms
Input Resistance Tempco	TCR					-300		ppm/°C

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

CMOS 12-Bit Buffered Multiplying DAC

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					70 200	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C Over Temp.			10 50	nA nA
			A,B,C,GC	T_A = +25°C Over Temp.			10 50	nA nA
			S,T,U,GU	T_A = +25°C Over Temp.			10 200	nA nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				2.4			V
Input Low Voltage	V_{IL}						0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}		T_A = +25°C Over Temp.		±0.001	±1 ±10	μA μA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0 V_{IN} = 0V; $\overline{WR}$, $\overline{CS}$					5 20	pF pF
SWITCHING CHARACTERISTICS (Notes 4, 5)								
Chip Select to Write Setup Time	t_{CS}			T_A = +25°C Over Temp.	280 380	200 270		ns ns
Chip Select to Write Hold Time	t_{CH}				0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$		T_A = +25°C Over Temp.	250 400	175 280		ns ns
Data Setup Time	t_{DS}			T_A = +25°C Over Temp.	140 210	100 150		ns ns
Data Hold Time	t_{DH}				10			ns
POWER SUPPLY								
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} : 0V or V_{DD}, : 0V or V_{DD}		T_A = +25°C Over Temp.		10 10	2 100 500	mA μA μA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N						12	Bits
Relative Accuracy	INL		J,A,S K,B,T L,C,U GL,GC,GU				±2 ±1 ±1/2 ±1/2	LSB LSB LSB LSB
Differential Non-Linearity	DNL	10-bit Monotonic 12-bit Monotonic 12-bit Monotonic 12-bit Monotonic	J,A,S K,B,T L,C,U GL,GC,GU				±4 ±1 ±1 ±1	LSB LSB LSB LSB
Gain Error (Note 1)	FSE		J,A,S K,B,T L,C,U				±25 ±15 ±10	LSB LSB LSB
			GL,GC,GU	T_A = +25°C Over Temp.			±6 ±7	LSB LSB
Gain Tempco ΔGain/ΔTemp. (Note 2)	TCFS					±2	±10	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 2)	PSR	ΔV_{DD} = ±5%		T_A = +25°C Over Temp.			0.01 0.02	%/% %/%
DYNAMIC PERFORMANCE								
Current Settling Time (Note 2)	t_S	To ±1/2 LSB OUT1 Load is 100ohms. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.					2	μs
Propagation Delay (Note 2)	t_{PD}	From digital inputs, DB11-DB0, change from V_{DD} to 0V or 0V to V_{DD}, to 90% of final analog output. OUT1 Load is: R = 100ohms/C = 13pF.		T_A = +25°C			250	ns
Digital to Analog Glitch Impulse	Q	V_{REF} = AGND		T_A = +25°C		250		nV-s
AC Feedthrough at OUT1 (Note 3)	FTE	V_{REF} = ±10V, 10kHz sinewave, DB11-DB0 = 0V.				5		mVp-p
REFERENCE INPUT								
Input Resistance	R_{REF}	V_{REF} pin to AGND			7	11	25	kohms
Input Resistance Tempco	TCR					-300		ppm/°C
ANALOG OUTPUTS								
OUT1 Capacitance (Note 2)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V					70 200	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	J,K,L,GL	T_A = +25°C Over Temp.			10 50	nA nA
			A,B,C,GC	T_A = +25°C Over Temp.			10 50	nA nA
			S,T,U,GU	T_A = +25°C Over Temp.			10 200	nA nA
DIGITAL INPUTS								
Input High Voltage	V_{IH}				13.5			V
Input Low Voltage	V_{IL}						1.5	V

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ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND. Over specified temperature range unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Continued)							
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C Over Temp.		±0.001	±1 ±10	µA µA
Input Capacitance (Note 2)	C_{IN}	V_{IN} = 0V; DB11-DB0 V_{IN} = 0V; $\overline{WR}$, $\overline{CS}$				5 20	pF pF
SWITCHING CHARACTERISTICS (Notes 4, 5)							
Chip Select to Write Setup Time	t_{CS}		T_A = +25°C Over Temp.	180 200	120 150		ns ns
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	T_A = +25°C Over Temp.	160 240	100 170		ns ns
Data Setup Time	t_{DS}		T_A = +25°C Over Temp.	90 120	60 80		ns ns
Data Hold Time	t_{DH}			10			ns
POWER SUPPLY							
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} : 0V or V_{DD}, : 0V or V_{DD}	T_A = +25°C Over Temp.		10 10	2 100 500	mA µA µA

Note 1: Using internal feedback resistor, RFB. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 3, 4 and 8.
Note 2: Guaranteed by design but not tested.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: Sample tested at 25°C to ensure compliance.
Note 5: See timing diagram for definitions of the switching times.

Detailed Description

D/A Converter

The basic AD7545 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or AGND depending on the status of each input bit. Although the current at OUT1 and AGND will depend on the digital input code, the sum of the two output currents is always equal to the input current at V_{REF}.

Either current output can be converted into a voltage externally by adding an output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low temperature coefficient external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT1} pin output capacitance, C_{OUT1}, is code dependent and is typically 70pF to 200pF, with all switches to AGND and I_{OUT1}, respectively.

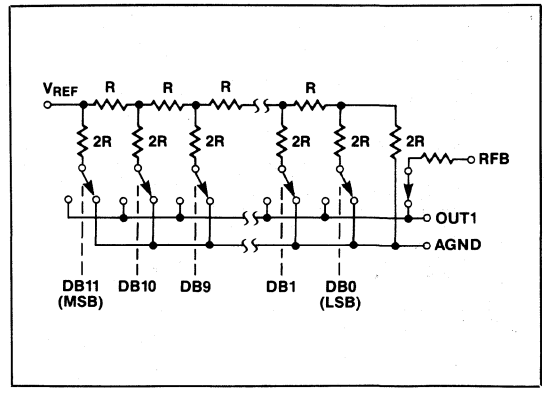


Figure 1. Simplified D/A Circuit of AD7545

Digital Circuit

The digital circuit for one bit is shown in Figure 2. The digital CONTROL signal is HIGH when $\overline{WR}$ and $\overline{CS}$ are both low. When $\overline{WR}$ and $\overline{CS}$ are tied low, the digital input directly controls the D/A switches.

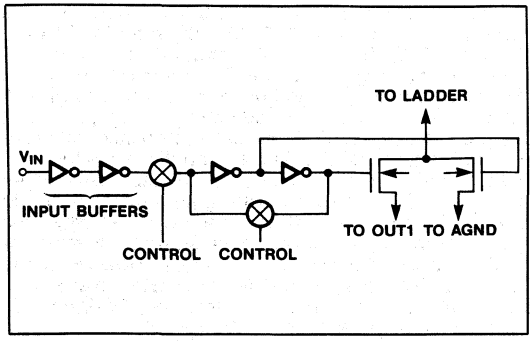
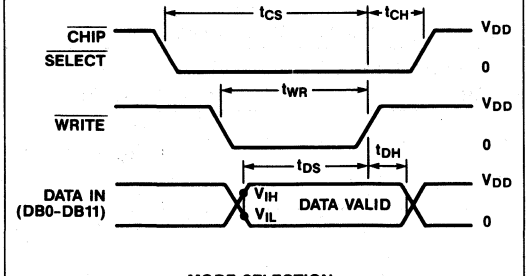


Figure 2. Digital Input Structure

The input buffer inverters act as a level shifter converting TTL levels into CMOS logic levels. These input buffers are CMOS/TTL compatible (0.8V and 2.4V) at V_{DD} = +5V. The AD7545 also works with V_{DD} = +15V where the input buffers are CMOS compatible (1.5V and 13.5V) only. With the digital input voltages at 1V to 6V the input buffers work in their linear regions drawing current from the power supply. Therefore to minimize high supply currents the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and DGND) as possible.

All digital inputs are ruggedized against electrostatic-discharge (ESD) sensitivity and can typically withstand ESD voltages of over 6kV.



MODE SELECTION

WRITE MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.

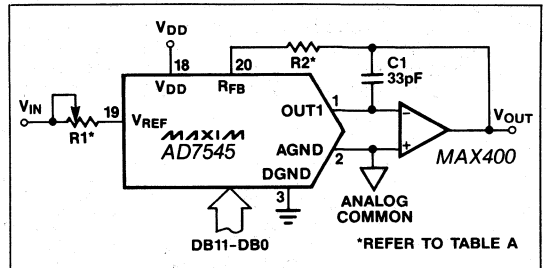
HOLD MODE:
Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V, $t_r = t_f$ = 20ns
V_{DD} = +15V, $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Circuit Configurations

Unipolar Operation

The most common configuration for the AD7545 is shown in Figure 3. This circuit is used for unipolar binary operation or two-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.



TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

TABLE A. RECOMMENDED TRIM RESISTOR VALUES vs. GRADES FOR V_{DD} = +5V

Figure 3. Unipolar Binary Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 3 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

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The capacitor C1 provides phase compensation and helps reduce the overshoot and ringing when using fast amplifiers at the output of the DACs.

Bipolar Operation

With the circuit configuration shown in Figure 4, the AD7545 operates in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors, R3, R4 and R5 are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature characteristics, and they should match to 0.01% for 12-bit performance.

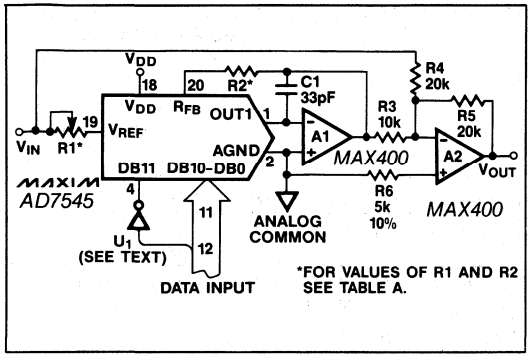


Figure 4. Bipolar Operation (2's Complement Code)

Table 2. 2's Complement Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{2048}\right)$

The code table for the output, which is 2's complement is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude. The U1 inverter on the MSB line converts the 2's complement input code to offset-binary code. If this inversion is done in software using an exclusive-OR instruction or the input code is in offset binary, the U1 inverter can be omitted. Table 3 shows the code relationships to output voltage for the offset binary operation.

To adjust the circuit with offset binary code, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using the "G" suffix parts with guaranteed maximum ±1 LSB gain errors. In those cases and also when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 4 can be omitted. However,if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

(Voltage Mode) Single Supply

The AD7545 can be conveniently used in single supply (voltage mode) operation with OUT1 and AGND biased at any voltage between DGND and V_{DD}. This is possible since the ladder termination resistor is connected to AGND. OUT1 and AGND must not be allowed to go 0.3V lower or higher than the DGND or V_{DD}, respectively. Otherwise, internal diodes would turn on and a heavy current flow from the supply, possibly destroying the device.

Figure 5 shows the AD7545 connected as a voltage output DAC. OUT1 is connected to the reference input and AGND is grounded. V_{REF} pin, now the DAC output, is a voltage source with a constant impedance equal to the reference input resistance (typically 11kohms). This output should be buffered with an op-amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

Table 3. Offset Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

The input impedance of the reference input (OUT1) for this mode is code dependent, and the response time of the circuit depends on the behaviour of the reference source with changing load conditions.

Two advantages of the voltage mode operation are

single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (the voltage at OUT1) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded linearity and differential nonlinearity (DNL). Figures 6 and 7 show the typical dependence of DNL on supply voltage, V_{DD}, and the reference voltage, V_{REF}. If the DAC is offset from DGND by biasing OUT1 and AGND at a voltage above DGND, this will effect DNL and its effect will be the same as reducing V_{DD} by the amount of the offset.

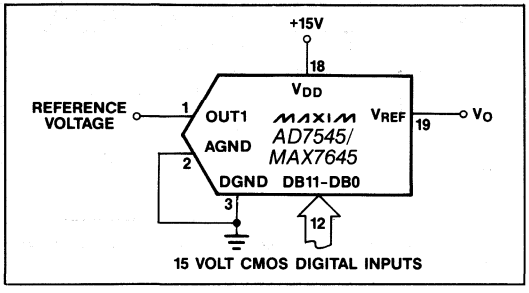


Figure 5. Single Supply Operating Using Voltage Switching Mode

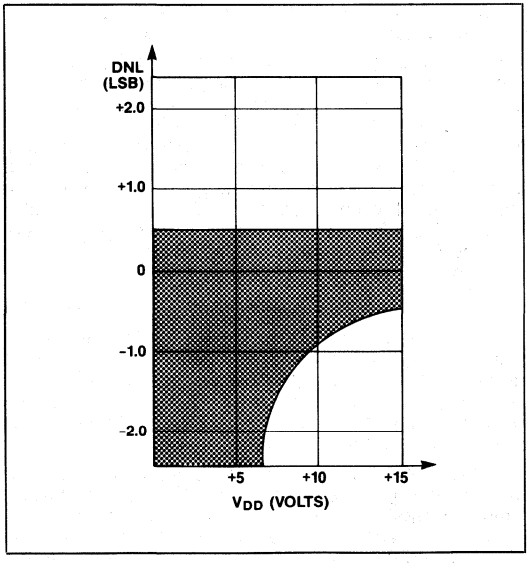


Figure 6. Differential Nonlinearity vs. V_{DD} for Figure 4 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode. For example, Figure 8 shows the 2's complement bipolar circuit of Figure 4 modified to work with an output range of +2V to +8V around an offset ground potential of +5V from a single supply, V_{DD}, of +10V to 15V. The REF02 reference is used to bias the AGND at +5V. The R1 and R2 resistors form a voltage divider together

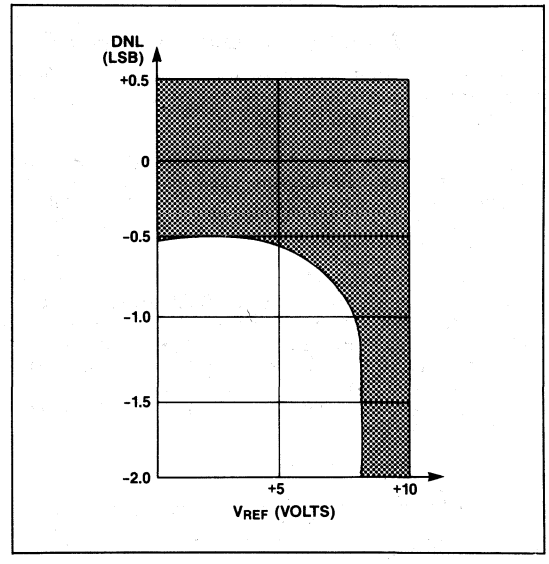


Figure 7. Differential Nonlinearity vs. Reference Voltage for Figure 4 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

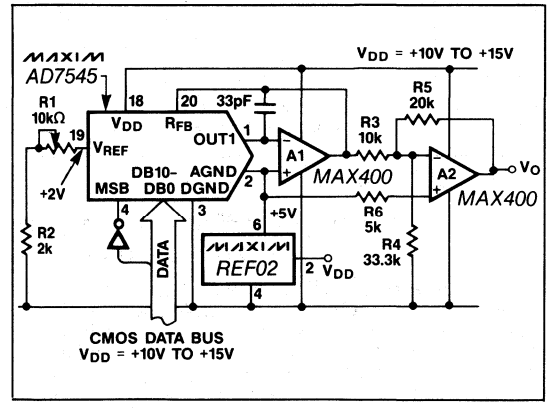


Figure 8. Single Supply "Bipolar" 2's Complement D/A Converter

CMOS 12-Bit Buffered Multiplying DAC

with the DAC reference input resistor, supplying the DAC with +2V input voltage. If the application requires a wide temperature range, the +2V should be generated with an op-amp to avoid drifts due to tempco matching of the DAC resistors to the external resistors. Output voltage ranges can be produced by changing R4 to change the offset, and (R1 + R2) to change the gain (slope) of the DAC transfer function. To ensure good linearity, the supply voltage, V_{DD}, must be kept at least +5V above the OUT1 voltage.

Microprocessor Interfacing

The AD7545 directly interfaces to 8- and 16-bit microprocessors using standard WR and $\overline{CS}$ control signals and its 12-bit data latch.

Figure 9 shows a typical interface circuit for an 8-bit processor. This application uses two memory addresses for the lower 8 bits and the upper 4 bits of data to the DAC. A 4-bit external latch is required to facilitate the interface.

For processors with 16-bit wide address busses and 8-bit data busses, such as 6800, 8080 and Z80, the 12 lower address lines can be used to supply data to the DAC, as shown in Figure 10. The upper 4 bits contain the address of the DAC that is selected. This arrangement takes 4k bytes of address locations for each DAC and the data is written with a single instruction cycle into the DAC.

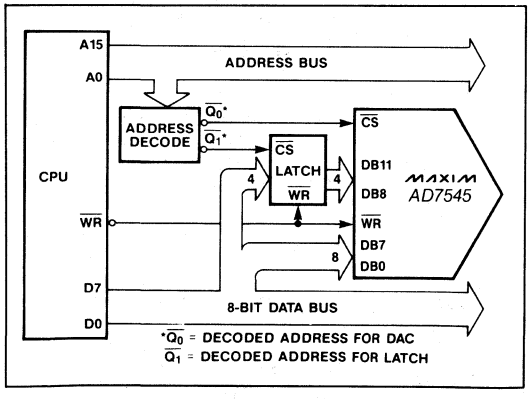


Figure 9. 8-Bit Processor to AD7545 Interface

Application Information

Output Amplifier Offset

For best linearity, OUT1 and AGND should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op-amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R_O)$$

where V_{OS} is the op-amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code and varies from approximately 11kohms to 33kohms. The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS}, a change of 2/3 V_{OS}. An amplifier with 3mV of offset will therefore degrade the

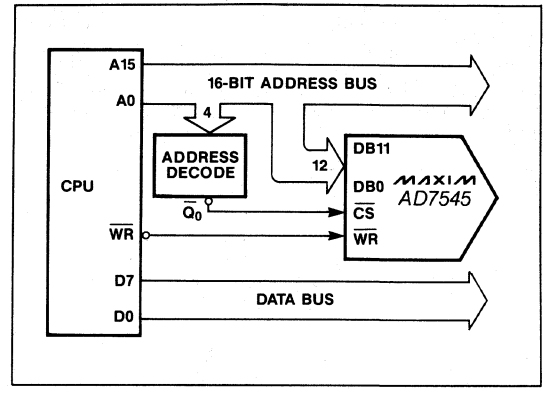


Figure 10. Connecting the AD7545 to 8-Bit Processors via the Address Bus

linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 LSBs.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1 LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor". This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to OUT1. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs V_{REF} and OUT1 pins.

The DAC output follows the digital inputs when the $\overline{WR}$ and $\overline{CS}$ pins are low. In those systems where the data is not valid for the full period where $\overline{WR}$ is low, invalid outputs and voltage glitches can appear at the DAC output. Adjusting the timing of the $\overline{WR}$ signal so that it is low only when data is valid eliminates this problem.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance C_{OUT1} and the internal feedback resistor, R_{FB}. Its value depends on the type of op-amp used but typically ranges from 10pF to 3pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at OUT1 as small as possible.

Grounding and Bypassing

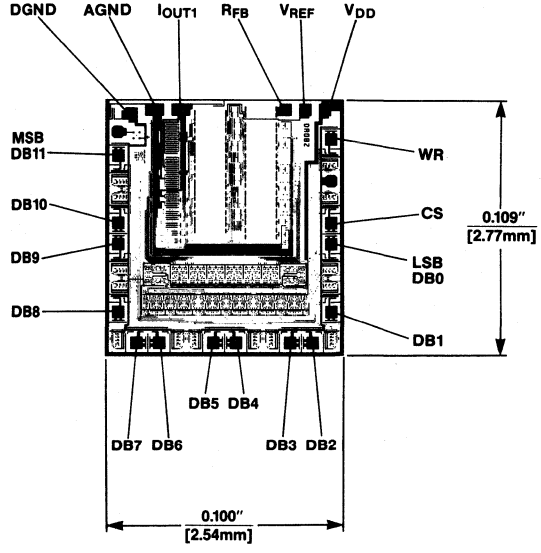
Since OUT1, AGND and noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2ohms) connection. The current at OUT1 and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC V_{DD} and DGND pins as possible.

The AD7545 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is also a good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1Mohms) to prevent static charge accumulation if these pins are left floating, such as when a circuit card is left unconnected.

It is also recommended that two back-to-back diodes be connected between the DGND and AGND pins in those systems where these pins tie on the backplane.

Chip Topology



Voltage References

3

Voltage References

Part Number	Output Voltage	Temperature Coefficient (ppm/°C)	Initial Output Voltage Accuracy	Supply Voltage	Supply Current (Typ/Max mA)	Features	Page No.
MAX670	10V	3	±2.5mV	+15V	9/14	Kelvin sensing	3-1
MAX671	10V	1	±1.0mV	+15V	9/14	Kelvin sensing	3-1
MAX672	10V	5	±5mV	+13V to +40V	1/1.4	Precision/Low Cost	3-7
MAX673	5V	5	±2.5mV	+8V to +40V	1/1.4	Precision/Low Cost	3-7
AD580	2.5V	10	±10mV	+15V	0.75/1.0	+5V power	3-11
AD581	10V	5	±5mV	+15V	0.75/1.0		3-13
AD584	10V, 7.5V, 5V, 2.5V	5	±5mV	+15V	0.75/1.0	Programmable output voltage	3-19
AD2700	10V	3	±2.5mV	+15V	9/14	Precision	3-25
AD2710	10V	1	±1.0mV	+15V	9/14	Precision	3-25
AD2701	-10V	2	±2.5mV	-15V	9/14	Precision	3-25
ICL8069	1.23V	10 to 100	±25mV	—	50μA to 5mA	2 terminal bandgap reference	3-29
REF01E	10V	8.5	±30mV	+15V	1/1.4		3-31
REF01HP	10V	25	±50mV	+15V	1/1.4		3-31
REF02E	5V	8.5	±15mV	+15V	1/1.4		3-31
REF02HP	5V	25	±25mV	+15V	1/1.4		3-31

Voltage Reference Terminology

Kelvin Sensing: Also Four Terminal Sensing. A voltage sourcing technique where the connections that supply power to a load are separate from those that sense the voltage at the load. A precise voltage can then be supplied at high current since errors caused by wire resistance are eliminated.

Line Regulation: The output voltage change as a function of a specified change in input voltage. Specified in %/ΔV or μV/ΔV.

Load Regulation: The output voltage change as a function of a specified change in load current. Specified in μV/mA or Ω.

Long-Term Stability: The output voltage change with time at a specified temperature. Specified in ppm/1000hrs.

Temperature Coefficient: The average change in output voltage for a specified range of temperature. Specified in ppm/°C or mV/°C.

Turn-On Settling Time: The time required for the output to settle within specified limits from a cold start. Does not include thermal settling time which depends on external conditions.

Voltage Change with Temperature: The total deviation from the actual output at +25°C over the specified temperature range. Specified in mV or %.

Quiescent Current: The power supply current required to operate the reference under no-load conditions. Specified in mA or μA.

MAXIM

+10V Precision Kelvin Sensed References

General Description

The MAX670/671 are precision +10 volt reference sources with Kelvin connections on both output and ground, which offer superior load regulation and line regulation independent of the line impedance between the reference and load. The MAX670 has initial accuracy of 2.5mV with 3ppm/°C temperature coefficient and the MAX671 is specified with initial accuracy of 1.0mV and temperature coefficient of 1ppm/°C. Both devices are designed to upgrade existing sockets which employ the popular AD2700 and AD2710 series by connecting a few of the unused pins together to obtain improved performance. The MAX670/671 have two methods of fine trim adjustment, one which is an improved technique which will not disturb the output voltage temperature coefficient, and the other is compatible with the AD2700/2710. All parts are packaged in 14 lead ceramic side brazed DIP and include burn-in at +150°C.

Applications

Precision D/A and A/D Converters

Digital Voltmeters

Precision Test and Measurement System

Precision Calibrated Voltage Reference Standard

High Accuracy Transducers

Features

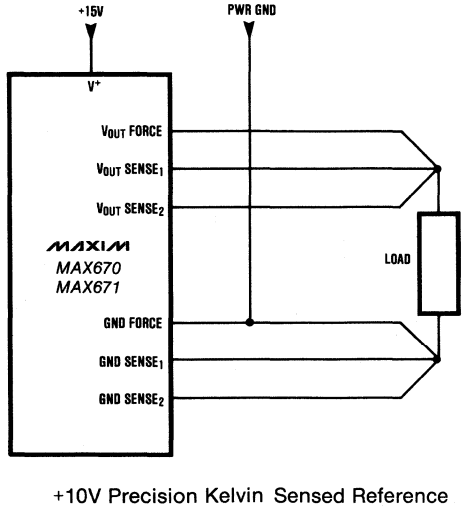
- **Superior Load Regulation: 10μV/mA Max.**
- **Superior Line Regulation: 50μV/V Max.**
- **Excellent Initial Accuracy: +10V ±1mV Max. (MAX671)**
- **Low Temperature Coefficient: 1ppm/°C Max. (MAX671)**
- **10mA Output Current**
- **High Current Capability with External Transistor**
- **Functionally Compatible with AD2700 and AD2710**

Ordering Information

PART	INIT. ACC.	*TEMP. COEFF.	TEMP. RANGE
MAX670CDD	2.5mV	3ppm/°C	0°C to +70°C
MAX670EDD	2.5mV	3ppm/°C	-40°C to +85°C
MAX670MDD	2.5mV	3ppm/°C	-55°C to +125°C
MAX671CDD	1.0mV	1ppm/°C	0°C to +70°C
MAX671EDD	1.0mV	1ppm/°C	-40°C to +85°C
MAX671MDD	1.0mV	1ppm/°C	-55°C to +125°C

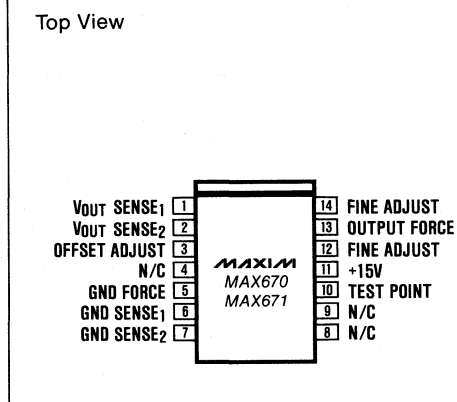
(All devices are packaged in a 14 lead ceramic side brazed DIP.)
**Restricted temperature range (See Electrical Characteristics).*

Typical Operating Circuit



+10V Precision Kelvin Sensed Reference

Pin Configuration



+10V Precision Kelvin Sensed References

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... +20V
Power Dissipation 400mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Short Circuit to GND ..... Continuous

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, T_A = +25°C, R_L = 2kΩ, unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Initial Output Voltage	V_O	MAX670		9.9975	10.0000	10.0025	V
		MAX671		9.9990	10.0000	10.0010	
Output Voltage Drift (See Figures 12 and 13)	$\Delta V_O/\Delta T$	MAX670C	T_A to +70°C T_A to 0°C	-3 -5		+3 +3	ppm/°C
		MAX670E	T_A to +85°C T_A to -40°C	-3 -5		+3 +3	
		MAX670M	T_A to +85°C T_A to +125°C +85°C to +125°C T_A to -55°C	-3 -5 -10 -5		+3 +3 +3 +3	
		MAX671C	T_A to +70°C T_A to 0°C	-1 -5		+1 +1	
		MAX671E	T_A to +85°C T_A to -40°C	-1 -5		+1 +1	
		MAX671M	T_A to +85°C T_A to +125°C +85°C to +125°C T_A to -55°C	-1 -5 -10 -5		+1 +1 +1 +1	
Load Regulation	$\Delta V_O/\Delta I_O$	0mA to 10mA to GND MAX670 MAX671				20 10	μV/mA
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 13.5V to 16.5V MAX670 MAX671				100 50	μV/V
Input Voltage Range	V_{IN}			13.5		16.5	V
Supply Current	I_S	No Load			9	14	mA
Noise (Note 1)	e_N	0.1Hz to 10Hz			12	50	μV_{P-P}
Long Term Stability	$\Delta V_O(T)$	T_A = +55°C			50		ppm/1K hrs
Output Adjust Range	$\Delta V_{ADJ.}$	per Figure 10			20		mV
Output Adjust vs. TC	$\frac{\Delta V_O/\Delta T}{\Delta V_{ADJ.}}$	per Figure 10			0.4		ppm/°C/mV

Note 1: This parameter is sample tested to 10% LTPD, and is not used to calculate outgoing quality level.

+10V Precision Kelvin Sensed References

Theory of Operation

A temperature compensated zener diode is applied to the non-inverting input of an operational amplifier (Figure 1). The zener voltage is amplified and accurately laser trimmed to produce a precise 10.000V. The zener operating current is derived from the regulated output voltage, and actively laser trimmed for the lowest temperature coefficient at the output of the op amp.

The MAX670 and MAX671 each have three Kelvin connections for both output and ground which eliminates errors due to the I-R voltage drops from the resistance of the pins, sockets, and connecting wires. The FORCE pin output current varies as the load changes such that the voltage reflects changes due to I-R drops as well. V_{OUT} SENSE1 and GND SENSE1 are the gain resistors of the op amp that are used to maintain to a precise voltage the points at the load to which they are connected. The V_{OUT} SENSE2 and GND SENSE2 pins when connected in the circuit are constant current points but do not contribute errors from I-R drops as long as they are connected to the same points as V_{OUT} SENSE1 and GND SENSE1.

Applications Information

The Force and Sense lines should be connected together as close as possible to the load or reference input of the converter. The power supply ground must be connected either at the same ground point at the load or along the GND FORCE path.

The additional benefit of separate Force and Sense lines allows the use of an external buffer for increased output current while maintaining the specified output accuracy. There are several methods of buffering, the choice of which depends on the constraints of the application.

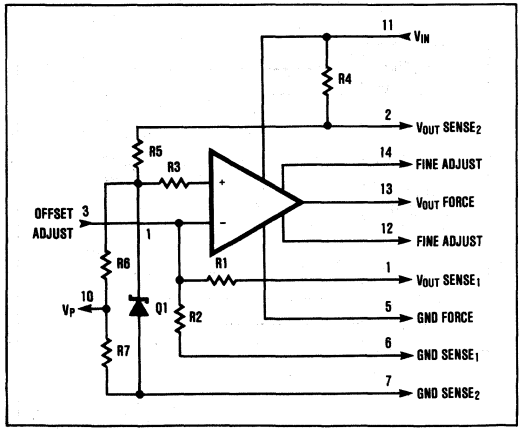


Figure 1. MAX670/671 Schematic Diagram

Emitter Follower

An NPN transistor can be used as a buffer for very low impedance output if only current sourcing (i.e. from Output to GND) is desired (Figure 2). It is advisable to place a small resistor in series with the base of the transistor to prevent oscillation unless the f_T is low. Since the Sense lines will keep the emitter at 10V, the base will rise up to about 10.7V due to the transistor Vbe. This limits the low end of the supply range, especially at cold temperatures where the Vbe of the transistor is the largest and the headroom of the internal op amp is lowest. The output of the internal op amp on the Force pin will change as much as necessary over temperature to maintain the Sense pins on the emitter at a constant voltage.

Similarly, a FET (Figure 3) can be used as a source follower. However, the V_T of a N-channel FET must be low, about 2V, so that the MAX670 output will

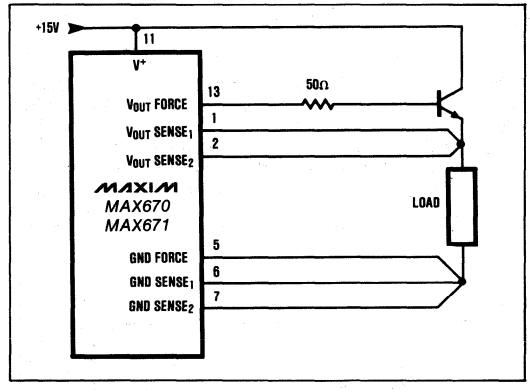


Figure 2. NPN Emitter Follower

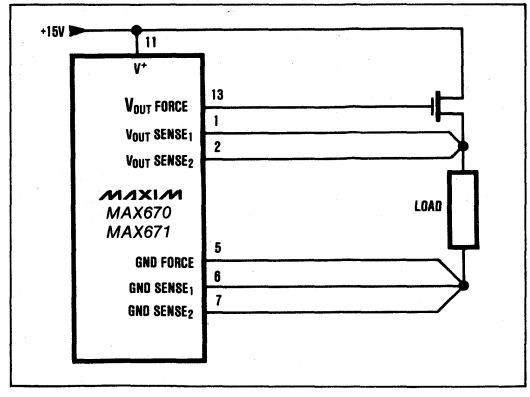


Figure 3. FET Source Follower

+10V Precision Kelvin Sensed References

have sufficient headroom. Alternatively, a P-channel FET, whose gate voltage will be more negative than the source would be more suitable because the op amp output voltage would be driven further into the middle of its output swing range.

If the load only requires the reference to sink current, a PNP transistor can be used as shown in Figure 4.

+12 Volt Operation

A few forward biased diodes in series with the base of the transistor in Figure 5 will drop the MAX670 output by as many Vbe's for more op amp headroom and therefore lower operating voltage. Over temperature, the MAX670 V_{OUT} FORCE will change as much as required due to the temperature coefficient of the Vbe's. One diode will best compensate the Vbe of the transistor so that the Force output will be close to 10V. However, two diodes will place the internal op amp output at about 9.3V to give enough headroom for 12V ±10% operation (i.e. 11.4V minimum).

External Buffer

A more simple, yet more costly method to increase the output current is by the use of an external buffer amplifier, such as a BUF-03, LH0002, or an LH0033 (Figure 6) for up to 100mA of output current. The Force output drives the buffer input, while the Sense lines maintain the buffer output to the initial +10V value, even if the offset drift is high. V_{OUT} SENSE2 can be connected to the input of the buffer if necessary, but there will be a small second order error over temperature as the offset drift slightly changes the reference zener operating current. Therefore it is always better to connect both SENSE lines together at the load.

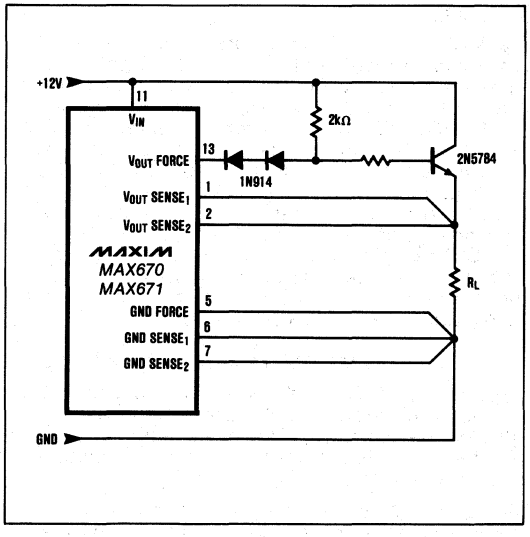


Figure 5. Application Circuit for 12V Operation, 120mA Output Current

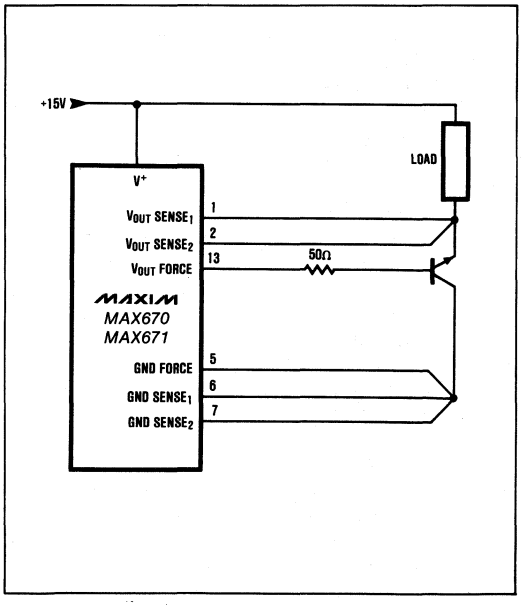


Figure 4. PNP Emitter Follower

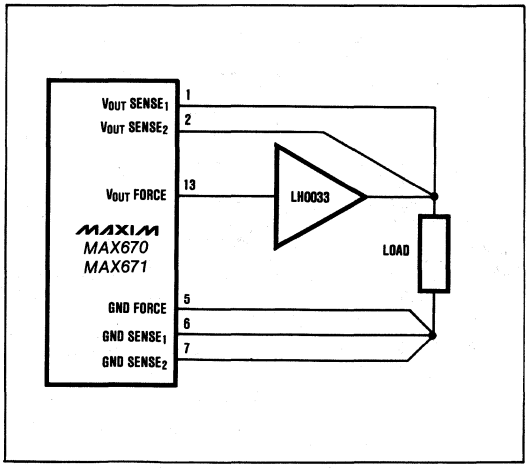


Figure 6. 100mA Output Current with Buffer Amplifier

+10V Precision Kelvin Sensed References

High Power Output

The specified accuracy of the MAX670 can be obtained even at currents of several amps using a Power Amplifier such as the LH0101 as a non-inverting buffer amplifier (Figure 7). By placing the amplifier inside the loop and sensing the output, the reference will have a 2A output capability keeping in mind the heat sink requirements of the LH0101.

High Speed Buffer

In some cases, the reference is required to drive a circuit that contains high speed transients or glitches which must settle back to a steady state value quickly. In this case a fast op amp can be used on the output, such as an HA-2525 or a BB3554 (Figure 7). The high bandwidth of these amplifiers enables them to settle quickly at the expense of higher noise bandwidth that may restrict their applications.

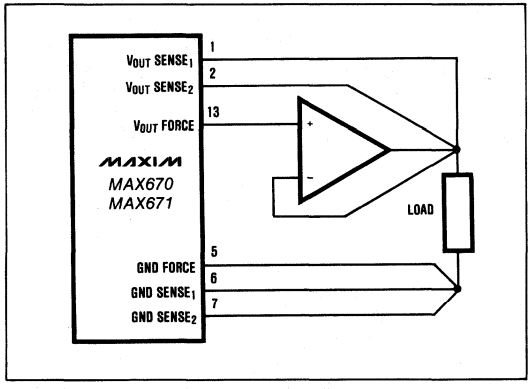


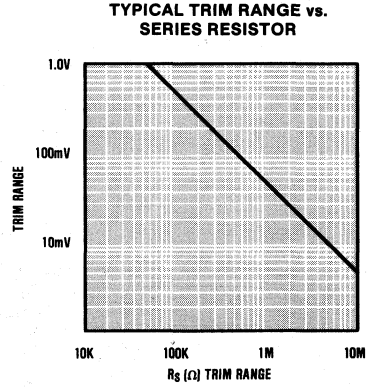
Figure 7. 2A Output Current Using LH0101 Power Amplifier or BB3554 FAST Op-Amp

Load Balancing

If the load current is known, and is constant, such as in the case of driving the reference input of numerous D/A converters, a pull up resistor (Figure 8) can be used to match the load current to ground with the MAX670 regulating the output voltage and supplying the error current up to 10mA. For this special case, the cost of an amplifier is eliminated and the circuit complexity is reduced.

Offset Adjust

The output voltage of the MAX670 and MAX671 can be adjusted in two ways. The Offset Adjust Input on pin 3 (Figure 9) has the unique advantage of changing the output voltage without disturbing the temperature coefficient. Also, a wide variety of trim range and resolution can be obtained by appropriate selection of the resistor in series with pin 3 as shown in graph below.



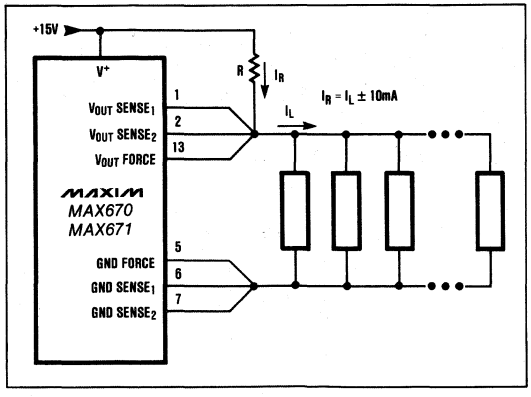


Figure 8. Pull Up Resistor Load Balancing

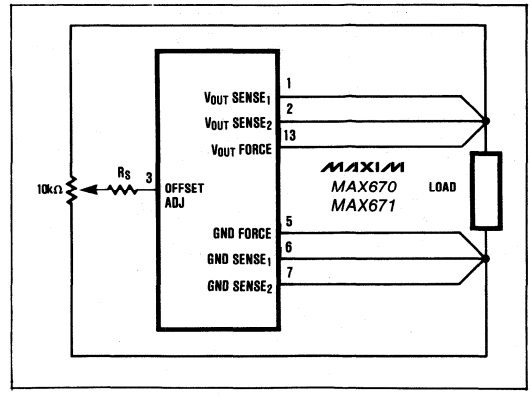


Figure 9. MAX670/671 Improved TC Independent Trim Adjustment

+10V Precision Kelvin Sensed References

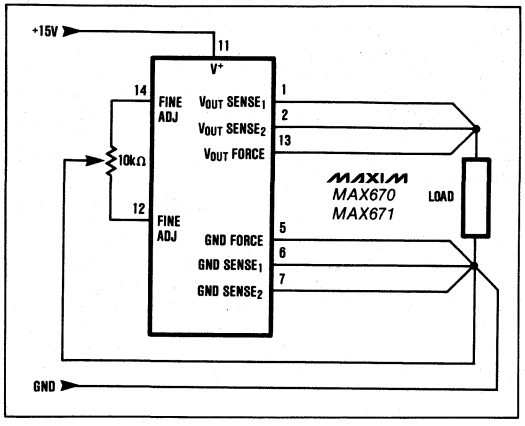


Figure 10. AD2700/2710 Compatible Trim Adjustment

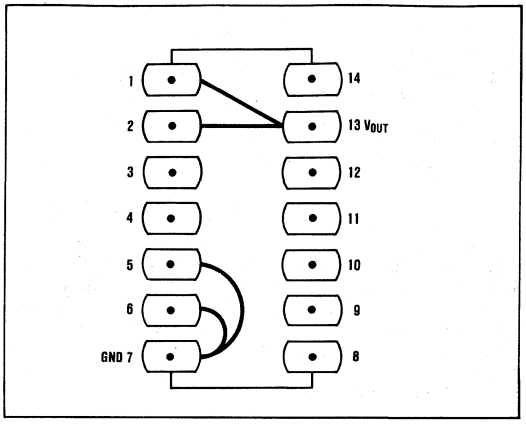


Figure 11. Using MAX670/671 in AD2700/2710 Sockets

The other adjustment method is designed to be compatible with the AD2700/AD2710 series of references. A potentiometer is connected between pins 12 and 14 with the wiper to ground (Figure 10), but this method affects the output temperature coefficient by approximately 0.4ppm/°C per millivolt of adjustment.

Upgrading AD2700/AD2710

Any existing socket containing an AD2700 or AD2710 can be easily adapted to the MAX670 or MAX671 by shorting pin 13 to pins 1 and 2, and also shorting pin 7 to pins 5 and 6 (Figure 11).

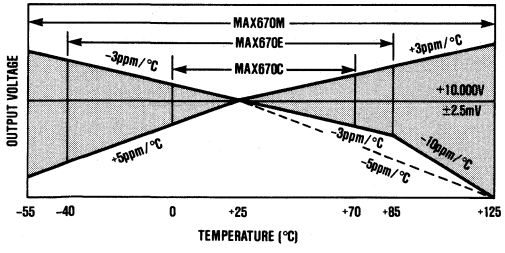


Figure 12. MAX670 Temperature Coefficient

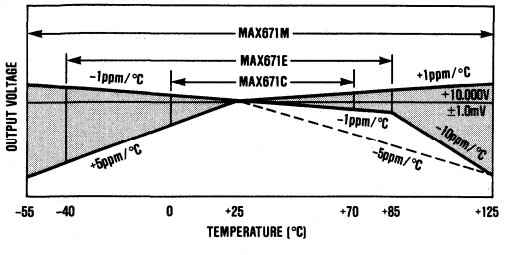
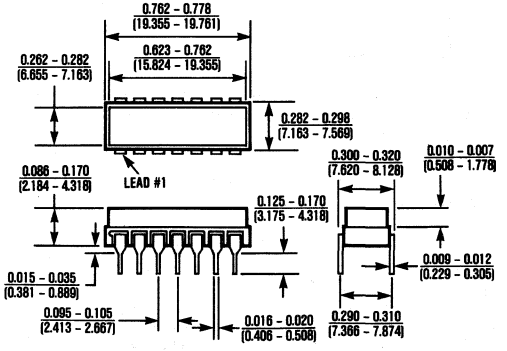


Figure 13. MAX671 Temperature Coefficient

Package Information



14 Lead HYBRID
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUTION OF LIMITED NUMBER OF DEVICES

MAXIM

+5V, +10V Precision Voltage References

General Description

The MAX672 and MAX673 are precision voltages references that are pretrimmed to within ±.05% of 10V and 5V respectively. Both references feature excellent temperature stability (as low as 5.0 ppm/°C worst case), low current drain and low noise. The MAX673 also provides a TEMP pin whose output voltage varies linearly with temperature, making this device suitable for a wide variety of temperature sensing and control applications. Both devices are available from Maxim in the space-saving Small Outline package, as well as the standard 8 pin TO-99 and MINI-DIP packages.

Applications

A to D Converters

D to A Converters

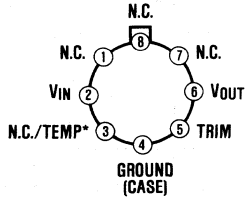
Digital Voltmeters

Voltage Regulators

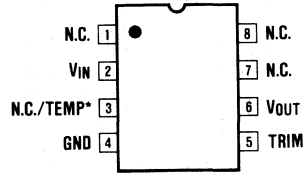
Threshold Detectors

Pin Configuration

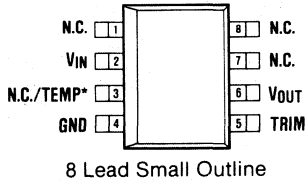
Top View



8 Lead TO-99 Metal Can



8 Lead DIP



8 Lead Small Outline

***NOTE:** Pin 3 is N.C. (No Connection) on MAX672, TEMP Output on MAX673

Features

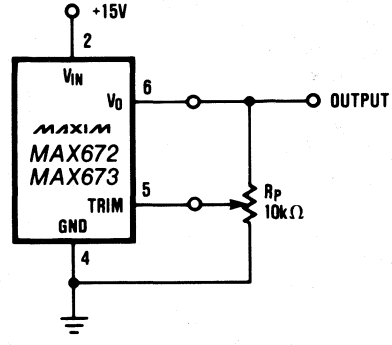
- **Pretrimmed to +5V, +10V ±0.05%**
- **Excellent Temperature Stability 2 ppm/°C**
- **Low Noise: 10μV_{p-p} (MAX673)**
- **Low Supply Current: 1.4mA Max**
- **Short Circuit Proof**
- **Load Regulation 0.001%/mA**
- **Improved REF01 and REF02**

Ordering Information

PART	V_{OUT} @ 25°C	PACKAGE*
TEMP RANGE: 0°C TO +70°C		
MAX672CTV	10V ± 5mV	TO-99
MAX672CPA	10V ± 5mV	Plastic Dip
MAX672CSA	10V ± 5mV	Small Outline
TEMP RANGE: -40°C TO +85°C		
MAX672ETV	10V ± 5mV	TO-99
MAX672EJA	10V ± 5mV	CERDIP
MAX672EPA	10V ± 5mV	Plastic Dip
MAX672ESA	10V ± 5mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
MAX672MTV	10V ± 5mV	TO-99
MAX672MJA	10V ± 5mV	CERDIP

(Ordering information continued on page 4.)

Typical Operating Circuit



Reference with Trimmed Output

3

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Power Dissipation
TO99 (TV) (Derate at 7.1mW/°C above +80°C) 500mW
CERDIP (J) (Derate at 6.7mW/°C above +75°C) 500mW
Plastic DIP (P) (Derate at 5.6mW/°C above +36°C) 500mW
Small Outline (S) (Derate at 5.0mW/°C above +55°C) ... 300mW
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
MAX672M/MAX673M ..... -55°C to +125°C
MAX672E/MAX673E ..... -40°C to +85°C
MAX672C/MAX673C ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
DICE Junction Temperature (T_J) .. -65°C to +150°C
Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX672			MAX673			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	9.995	10.000	10.005	4.9975	5.000	5.0025	V
Output Adjustment Range	ΔV_{trim}	R_P = 10kΩ	±3	±6		±3	±6		%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)		10	15		10	15	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 13V to 33V (MAX672) V_{IN} = 8V to 33V (MAX673)		0.006	0.010		0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA		0.001	0.002		0.001	0.002	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value		5			5		μs
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4		1.0	1.4	mA
Sink Current	I_S		-0.3	-0.5		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA
Temperature Voltage Output	V_T	(Note 2)					630		mV

ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, $T_{MIN} \le T_A \le T_{MAX}$, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX672			MAX673			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		.014 .022 .036	.035 .055 .090		.014 .022 .036	.035 .055 .090	%
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		1.40 2.20 3.60	3.50 5.50 9.00		0.70 1.10 1.80	1.75 2.75 4.50	mV
Output Voltage Temperature Coefficient	TCV_O	(Note 5)		2	5		2	5	ppm/°C
Line Regulation (Note 1) (V_{IN} = 13V to 33V) (MAX672) (V_{IN} = 8V to 33V) (MAX673)		0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		0.007 0.008 0.009	0.012 0.013 0.015		0.007 0.008 0.009	0.012 0.013 0.015	%/V %/V
Load Regulation (I_L = 0 to 8mA) (Note 1)		0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C -55°C ≤ T_A ≤ +125°C		0.001 0.001 0.001	0.002 0.002 0.002		0.001 0.001 0.001	0.002 0.002 0.002	%/mA

Note 1: Line and Load Regulation specifications include the effect of self heating.
Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
Note 3: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V (MAX672) or 5V (MAX673).
Note 4: ΔV_{OT} specification applies trimmed to +10.000V/5.000V or untrimmed.
Note 5: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 6: Sample tested.

Output Adjustment

The MAX672(MAX673) trim terminal can be used to adjust the voltage over a 10V(5V) ± 300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V(5V), including 10.240V for binary applications (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment.

Temperature Voltage Output

The MAX673 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately 2.1mV/°C (Figure 2).

Output Voltage = 2.1(T + 273)mV
where T = Temperature in °C

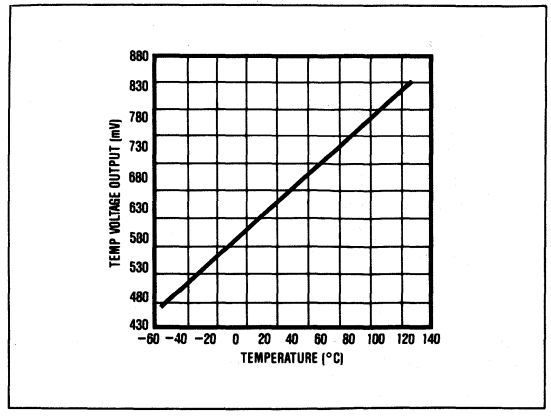
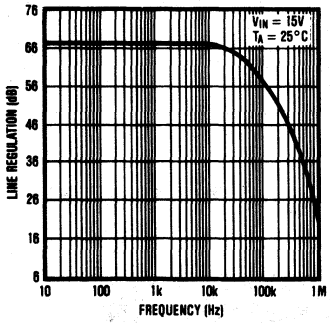


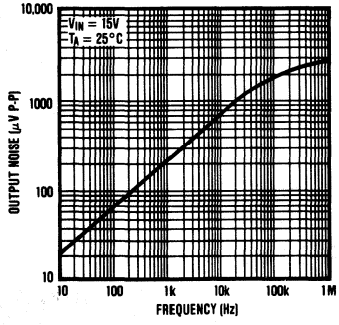
Figure 2. MAX673 Temperature Voltage Output vs. Temperature.

Typical Operating Characteristics

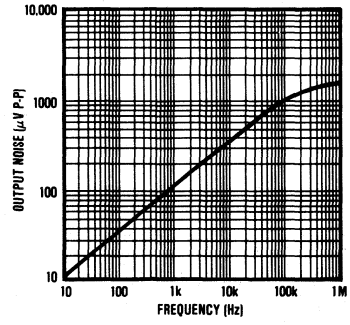
LINE REGULATION vs FREQUENCY



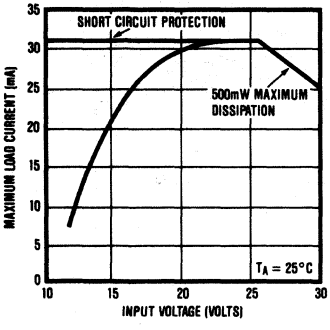
MAX672 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



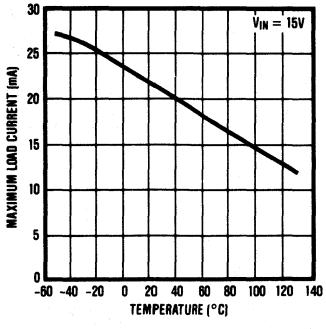
MAX673 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



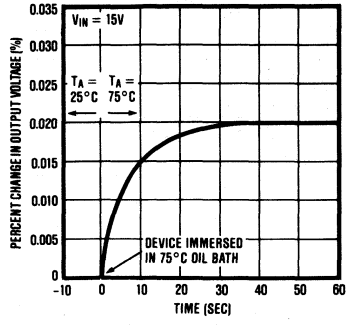
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



MAXIMUM LOAD CURRENT vs TEMPERATURE



OUTPUT CHANGE DUE TO THERMAL SHOCK



+5V, +10V Precision Voltage References

Typical Applications

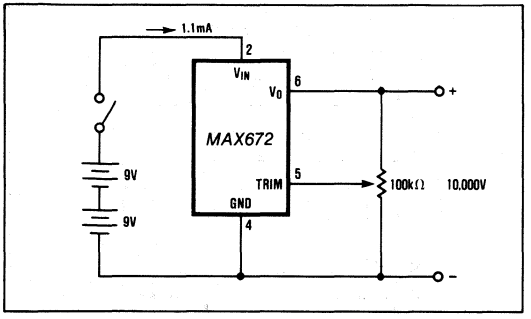


Figure 3. Precision Calibration Standard

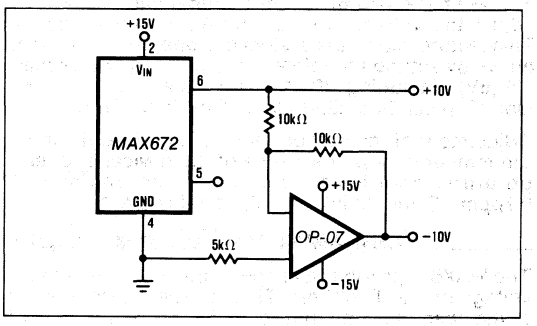


Figure 4. ±10V Reference

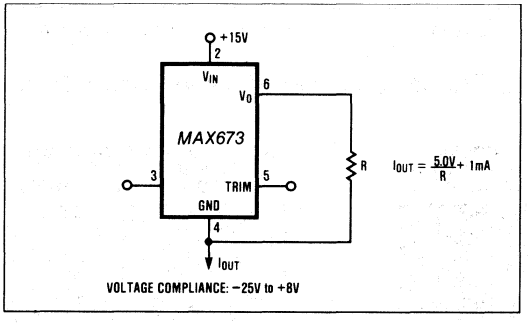


Figure 5. Current Source

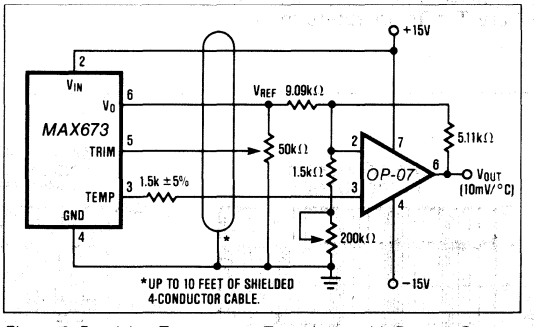
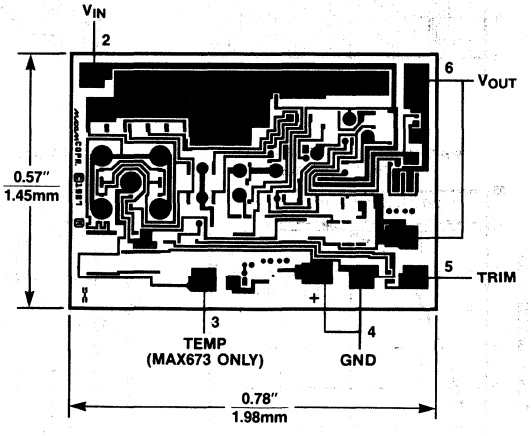


Figure 6. Precision Temperature Transducer with Remote Sensor

Ordering Information (continued)

PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C		
MAX673CTV	5V ± 2.5mV	TO-99
MAX673CPA	5V ± 2.5mV	Plastic Dip
MAX673CSA	5V ± 2.5mV	Small Outline
TEMP RANGE: -40°C TO +85°C		
MAX673ETV	5V ± 2.5mV	TO-99
MAX673EJA	5V ± 2.5mV	Hermetic Dip
MAX673EPA	5V ± 2.5mV	Plastic Dip
MAX673ESA	5V ± 2.5mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
MAX673MTV	5V ± 2.5mV	TO-99
MAX673MJA	5V ± 2.5mV	Hermetic Dip

Chip Topography



MAXIM

High Precision +2.5 Volt Reference

General Description

The AD580 is a high performance three-terminal voltage reference which provides a stable +2.5V source for 8, 10, and 12-bit data converters and analog functions. A temperature compensated internal bandgap operates from +4.5V to +30V and consumes only 1.5mA.

The reference can be connected directly to a number of CMOS A-to-D and D-to-A converters and is especially convenient in +5V powered systems. An inital untrimmed accuracy of 0.4% and temperature stability of 10ppm/°C allow adjustment-free designs in many precision applications.

Available packages include TO-52 metal cans for commercial and military temperature grades, as well as 8 lead small outline for commercial grade devices.

Applications

CMOS Data Conversion
Digital Panel Meters
Portable Instrumentation
Remote Measurement Systems
Logic Powered Analog Systems

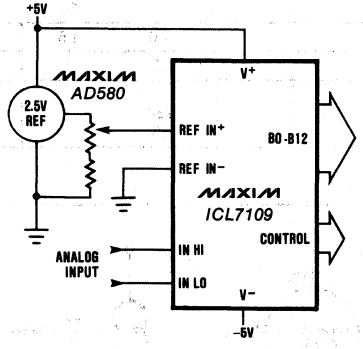
Features

- **2.500V ±0.4% Accuracy (AD580L/M)**
- **10ppm/°C Temperature Stability (AD580M)**
- **No Adjustments**
- **250μV Long Term Stability**
- **1.5mA Quiescent Current**
- **+4.5V to +30V Operation**

Ordering Information

PART	TEMP. RANGE	PACKAGE	TOLERANCE
AD580JH	0°C to +70°C	TO-52 Can	±75mV
AD580KH	0°C to +70°C	TO-52 Can	±25mV
AD580LH	0°C to +70°C	TO-52 Can	±10mV
AD580MH	0°C to +70°C	TO-52 Can	±10mV
AD580JCSA	0°C to +70°C	8 Lead S.O.	±75mV
AD580KCSA	0°C to +70°C	8 Lead S.O.	±25mV
AD580LCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD580MCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD580SH	-55°C to +125°C	TO-52 Can	±25mV
AD580TH	-55°C to +125°C	TO-52 Can	±10mV
AD580UH	-55°C to +125°C	TO-52 Can	±10mV

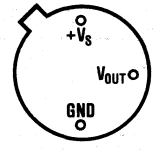
Typical Application



Reference for 12-Bit A/D Converter

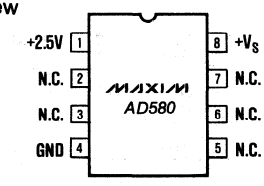
Pin Configurations

Bottom View



TO-52

Top View



8 Lead Small Outline

High Precision +2.5 Volt Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to GND ..... -0.3V, +40V
Power Dissipation
  TO-52 Metal Can (Derate 2.8mW/°C above +25°C) ... 350mW
  Small Outline (Derate 5.3mW/°C above +75°C) 400mW
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
  Commercial (J, K, L, M) ..... 0°C to +70°C
  Military (S, T, U) ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +175°C

Lead Temperature (Soldering 10sec) ..... +300°C
Junction Temperature (T_j) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
  TO-52 Metal Can ..... 360°C/W
  Small Outline Package ..... 170°C/W
Junction to Case
  TO-52 Metal Can ..... 100°C/W
  Small Outline Package ..... 55°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance		I_L = 0mA;	AD580J/S			±75	mV
			AD580K/T			±25	
			AD580L/M/U			±10	
Output Voltage Change with Temperature, (Temperature Coefficient)		T_A = 0°C to +70°C;	AD580J			15 (85)	±mV (ppm/°C)
			AD580K			7 (40)	
			AD580L			4.3 (25)	
			AD580M			1.75 (10)	
		T_A = -55°C to +125°C;	AD580S			25 (55)	
			AD580T			11 (25)	
			AD580U			4.5 (10)	
Line Regulation		I_L = 0mA, +4.5V < V_{IN} < +7V;	AD580J/S		0.3	3	mV
			AD580K		0.3	2	
			AD580L/M/T/U			1	
		I_L = 0mA, +7V < V_{IN} < +30V;	AD580J/S		1.5	6	
			AD580K		1.5	4	
			AD580L/M/T/U			2	
Load Regulation		I_L = 0mA to 10mA				10	mV
Quiescent Supply Current	I_Q	I_L = 0mA			1.0	1.5	mA
Noise	e_{NP-P}	0.1Hz to 10Hz			60		μV_{P-P}
Stability Long Term					250		μV
Stability Per Month					25		

Note 1: Absolute Maximum power dissipation must not be exceeded.

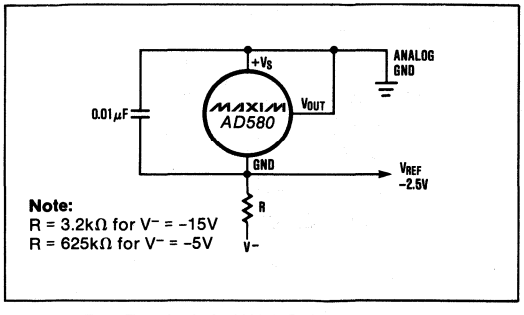


Figure 1. Two-Terminal -2.5V Volt Reference

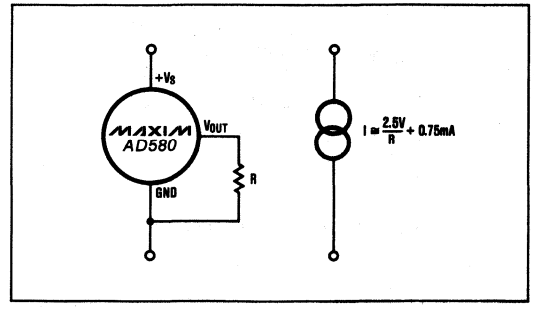


Figure 2. Two-Component Precision Current Limiter

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

High Precision 10 Volt Reference

General Description

Maxim's AD581 is a three-terminal, temperature compensated, band-gap voltage reference which provides a precise 10.00V output from an unregulated input of 12.5V to 30V. Laser trimming is used to minimize initial error and temperature drift, to as low as 5mV and 5ppm/° C with the AD581L.

No external components are needed to acheive full accuracy over the operating temperature range. Total supply current to the device, including the internal output buffer amplifier, is typically 750μA.

The AD581 is designed for use with 8 to 14 bit A/D and D/A converters as well as data acquisition systems. The reference is available in a 3 pin TO-5 metal can and 8 lead small outline surface mount package.

Applications

CMOS DAC Reference
A/D Converter Reference
Measurement Instrumentation
Threshold Detectors
Precision Analog Systems

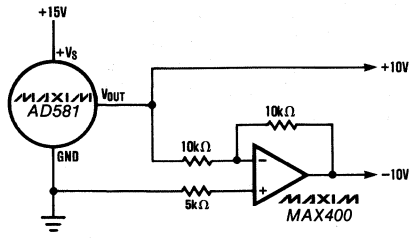
Features

- ±5mV Tolerance (AD581L)
- Low Tempco — 5ppm/° C Max. (AD581L)
- No External Components or Trims
- Short Circuit Proof
- Output Sources and Sinks Current
- 10mA Output Current
- Low Supply Current — 1.0mA Max.
- Three-Terminal Package

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
AD581JH	0°C to +70°C	TO-39 Can	±30mV
AD581KH	0°C to +70°C	TO-39 Can	±10mV
AD581LH	0°C to +70°C	TO-39 Can	±5mV
AD581JCSA	0°C to +70°C	8 Lead S.O.	±30mV
AD581KCSA	0°C to +70°C	8 Lead S.O.	±10mV
AD581LCSA	0°C to +70°C	8 Lead S.O.	±5mV
AD581SH	-55°C to +125°C	TO-39 Can	±30mV
AD581TH	-55°C to +125°C	TO-39 Can	±10mV
AD581UH	-55°C to +125°C	TO-39 Can	±5mV

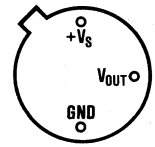
Typical Operating Circuit



±10 Volt Reference

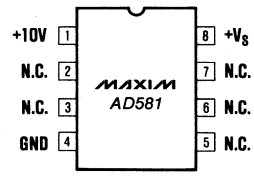
Pin Configurations

Bottom View



TO-39

Top View



8 Lead Small Outline

High Precision 10 Volt Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to GND ..... -0.3V, +40V
Power Dissipation
  Metal Can (Derate 6.7mW/°C above 60°C) 600mW
  Small Outline (Derate 5.3mW/°C above 75°C) 400mW
Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
  Commercial (J, K, L) ..... 0°C to +70°C
  Military (S, T, U) ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +175°C
Lead Temperature (Soldering 10sec) ..... +300°C
Dice Junction Temperature (Tj) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
  Metal Can ..... 150°C/W
  Small Outline Package ..... 170°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

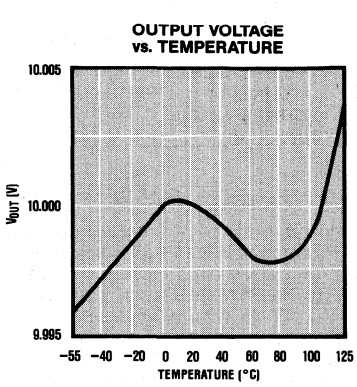
(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

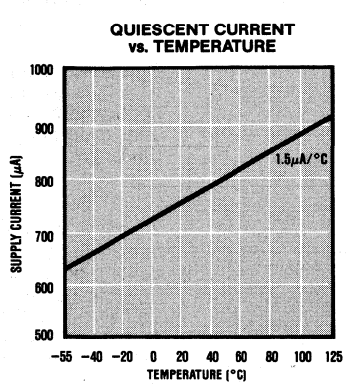
PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance			I_L = 0mA, AD581J/S AD581K/T AD581L/U				±30 ±10 ±5	mV
Output Voltage Change with Temperature, (Temperature Coefficient)			AD581J AD581K AD581L AD581S AD581T AD581U				13.5 (30) 6.75 (15) 2.25 (5) 30 (30) 15 (15) 10 (10)	±mV (ppm/°C)
Line Regulation			No Load, +12.5V < V_{IN}< +15V +15V < V_{IN} < +30V				0.005 (1.0) 0.002 (3.0)	%/V (mV) %/V (mV)
Load Regulation			I_L = 0mA to 5mA			20 (200)	50 (500)	ppm/mA (μV/mA)
Quiescent Supply Current		I_Q	I_L = 0mA			750	1000	μA
Turn-on Settling Time to 0.1%		t_{ON}				200		μs
Noise		e_{NP-P}	0.1Hz to 10Hz			50		μV_{P-P}
Long-Term Stability			(Non-Cumulative)			25		ppm/kHrs
Short Circuit Current		I_{SC}				30		mA
Output Current	Source	I_L	V_{IN} > V_{OUT} + 2.5V	T_A = +25°C T_{MIN} to T_{MAX}	10 5			mA
	Sink			T_{MIN} to T_{MAX}, AD581J/K/L AD581S/T/U -55°C to +85°C, AD581S/T/U	5 0.2 5			

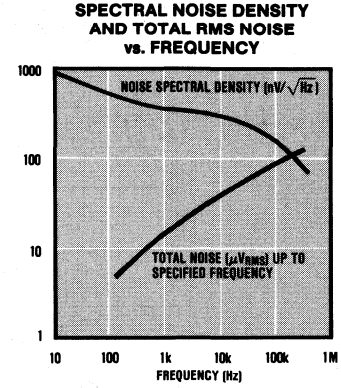
Note 1: Absolute Maximum power dissipation must not be exceeded.

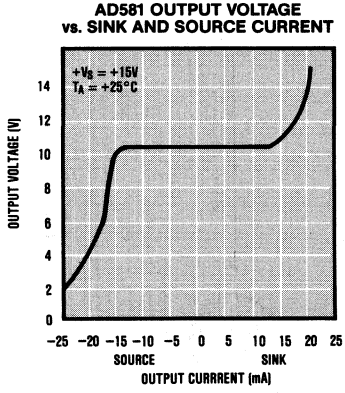
High Precision 10 Volt Reference

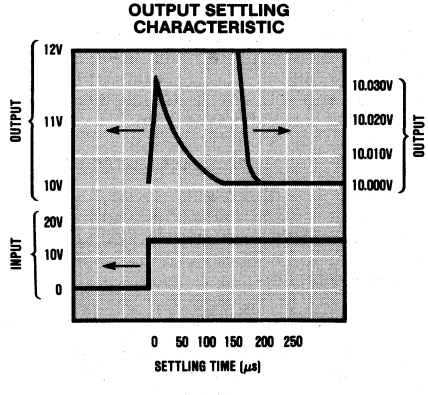
Typical Operating Characteristics











Detailed Description

As shown in Figure 1, most applications of the AD581 require no external components. Connections are $+V_S$, V_{OUT}, and GND (GND is tied to the case in the TO-5 package). Usually the desired accuracy is obtained by selecting the appropriate device grade. However, any part can be adjusted to a tighter tolerance, or to slightly different voltage, using the fine trim circuit in Figure 2. The table in Figure 2 lists the trim range for different values of R in the figure, and also shows the effect on temperature coefficient.

Voltage Temperature Coefficient

The temperature characteristic of the AD581 consistently follows an "S-curve" (see Typical Operating Characteristics). A five-point 100% test guarantees compliance with -55° C to +125° C specifications and a three-point 100% test guarantees 0° C to +70° C specifications.

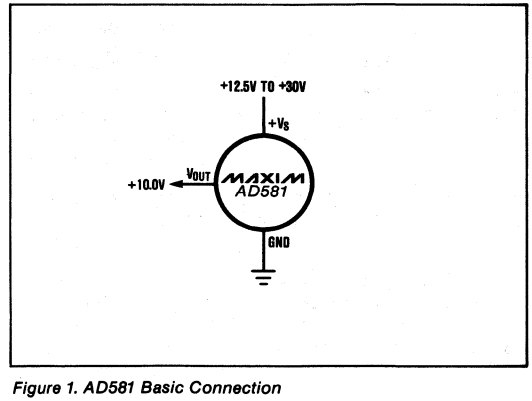
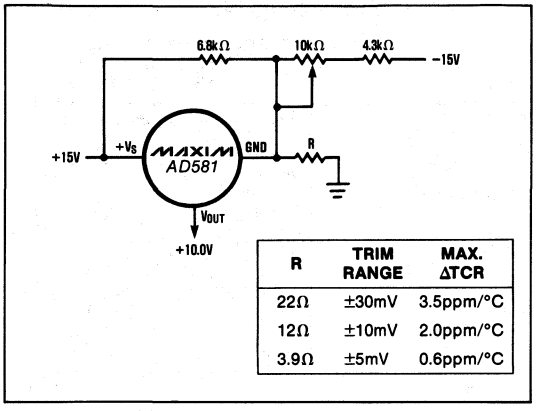


Figure 1. AD581 Basic Connection

High Precision 10 Volt Reference



R	TRIM RANGE	MAX. ΔTCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

The Voltage Change specifications in the Electrical Characteristics table state the maximum deviation over temperature from the reference's initial value at 25°C, as well as drift in ppm/°C. By adding the maximum deviation for a given device to its initial tolerance, the total error is quickly determined.

Output Current

The AD581 is unique in that it can sink as well as source current. The circuit is also protected for output shorts to either $+V_S$ or GND. The output voltage versus current characteristic is shown in the Typical Operating Characteristics section.

Dynamic Performance

The turn-on characteristics and settling performance of the AD581 are shown in the Typical Operating Characteristics. Both coarse and fine transient response is shown. The reference typically settles to 1mV within 180μs after power is applied.

Applications

Precision High Current Reference

A PNP power transistor, or Darlington, is easily connected to the AD581 to greatly increase its output current. The circuit of Figure 3 provides a +10V output at up to 4 Amps. If the load has a significant capacitive component, compensation capacitor, C1, should be added. If the load is purely resistive, high frequency supply rejection is improved without C1.

Low Input Voltage

Although line regulation is specified from 12.5V to 40V, the AD581 can operate with a +12V ±5% input by adding a resistor as shown in Figure 4. The resistor reduces the current that must be supplied from V_{OUT}. Note that the resistor cannot be used at higher input voltages since, as the supply increases, it sources more current than V_{OUT} can sink.

Current Limiter

By adding a single resistor as shown in Figure 5, the AD581 is turned into a precision current limiter for applications where the driving voltage is 12.5V to 40V. The programmed current ranges from 0.75mA to 5mA.

Negative 10V Reference

Where a -10V reference is required, the AD581 can be connected as a two-terminal device and biased like a zener diode. The circuit is shown in Figure 6. $+V_S$ and V_{OUT} are connected to the system's analog ground, and the AD581's GND pin is connected, through a resistor, to the negative supply. With 1mA flowing in the reference, the output voltage is typically 2mV greater than what is obtained with the conventional, positive, hook-up.

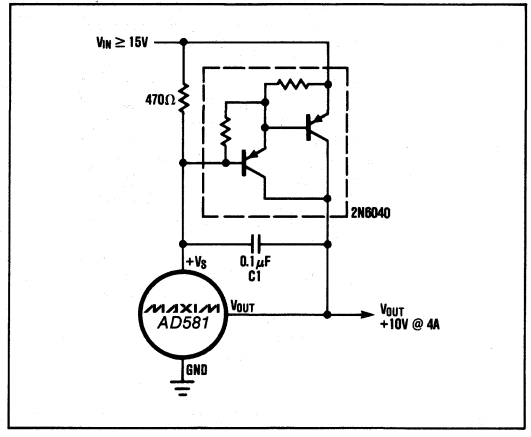


Figure 3. High Current Precision Supply

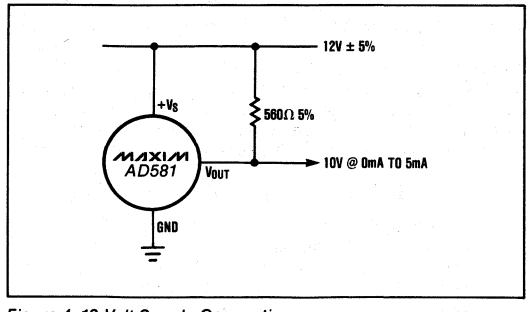


Figure 4. 12-Volt Supply Connection

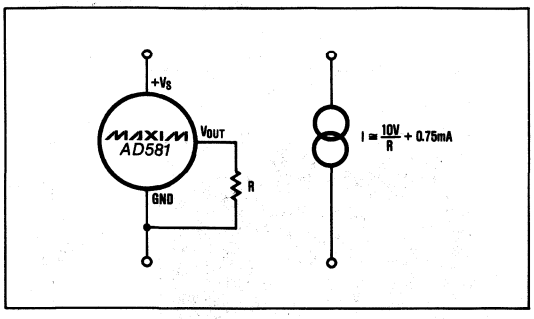


Figure 5. A Two-Component Precision Current Limiter

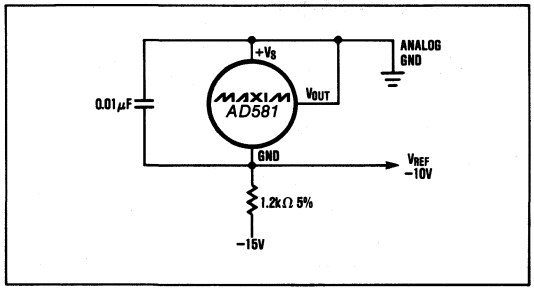


Figure 6. Two-Terminal -10 Volt Reference

When using the 2-terminal connection, the load and the bias resistor must be selected so that the current flowing in the reference is maintained between 1mA and 5mA. The operating temperature range for this connection is limited to -55° to +85°C.

Reference for CMOS DACs and ADCs

The AD581 is well suited for use with a wide variety of D-to-A converters, especially CMOS DACs. Figure 7 shows a circuit in which an AD7533 10 bit DAC outputs 0 to -10V when using a +10V reference. For a positive DAC output, the AD581 is configured as a 2-terminal -10V reference (Figure 6) and connected to the DAC's V_{REF} input.

In Figure 8, an AD7574 CMOS A/D converter uses an AD581 for its -10V reference input. The input range for the A/D converter is 0V to +10V.

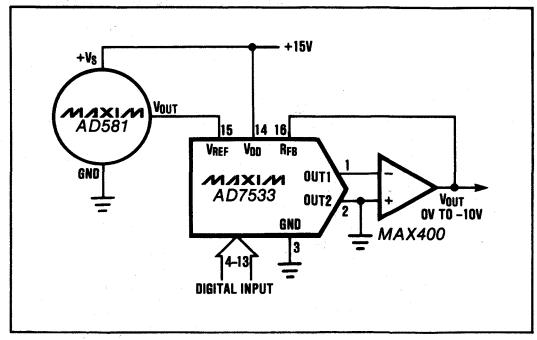


Figure 7. Low Power 10 Bit CMOS DAC Connection

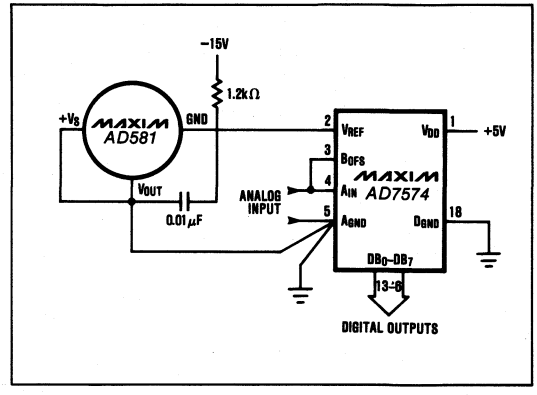


Figure 8. Negative 10V Reference for CMOS A/D Converter

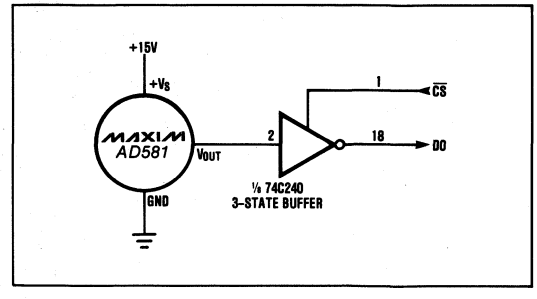
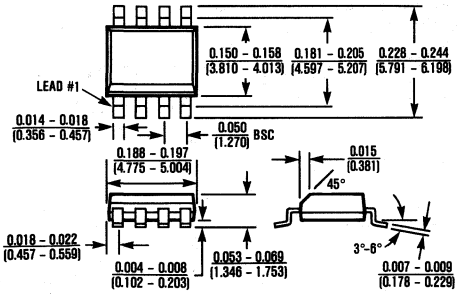


Figure 9. AD581 Microprocessor Interface

High Precision 10 Volt Reference

Package Information

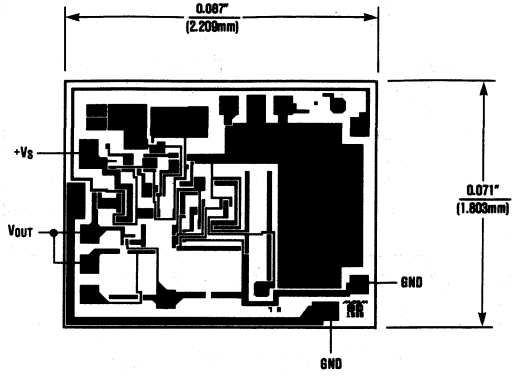


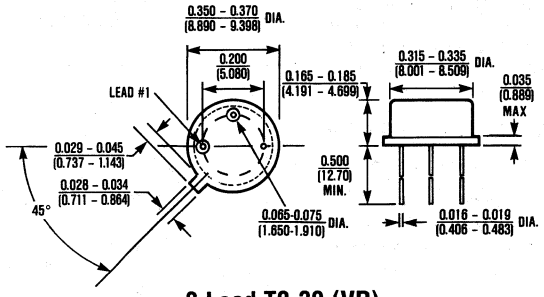
8 Lead Small Outline (SA)

θ_{JA} = 170°C/W

θ_{JC} = 80°C/W

Chip Topography





3 Lead TO-39 (VR)

θ_{JA} = 150°C/W

θ_{JC} = 15°C/W

MAXIM

Pin Programmable Precision Voltage Reference

General Description

Maxim's AD584 is a temperature compensated, bandgap voltage reference which provides pin-programmable output voltages of +10.00V, +7.50V. +5.00V, and +2.50V. External components are not required for these outputs, but if other voltages are desired, they can be programmed with external resistors. Laser trimming minimizes output error as well as temperature drift, to as low as 5mV and 5ppm/°C with the AD584L.

The input voltage range of the AD584 is 4.5V to 30V. The reference also includes a STROBE input which shuts down the reference output. Typical current drain when ON is 750μA. This drops to about 100μA when the reference is strobed OFF.

The AD584 is designed for use with 8 to 14 bit A/D and D/A converters as well as data acquisition systems. It is available in 8-lead TO-99 metal cans, plastic DIPs, CERDIPs, and small outline packages.

Applications

CMOS DAC Reference
A/D Converter Reference
Measurement Instrumentation
Data Loggers
Precision Analog Systems
Programmable Offset for PGAs

Features

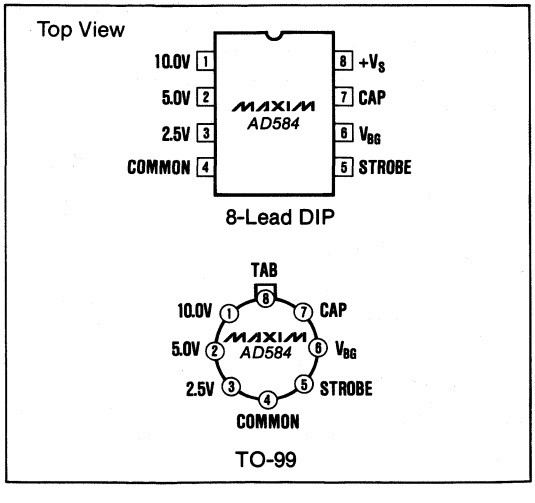
- **Programmable Outputs of: +10.0V, +7.5V, +5.0V, +2.5V**
- **±5mV Tolerance at +10V (AD584L)**
- **Low Tempco: 5ppm/°C Max. (AD584L)**
- **No External Components or Trims**
- **Short Circuit Proof**
- **Output Sources and Sinks Current**
- **10mA Output Current**

Ordering Information

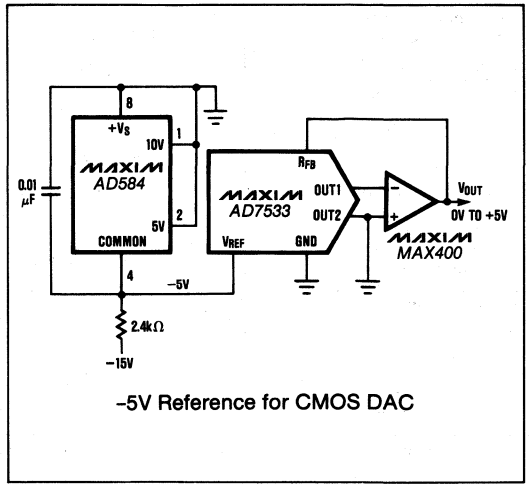
PART	TEMP. RANGE	PACKAGE*	ERROR
AD584JH	0°C to +70°C	TO-99 Can	±30mV
AD584KH	0°C to +70°C	TO-99 Can	±10mV
AD584LH	0°C to +70°C	TO-99 Can	±5mV
AD584JN	0°C to +70°C	Plastic DIP	±30mV
AD584KN	0°C to +70°C	Plastic DIP	±10mV
AD584LN	0°C to +70°C	Plastic DIP	±5mV
AD584JCSA	0°C to +70°C	Small Outline	±30mV
AD584KCSA	0°C to +70°C	Small Outline	±10mV
AD584LCSA	0°C to +70°C	Small Outline	±5mV
AD584JC/D	0°C to +70°C	Dice	±30mV
AD584SH	-55°C to +125°C	TO-99	±30mV
AD584TH	-55°C to +125°C	TO-99	±10mV
AD584SQ	-55°C to +125°C	CERDIP	±30mV
AD584TQ	-55°C to +125°C	CERDIP	±10mV

** All devices — 8 Lead Packages*

Pin Configuration



Typical Operating Circuit



Pin Programmable Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Common ..... -0.3V, +40V
Power Dissipation
- Metal Can (Derate 6.7mW/ above +60°C) 600mW
- CERDIP (Derate 8mW/ above +75°C) 600mW
- Plastic DIP (Derate 6mW/ above +75°C) 450mW
- Small Outline (Derate 5.3mW/ above +75°C) 400mW

Output Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range
- Commercial (J, K, L) ..... 0°C to +70°C
- Military (S, T, U) ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10sec) ..... +300°C
Dice Junction Temperature (T_J) ..... -55°C to +150°C
Thermal Resistance, Junction to Ambient
- Metal Can ..... 150°C/W
- CERDIP ..... 125°C/W
- Plastic DIP ..... 160°C/W
- Small Outline ..... 170°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

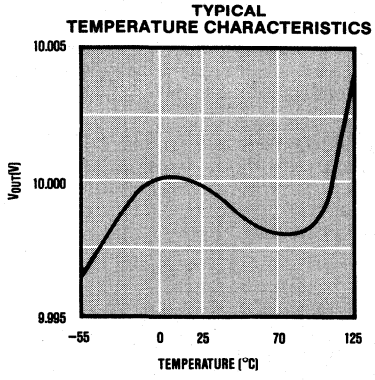
(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

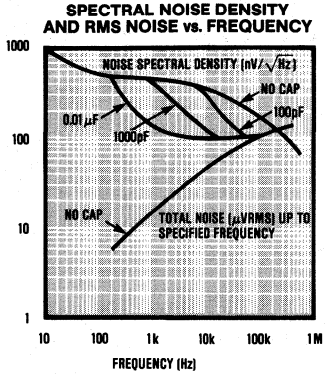
PARAMETER		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Output Voltage Tolerance			I_L = 0mA, At Pin 1	V_{OUT} = +10V, AD584J/S			±30	mV
				AD584K/T			±10	
				AD584L			±5	
				V_{OUT} = +7.5V, AD584J/S			±22	
				AD584K/T			±8	
				AD584L			±4	
				V_{OUT} = +5.0V, AD584J/S			±15	
				AD584K/T			±6	
				AD584L			±3	
				V_{OUT} = +2.5V, AD584J/S			±7.5	
				AD584K/T			±3.5	
				AD584L			±2.5	
Output Voltage Temperature Coefficient			AD584L, +10V, +7.5V, +5V Out				5	ppm/°C
			+2.5V Out				10	
			AD584J/S, All Outputs				30	
			AD584K, All Outputs				15	
			AD584T, +10V, +7.5V, +5V Out				15	
			+2.5V Out				20	
Differential Tempco Between Outputs			AD584K/L/T			3		ppm/°C
			AD584J/S			5		
Quiescent Supply Current		I_Q	I_L = 0mA			750	1000	µA
Quiescent Current Tempco						1.5		µA/°C
Turn-on Settling Time		t_{ON}	To ±1%			200		µs
Noise		e_{NP-P}	0.1Hz to 10Hz			50		μV_{P-P}
Long-Term Stability			(Non-Cumulative)			25		ppm/ kHrs
Short Circuit Current		I_{SC}				30		mA
Line Regulation			No Load, (V_{OUT} + 2.5V) < V_{IN} < +15V			0.005		%/V
			+15V < V_{IN} < +30V			0.002		
Load Regulation			I_L = 0mA to 5mA			20	50	ppm/mA
Output Current	Source	I_L	V_{IN} > V_{OUT} +2.5V	T_A = +25°C	10			mA
				T_{MIN} to T_{MAX}	5			
	Sink			T_{MIN} to T_{MAX}, AD584J/K/L	5			
				AD584S/T	0.2			
				-55°C to +85°C, AD584S/T	5			

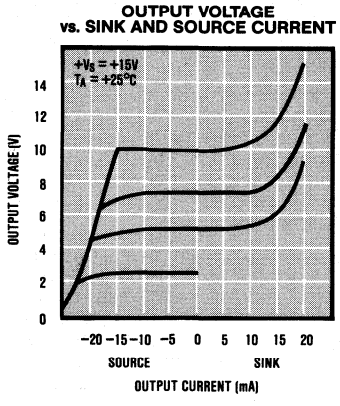
Note 1: Absolute Maximum power dissipation must not be exceeded.

Pin Programmable Precision Voltage Reference

Typical Operating Characteristics







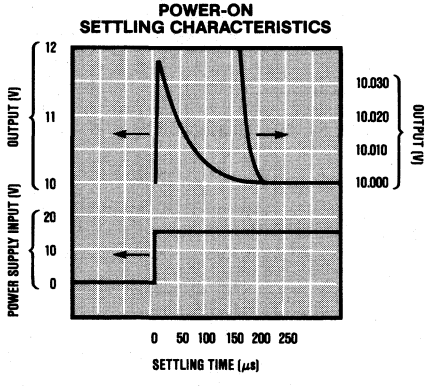


Table 1. Programming Pin Connections

OUTPUT VOLTAGE	PROGRAMMING (OUTPUT ON PIN 1)
10V	Pins 2 and 3 are unconnected.
7.5V	Connect pins 2 and 3 together.
5.0V	Connect pins 2 and 1 together.
2.5V	Connect pins 3 and 1 together.

Detailed Description

As shown in Figure 1, most applications of the AD584 require no external components. Connections to $+V_S$, and COMMON (COMMON is also tied to the case in the TO-99 metal package) with all other pins unconnected result in a buffered +10.00V output at pin 1. The other pretrimmed voltages are obtained by strapping pins as shown in Table 1. If one or more external buffer amplifiers are connected to the programming pins (pin 2,3), multiple outputs can be obtained from one reference.

Other Output Voltages

The AD584 can be adjusted to a different output voltage by adding one or more resistors as in Figure 2. As the diagram shows, the reference can be thought of as a 1.215V band-gap followed by a noninverting amplifier. If R1 and R2 are used alone, the adjustment range is widest but the resolution of the trim may be too coarse, even when a muti-turn trim pot is used.

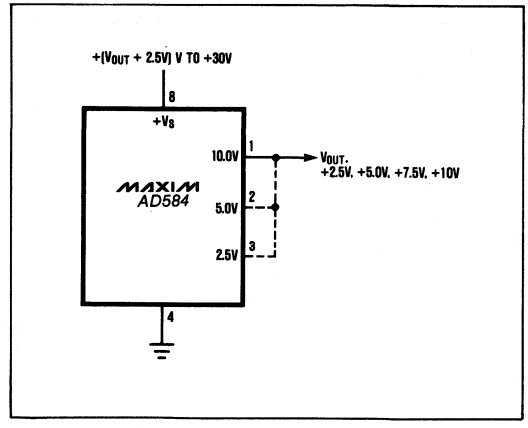


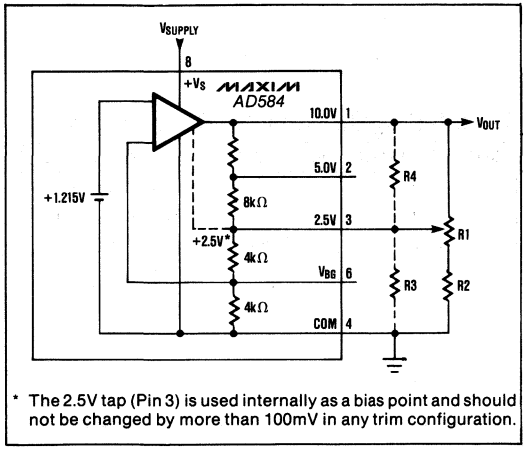
Figure 1. Basic Connection for Positive Outputs

Pin Programmable Precision Voltage Reference

When adding external resistors, output voltages well above 10V can be obtained. R2 should therefore be chosen carefully since it sets the maximum output voltage. R2's resistance should not be so low as to jeopardized other circuits if R1 is misadjusted.

The fixed output voltages can also be varied by connecting only one resistor, as in the dashed lines in Figure 2. Connecting R3 alone raises V_{OUT} while R4 alone lowers it. These resistors (or potentiometers) must have very low temperature coefficients if accuracy over temperature is to be unaffected by the adjustment.

If fine adjustment of the output is all that is required, the circuit of Figure 3 is recommended. It provides good stability and resolution for a trim range of ±200mV. If the 2.5V output is adjusted, R2 should be connected to V_{BG}, pin 6, and the trim range should be limited to ±100mV.



* The 2.5V tap (Pin 3) is used internally as a bias point and should not be changed by more than 100mV in any trim configuration.

Figure 2. Variable Output Options

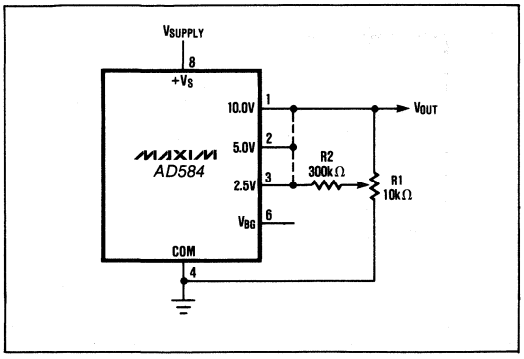


Figure 3. Fine Adjustment of Output Voltage (±200mV)

Voltage Temperature Coefficient

The temperature characteristic of the AD584 consistently follows an "S-curve" as shown in the Typical Charcteristics. A five-point 100% test guarantees compliance with -55°C to +125°C specifications and a three-point 100% test guarantees the 0°C to +70°C specifications.

The tolerance specifications in the Electrical Characteristics table state the maximum deviation from the reference's initial value at 25°C. By adding the maximum deviation for a given device to its initial tolerance, the total possible error is determined.

Output Current

The AD584 is capable of sinking as well as sourcing current. The circuit is also protected for output shorts to either $+V_S$ or ground (COMMON). The output's voltage-versus-current characteristic is shown in the Typical Characteristics section.

Dynamic Performance

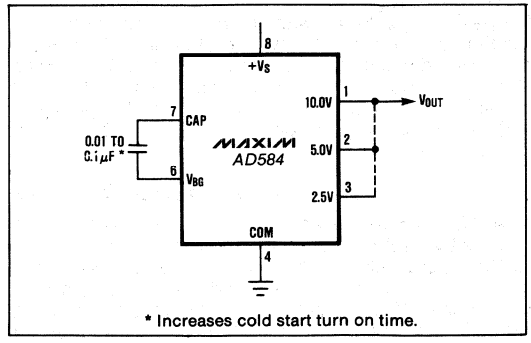
The turn-on settling performance of the AD584 is shown in the Typical Characteristics. Both coarse and fine transient response is shown. The reference typically settles to 1mV (10V output) within 180μs after power is applied.

Noise Filtering

The bandwidth of the AD584's output amplifier can be limited by connecting a capacitor between the CAP and V_{BG} pins (see Figure 4). Typical values range from 0.01μF to 0.1μF. The reduction of wideband and feedthrough noise is plotted in a graph in the Typical Characteristics section.

Strobe Input

The STROBE input, pin 5, zeroes the reference output when it is pulled LOW. If no current is pulled from STROBE, operation is normal. The threshold of the input is 200mV, so an open-drain N-channel FET or open-collector transistor driven from logic is re-



* Increases cold start turn on time.

Figure 4. Additional Noise Filtering with an External Capacitor

Pin Programmable Precision Voltage Reference

commended (see Figure 5). The current sinking ability should be at least 500μA and the leakage current should be 5μA or less. While shut down, the AD584 should not be required to source or sink current unless a 0.7V residual output is acceptable. If the reference is required to sink transient current while shut down, the current flowing out of STROBE should be limited with 100Ω as shown in the dashed connection in Figure 5.

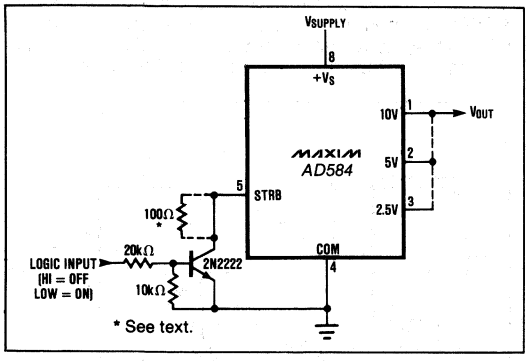


Figure 5. Use of Strobe Terminal

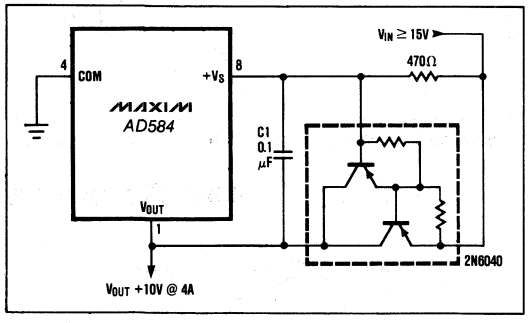


Figure 6. High Current Precision Supply

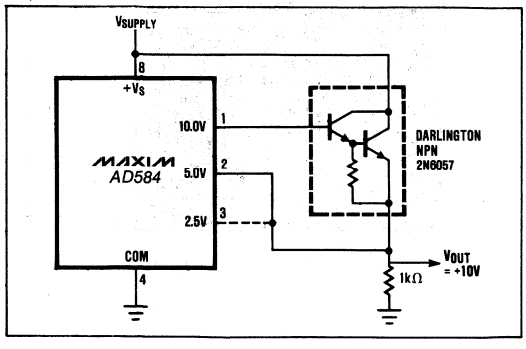


Figure 7. NPN Output Current Booster

Applications

Precision High Current Reference

A PNP power transistor, or Darlington, is easily connected to the AD584 to greatly increase its output current. The circuit in Figure 6 provides a +10V output at up to 4 Amps. If the load has a significant capacitive component, C1 should be added. If the load is purely resistive, high frequency supply rejection is improved without C1. An NPN output transistor or Darlinton can also be used to boost output current as shown in Figure 7.

Current Limiter

By adding a single resistor as shown in Figure 8, the AD584 is turned into a precision current limiter for applications where the driving voltage is 5V to 40V. The programmed current ranges from 0.75mA to 5mA.

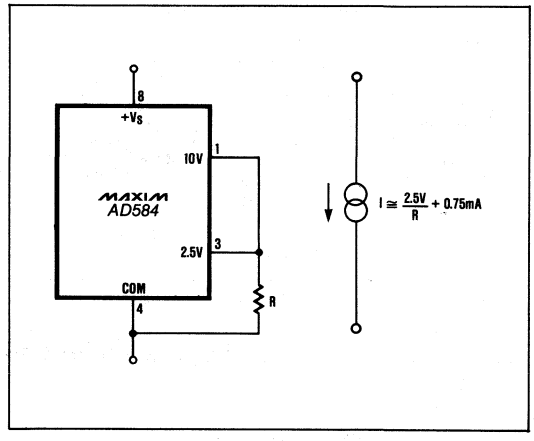


Figure 8. Precision Current Limiter

Negative 10V Reference

In applications which require a -10V, -7.5V, -5.0V, or -2.5V reference, the AD584 can be connected as a two-terminal device and biased like a zener diode. The circuit is shown in Figure 9. $+V_S$ and V_{OUT} are connected to the analog ground bus, and the AD584's COMMON pin is connected, through a resistor, to the negative supply. With 1mA flowing in the reference, the output is typically 2mV greater than what is obtained with a conventional, positive, hook-up.

When using the 2-terminal connection, the load and the bias resistor must be selected so that the current flowing in the reference is maintained between 1mA and 5mA. The operating temperature range for this connection is limited to -55° to +85°C.

Pin Programmable Precision Voltage Reference

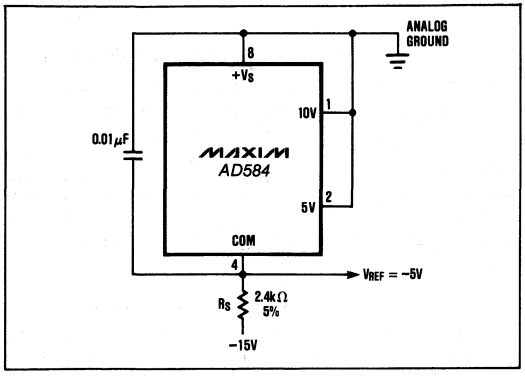


Figure 9. Two-Terminal -5 Volt Reference

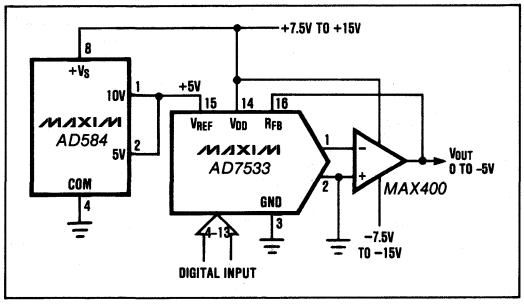


Figure 10. Low Power 10 Bit CMOS DAC Connection

Reference for DACs and ADCs

The AD584 is well suited for use with a wide variety of D-to-A converters, especially CMOS DACs. Figure 10 shows a circuit in which an AD7533 10 bit DAC outputs 0 to -5V when using a +5V reference. For a positive DAC output, the AD584 can be configured as a 2-terminal negative reference as well by using the connection of Figure 9.

In Figure 11, an AD7574 CMOS A/D converter uses an AD584, connected for -2.5V, as its reference input so that the system can operate from ±5V power. The analog input range for the circuit is 0V to +2.5V.

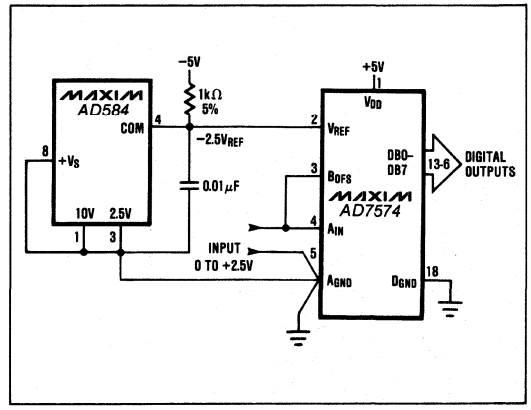
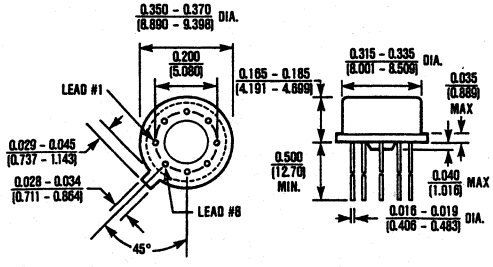


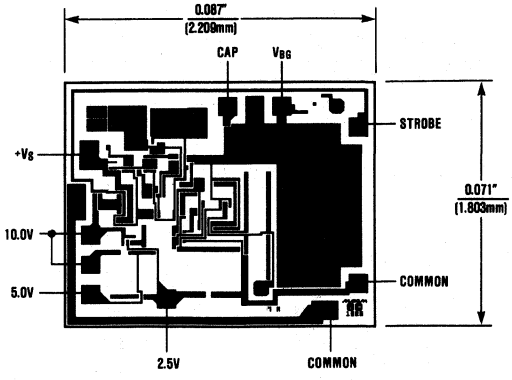
Figure 11. AD584 as Negative 2.5 Volt Reference for a CMOS ADC

Package Information



8 Lead TO-99 (TV)
θ_{JA} = 150°C/W
θ_{JA} = 45°C/W

Chip Topography



10 Volt Precision References

General Description

The AD2700 series of precision 10 volt reference sources offers excellent accuracy and stability. Laser trimming of both initial accuracy and temperature drift ensures high precision over the commercial (0°C to +70°C), industrial (-25°C to +85°C) and military (-55°C to +125°C) temperature ranges. The guaranteed absolute accuracy allows the user to configure systems without the need for ovens or chip heaters for temperature regulation. The AD2700 is a +10 volt output reference while the AD2701 is a -10 volt output. Both devices are guaranteed to 3ppm/°C max with 2.5mV initial accuracy. The AD2710, with a +10 volt output, is guaranteed to 1ppm/°C max with 1mV initial accuracy. These products are designed to interface with high accuracy, high resolution A to D and D to A converters, precision instrumentation, and data acquisition systems.

Applications

Precision D/A and A/D Converter Reference
Digital Voltmeters
Precision Test and Measurement Systems
Precision Calibrated Voltage Reference Standard
High Accuracy Transducers

Features

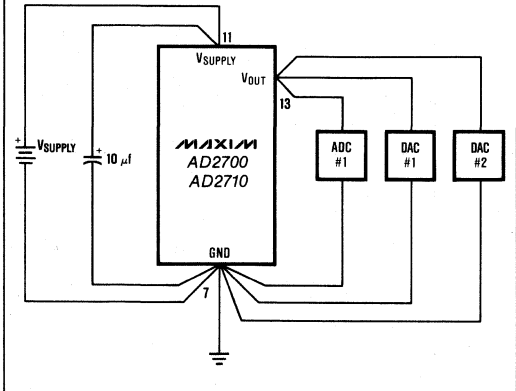
- **Pin-for-Pin 2nd Source!**
- **Excellent Initial Accuracy**
- **Low Temperature Coefficient**
- **Excellent Long-Term Stability, 50ppm/1000hrs.**
- **10mA Output Current Capability**
- **Superior Line Regulation: 100μV/V max.**
- **Standard Ceramic Side Brazed DIP**

Ordering Information

PART	OUTPUT VOLTAGE	TEMP. RANGE
AD2700JD	+10V, 10 ppm/°C	-25°C to +85°C
AD2700LD	+10V, 3 ppm/°C	-25°C to +85°C
AD2700SD	+10V, 3 ppm/°C	-55°C to +125°C
AD2700UD	+10V, 3 ppm/°C	-55°C to +125°C
AD2701JD	-10V, 10 ppm/°C	-25°C to +85°C
AD2701LD	-10V, 3 ppm/°C	-25°C to +85°C
AD2701SD	-10V, 3 ppm/°C	-55°C to +125°C
AD2701UD	-10V, 3 ppm/°C	-55°C to +125°C
AD2710LD	+10V, 1 ppm/°C	0°C to +70°C
AD2710KD	+10V, 2 ppm/°C	0°C to +70°C

All devices are available in a 14 lead ceramic side brazed DIP.

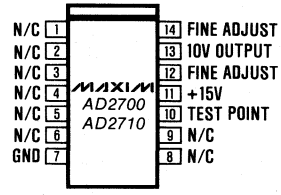
Typical Operating Circuit

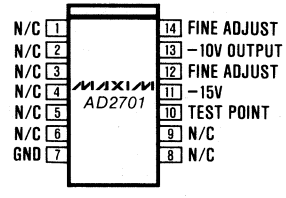


Precision +10V System Reference

Pin Configuration

Top View





10 Volt Precision References

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... +20V
Power Dissipation 400mW
Operating Temperature Range
AD2700JD, LD, AD2701JD, LD ..... -25°C to +85°C
AD2700SD, UD, AD2701SD, UD ..... -55°C to +125°C
AD2710KD, LD ..... 0°C to +70°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature ..... +300°C
(soldering, 10 seconds)
Short Circuit to GND ..... Continuous

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V for AD2700 and AD2710, V_{IN} = -15V for AD2701, T_A = +25°C, R_L = 2kΩ, unless otherwise noted)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Initial Output Voltage	AD2700JD, SD	9.9950	10.0000	10.0050	V
	AD2700LD, UD	9.9975	10.0000	10.0025	V
	AD2701JD, SD	-10.0050	-10.0000	-9.9950	V
	AD2701LD, UD	-10.0025	-10.0000	-9.9975	V
	AD2710KD, LD	9.9990	10.0000	10.0010	V
Output Voltage Drift	AD2700,01JD $T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
	AD2700,01LD, SD, UD $T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
	AD2710KD T_A = +25°C to +70°C			2	ppm/°C
	AD2710LD T_A = +25°C to +70°C			1	ppm/°C
	AD2710KD T_A = 0°C to +25°C			5	ppm/°C
	AD2710LD T_A = 15°C to +25°C			2	ppm/°C
	AD2710LD T_A = 0°C to +15°C			5	ppm/°C
Output Voltage Range	AD2700JD, AD2701JD $T_A = T_{MIN}$ to T_{MAX}			±11.0	mV
	AD2700LD, AD2701LD $T_A = T_{MIN}$ to T_{MAX}			±4.3	mV
	AD2700SD, AD2701SD $T_A = T_{MIN}$ to T_{MAX}			±8.0	mV
	AD2700UD, AD2701UD $T_A = T_{MIN}$ to T_{MAX}			±5.5	mV
Output Current	T_A = 25° C, for Specified Load Regulation			10	mA
	$T_A = T_{MIN}$ to T_{MAX} V_{IN} = +13V to +18V (2700, 2710) V_{IN} = -13V to -18V (2701)			5	mA
Line Regulation	V_{IN} = +13.5V to +16.5V (2700, 2710)			100	μV/V
	V_{IN} = -13.5V to -16.5V (2701)			100	μV/V
Load Regulation	0 to 10mA to GND			50	μV/mA
Output Resistance	0 to 10mA to GND			0.05	Ω
Input Voltage Range	AD2700, AD2710	+13		+18	V
	AD2701	-13		-18	V
Quiescent Current	No Load		9	14	mA
Noise (Note 1)	0.1 to 10Hz		6	50	μV_{P-P}
Long Term Stability	T_A = +55°C		50		ppm/1000 hrs.
Output Adjust Range	See Figure 1 and 2		±20		mV
Output Adjust Temperature Drift Effect			±4		μV/°C per mV of adjust

Note 1: QA sample tested.

Theory of Operation

A zener voltage of approximately 6.3V is applied to the non-inverting input of an operational amplifier. This voltage is accurately amplified to produce a precise 10.000V output. The amplifier's gain setting resistors are actively laser-trimmed to produce the desired output voltage. The zener operating current is derived from the regulated output voltage, and actively laser-trimmed to produce the lowest drift over temperature at the output of the amplifier.

Discussion of Performance

The Maxim AD2700 and AD2701 are designed for applications requiring a precision voltage reference, where initial accuracy at room temperature and drift over temperature are of prime importance.

The drift specification of the AD2700 and AD2701 are guaranteed by making precise voltage measurements at -55°C, -25°C, +25°C, +85°C, and -125°C, while maintaining unit identity. In this way, three key specifications are guaranteed: initial accuracy, absolute accuracy over temperature, and drift. The upper and lower bound limits of absolute accuracy over temperature are established by the sum of the maximum initial output voltage error and the maximum drift from +25°C to T_{MAX}. For example, the AD2700LD limit of 4.3mV is calculated from the addition of 2.5mV initial output voltage error plus the temperature drift error of 1.8mV [3ppm/°C x 10V x (85°C - 25°C)].

The drift specification is defined using the "box method" (Fig. 3). The "box" is formed by the T_{MAX} and T_{MIN} temperatures and a diagonal with a slope equal to the maximum specified drift. The maximum and minimum output voltages must meet the following conditions:

$$\frac{(V_{OUTMAX} - V_{OUTMIN})/10V}{T_{MAX} - T_{MIN}} \times 10^6 \leq \text{drift specification}$$

This assures that the output voltage variation over the temperature change is contained within the box with V_{OUTMAX} and V_{OUTMIN} limits.

For example, the AD2700LD maximum drift specification of 3ppm/°C from -25°C to +85°C restricts (V_{OUTMAX} - V_{OUTMIN}) to less than 3.3mV.

The AD2710 drift specification is defined over the temperature range of 0°C to +70°C using the "butterfly" method (Fig. 4), where endpoint measurements are tested for temperature coefficient from 25°C independent of the nominal voltage. Each device is tested at 0°C, +15°C, +25°C, and +70°C with the output voltage data recorded at each temperature. After the initial accuracy is checked for 1mV deviation from +10.000V at +25°C, the devices are graded according to temperature coefficient (TC). The AD2710K has a temperature coefficient less than or equal to 2ppm/°C from +25°C to +70°C and 5ppm/°C from 0°C to +25°C. These temperature coefficients correspond to a maximum change of 0.45mV and 1.25mV respectively (see Fig. 4a).

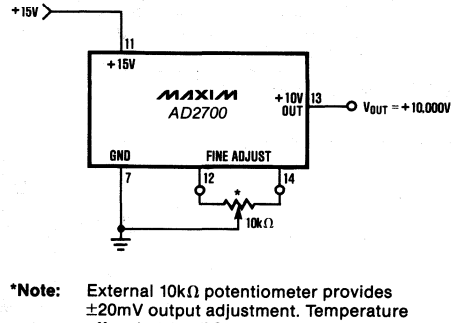
$$10V \times (V_{70°C} - V_{25°C}) \times 2\times10^{-6} = 0.45mV$$
$$10V \times (V_{25°C} - V_{0°C}) \times 5\times10^{-6} = 1.25mV$$

Similarly, the AD2710L is tested for 1ppm/°C from +25°C to +70°C, 2ppm/°C from +15°C to +25°C, and 5ppm/°C from 0°C to +15°C (see Fig. 4b). The corresponding voltage limits are 0.45mV from 25°C to +70°C, 0.2mV from +15°C to +25°C, and 0.75mV from 0°C to +15°C which, when added to the 0.2mV at +15°C, allows for 0.95mV change at 0°C.

Application Information

The Typical Operating Circuit shown on the front page shows the proper connection for the AD2700/2710. Special attention to layout is required to achieve the specified performance. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply.

The output voltage of the AD2700 and AD2710 can be trimmed, as shown in Figure 1, by connecting an external potentiometer between pins 12 and 14 with the wiper connected to ground. This external potentiometer provides typically ±20mV of output adjustment. The voltage drift will change by approximately 0.4ppm/°C (or 4μV/°C) per mV of adjustment.



*Note: External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.

Figure 1. Fine Trim Connection, AD2700 and AD2710

10 Volt Precision References

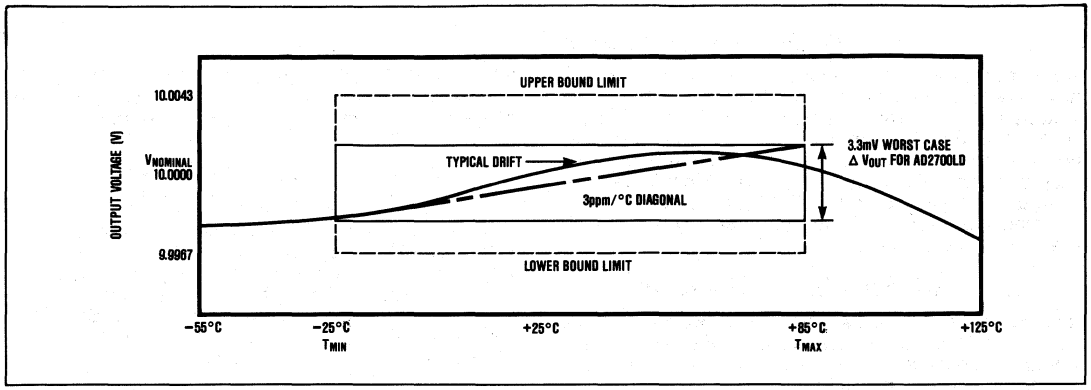
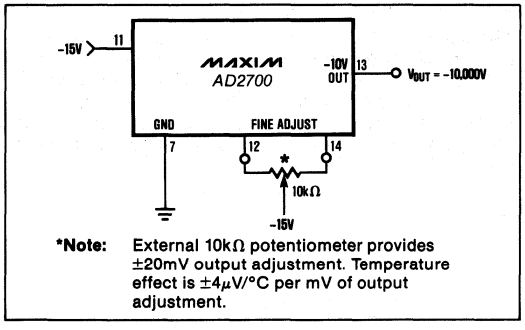


Figure 3. AD2700 Output Voltage Drift

The fine trim adjustment of the AD2701 is achieved by connecting the wiper of the potentiometer to V⁻, as shown in Figure 2.



***Note:** External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.

Figure 2. Fine Trim Connection, AD2701

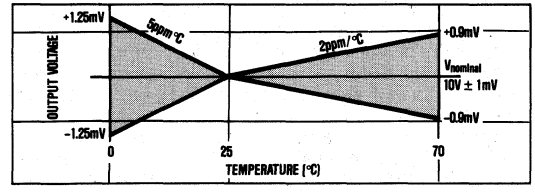


Figure 4a. AD2710K Output Voltage Drift

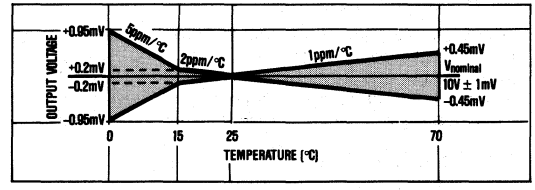
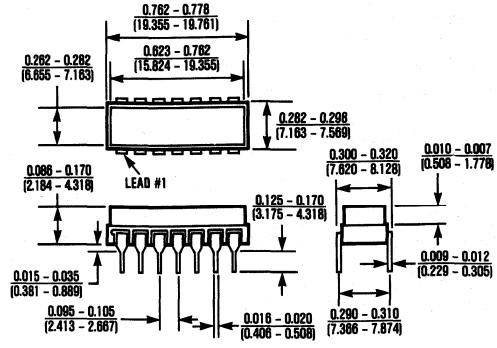


Figure 4b. AD2710L Output Voltage Drift

Package Information



14 Lead HYBRID
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W

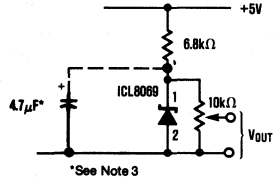
General Description

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Maxim's ICL8069 also features excellent stability, freedom from oscillation.

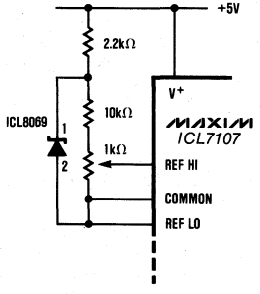
Applications

Analog to Digital Converters
Digital to Analog Converters
Threshold Detectors
Voltage Regulators
Portable Instruments

Typical Operating Circuits



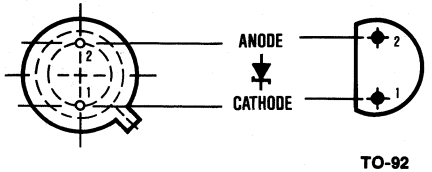
(a) Simple Reference (1.2 Volts or Less)



(b) Double Regulated 100mV Reference for ICL7107 One-Chip DPM Circuit.

Pin Configuration

Bottom View



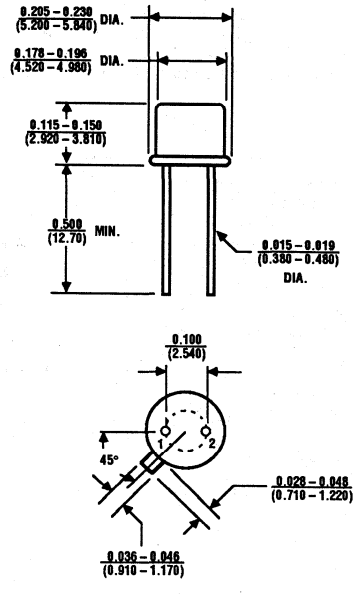
Features

- **Temperature Coefficient Guaranteed to 10ppm/°C Max.**
- **Low Bias Current . . . 50 μA Min.**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

Ordering Information

PART	TEMP. STABILITY	TEMP. RANGE
TO-92 Plastic:		
ICL8069CCZQ2	0.005%/°C	0°C to +70°C
ICL8069DCZQ2	0.01%/°C	0°C to +70°C
TO-52 Can:		
ICL8069ACSQ2	0.001%/°C	0°C to +70°C
ICL8069BCSQ2	0.0025%/°C	0°C to +70°C
ICL8069CCSQ2	0.005%/°C	0°C to +70°C
ICL8069DCSQ2	0.01%/°C	0°C to +70°C
ICL8069CMSQ2	0.005%/°C	-55°C to +125°C
ICL8069DMSQ2	0.01%/°C	-55°C to +125°C

Package Information



2 Lead TO-52
Can (SQ)

Low Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 1
Forward Current 10mA
Reverse Current 10mA
Power Dissipation .... Limited by Max Forward/Reverse Current
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... -55°C to +125°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse Breakdown Voltage Change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse Dynamic Impedance	I_R = 50μA I_R = 500μA		1 0.6	2 2	Ω
Forward Voltage Drop	I_F = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Breakdown Voltage Temperature Coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	I_R = 500μA T_A = Operating Temperature Range (Note 2)			 .001 .0025 .005 .01	%/°C
Reverse Current Range		.050		5	mA

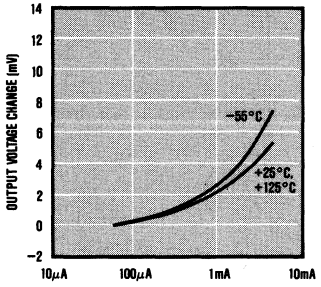
Note 1: In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.

Note 2: For the military devices, measurements are made at 25°C, -55°C, and 125°C, while for the commercial devices measurements are made at 25°C, 0°C and 70°C. The unit is then classified as a function of the worst case TC. Sample tested to 0.1% AQL.

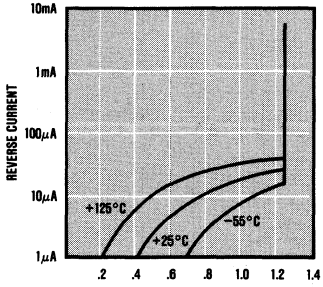
Note 3: If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.

Typical Operating Characteristics

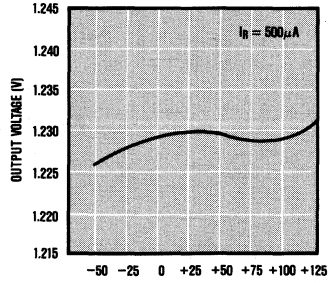
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



MAXIM

+5V, +10V Precision Voltage References

General Description

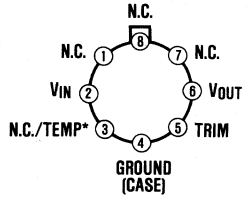
The REF01 and REF02 are precision voltages references that are pretrimmed to within ±.3% of 10V and 5V respectively. Both references feature excellent temperature stability (as low as 8.5 ppm/°C worst case), low current drain and low noise. The REF02 also provides a TEMP pin whose output voltage varies linearly with temperature, making this device suitable for a wide variety of temperature sensing and control applications. Both devices are available from Maxim in the space-saving Small Outline package, as well as the standard 8 pin TO-99 and MINI-DIP packages.

Applications

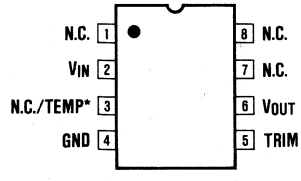
A to D Converters
D to A Converters
Digital Voltmeters
Voltage Regulators
Threshold Detectors

Pin Configuration

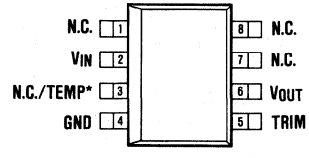
Top View



8 Lead TO-99 Metal Can



8 Lead DIP



8 Lead Small Outline

***NOTE:** Pin 3 is N.C. (No Connection) on REF01, TEMP Output on REF02

Features

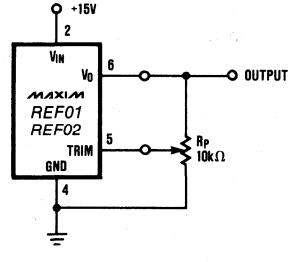
- **Pretrimmed to +5V, +10V ±0.3%**
- **Excellent Temperature Stability: 3ppm/°C**
- **Low Noise: 10μV_{p-p} (REF02)**
- **Low Supply Current: 1.4mA Max**
- **Short Circuit Proof**
- **Linear Temperature Transducer O/P (REF02)**

Ordering Information

PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C		
REF01EJ	10V ± 30mV	TO-99
REF01HJ	10V ± 50mV	TO-99
REF01CJ	10V ± 100mV	TO-99
REF01EZ	10V ± 30mV	Hermetic DIP
REF01HZ	10V ± 50mV	Hermetic DIP
REF01CZ	10V ± 100mV	Hermetic DIP
REF01HP	10V ± 50mV	Plastic DIP
REF01CP	10V ± 100mV	Plastic DIP
REF01HCSA	10V ± 50mV	Small Outline
REF01CCSA	10V ± 100mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
REF01AJ	10V ± 30mV	TO-99
REF01J	10V ± 50mV	TO-99
REF01AZ	10V ± 30mV	Hermetic DIP
REF01Z	10V ± 50mV	Hermetic DIP

(Ordering information continued on last page.)

Typical Operating Circuit



Reference with Trimmed Output

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF01

Input Voltage
- REF01, A, E, H, All DICE 40V
- REF01C 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF01A, REF01 ..... -55°C to +125°C
- REF01E, REF01H, REF01C ..... 0°C to +70°C

DICE Junction Temperature (T_J) ..... -65°C to +150°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF01A and REF01, 0°C ≤ T_A ≤ +70°C for REF01E and REF01H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

Note 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

Note 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
Note 3: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 4: Line and Load Regulation specifications include the effect of self heating.
Note 5: Sample tested.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 0.006	0.015 0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	ppm/%
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		I_L = 0 to 5mA	—	0.008	0.018	%/mA

Notes: See previous page.

Output Adjustment

The REF01 trim terminal can be used to adjust the voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V, including 10.240V for binary applications (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100mV of output adjustment.

Burn-In Circuit

The burn-in circuit of Figure 1 is used for both the REF01 and the REF02. All Maxim REF01s and REF02s are 100% burned-in for a minimum of 24hrs at 150°C (except for Small Outline package), which is equivalent to 25 years of operation at 25°C. This substantially improves the long term stability of the part, and allows Maxim to offer a product with a F.I.T. rate of better than 10 (See Product Reliability Report RR-1A).

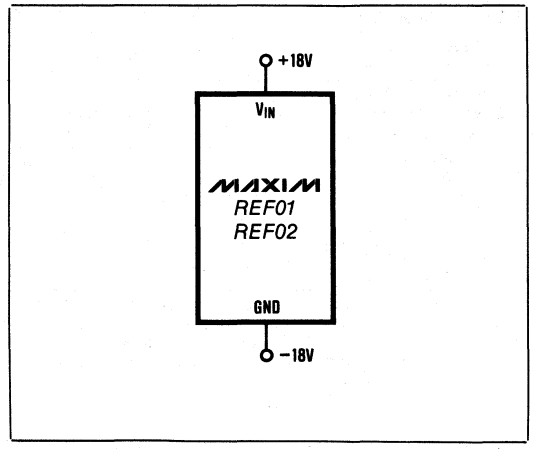


Figure 1. Burn-in circuit

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF02

Input Voltage
- REF02, A, E, H, All DICE 40V
- REF02C, D 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF02A, REF02 ..... -55°C to +125°C
- REF02E, REF02H ..... 0°C to +70°C
- REF02C, REF02D ..... 0°C to +70°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

DICE Junction Temperature (T_j) ..... -65°C to +150°C

Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF02A and REF02, 0°C ≤ T_A ≤ +70°C for REF02E and REF02H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8V to 33V)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Note 1: Line and Load Regulation specifications include the effect of self heating.
Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
Note 3: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

Note 4: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
Note 5: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 1)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 —	0.015 —	— —	— 0.015	— 0.04	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 3 and 4)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 1)		I_L = 0 to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Notes: See previous page.

Output Adjustment

The REF02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Temperature Voltage Output

The REF02 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately 2.1mV/°C (Figure 2).

Output Voltage = 2.1(T + 273)mV
where T = Temperature in °C

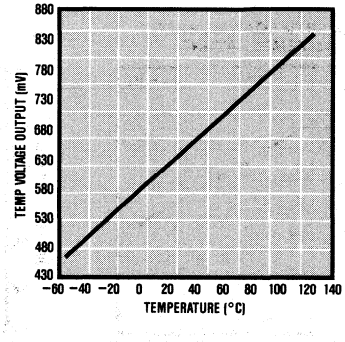
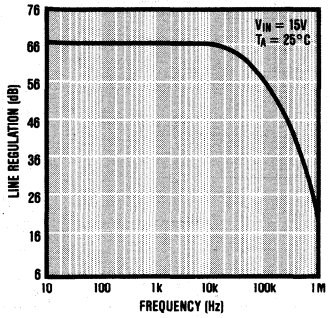


Figure 2. REF02 Temperature Voltage Output vs. Temperature.

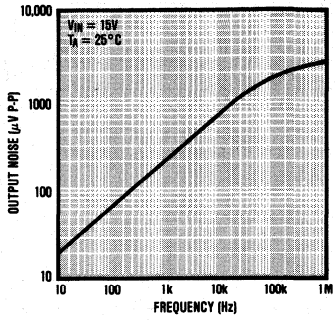
+5V, +10V Precision Voltage References

Typical Operating Characteristics

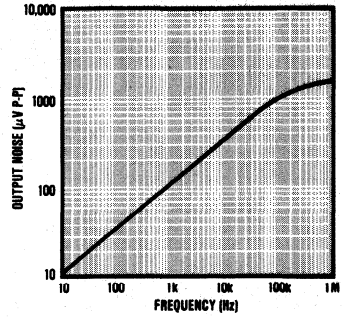
LINE REGULATION vs FREQUENCY



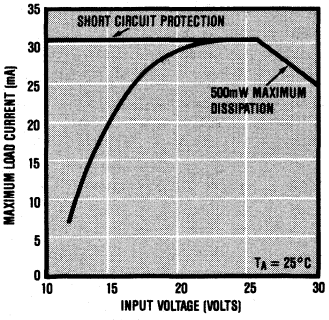
REF01 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



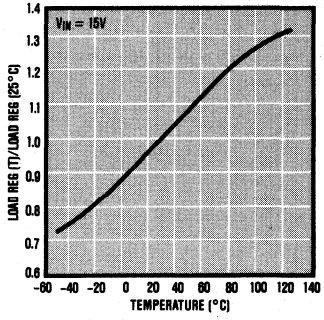
REF02 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



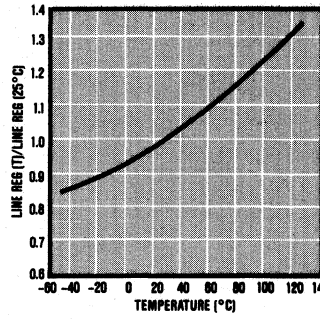
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



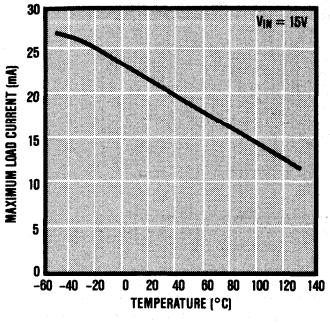
NORMALIZED LOAD REGULATION (ΔI_L = 10 mA) vs TEMPERATURE



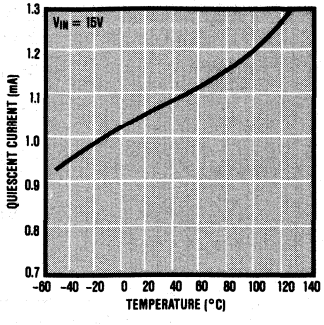
NORMALIZED LINE REGULATION vs TEMPERATURE



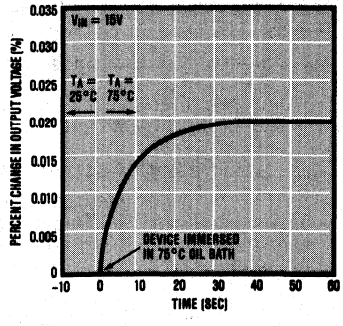
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



OUTPUT CHANGE DUE TO THERMAL SHOCK



Typical Applications

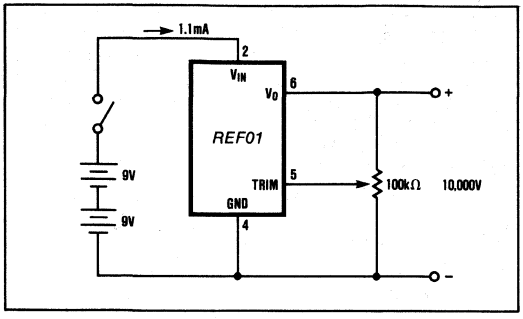


Figure 3. Precision Calibration Standard

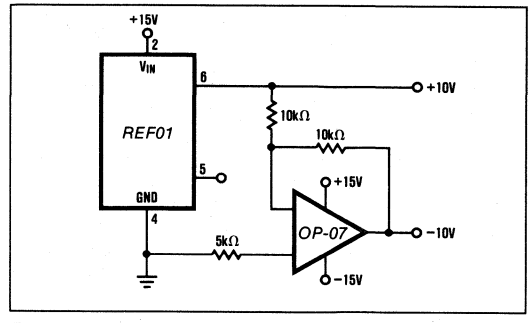


Figure 4. ±10V Reference

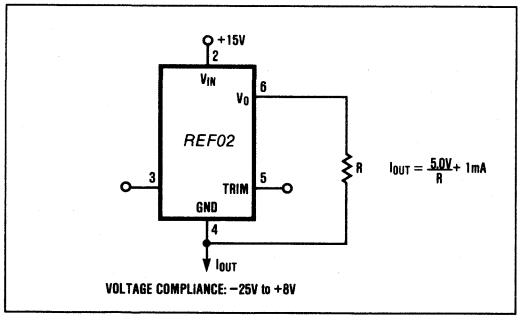


Figure 5. Current Source

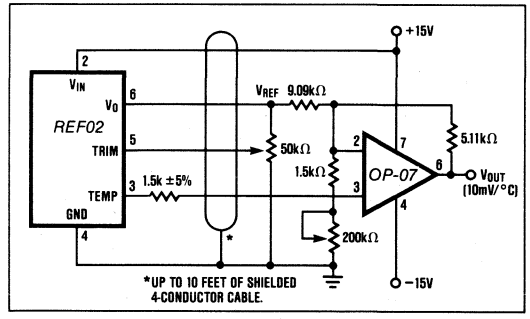
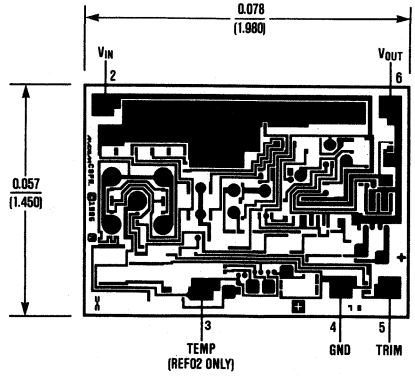


Figure 6. Precision Temperature Transducer with Remote Sensor

Chip Topography



+5V, +10V Precision Voltage References

Ordering Information

(Continued from first page)

PART	V_{OUT} @ 25°C	PACKAGE	PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C			**TEMP RANGE: 0°C TO +70°C**		
REF02EJ	5V ± 15mV	TO-99	REF02DP	5V± 100mV	Plastic DIP
REF02HJ	5V ± 25mV	TO-99	REF02HCSA	5V ± 25mV	Small Outline
REF02CJ	5V ± 50mV	TO-99	REF02CCSA	5V ± 50mV	Small Outline
REF02DJ	5V ± 100mV	TO-99	REF02DCSA	5V ± 100mV	Small Outline
REF02EZ	5V ± 15mV	Hermetic DIP	**TEMP RANGE: -55°C TO +125°C**		
REF02HZ	5V ± 25mV	Hermetic DIP	REF02AJ	5V ± 15mV	TO-99
REF02CZ	5V ± 50mV	Hermetic DIP	REF02J	5V ± 25mV	TO-99
REF02DZ	5V ± 100mV	Hermetic DIP	REF02AZ	5V ± 15mV	Hermetic DIP
REF02HP	5V ± 25mV	Plastic DIP	REF02Z	5V ± 25mV	Hermetic DIP
REF02CP	5V ± 50mV	Plastic DIP			

Appendix

A

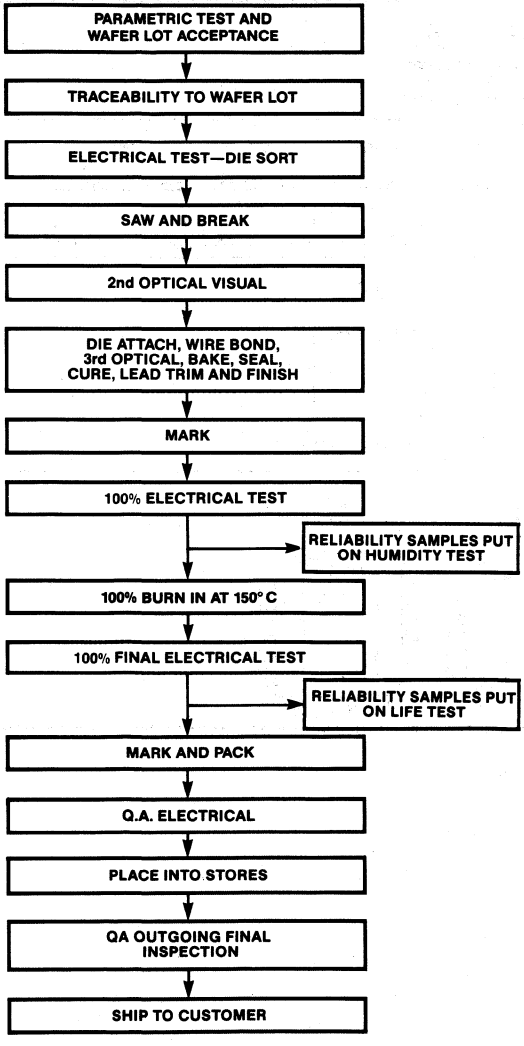
Package Unit Process Flow

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below IpA current levels, and less than IpF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.



Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature.* This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85°C/85%) cycles. In addition, *every unit shipped has been burned-in* (with the exception of reversed lead and Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including a 100% burn-in, at no additional cost.*

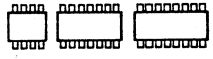
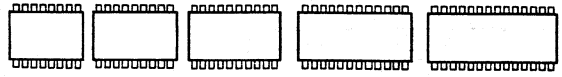
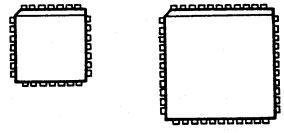
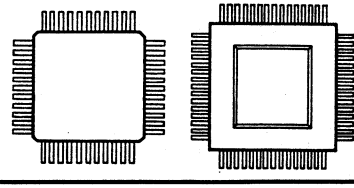
Surface Mount Products

Maxim is committed to providing high-quality, high reliability 8-44 lead plastic surface mount products. These products are processed through the same manufacturing flow as the Dual-in-Line (DIP) plastic parts and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs with the exception of 100% burn-in and cold test. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a Long-term Life Test prior to shipment.

A

Surface Mount Products

Maxim is committed to providing high quality, high reliability 8 to 60 lead plastic surface mount products. With few exceptions, every monolithic product will be offered in a surface mount package. These products are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels, with the exception of 100% burn-in and cold test. They receive the same product conditioning and lot qualification as the DIPs. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a long term life test prior to shipment.

PACKAGE	PKG ALPHA	LEAD COUNTS AVAILABLE
0.150" JEDEC SOIC	S	8 14 16 
0.300" JEDEC SOIC	W	16 18 20 24 28 
QUAD PACK JEDEC PLCC	Q	28 44 
FLAT PACK (PFP) 0.8 mm LEAD CENTERS	M	44 60 

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout as in the 0.300" DIP package equivalents.

0.300" JEDEC SOIC (W) parts also have the same pinout as in the 0.300" DIP package except for selected products in the 16 lead. 14 lead products that are too large for the 0.150" 14 lead (S) package are made available in the 0.300" 16 lead (W) package.

Quad Pack Pin Convention

1.) Devices in the 28 Lead Quad Pack are pin for pin number compatible with the DIP package. That is to say, pin 1 on the 28L Quad will be the same function as pin 1 on the DIP package.

2.) All 40 Lead devices planned for the 44 Lead Quad pack will have the following pin convention:

Flatpack Pin Convention

No fixed convention exists for 40-lead products assembled in either 44-lead or 60-lead flatpack. Consult product marketing for specific pin-outs.

DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#
	1 N/C		12 N/C		23 N/C		34 N/C
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

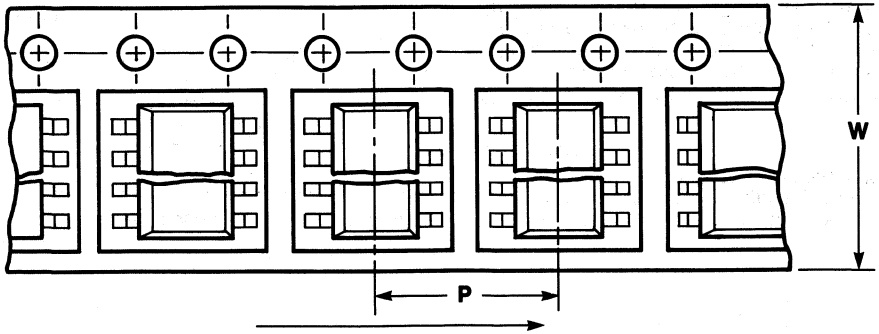
Surface Mount Packages In Reeled Tape

Maxim surface mount packages are normally shipped in antistatic plastic rails. They are also available mounted in pockets on embossed tape for customers using automatic placement systems. The tape is wound and shipped on reels.

The following table and diagrams indicate the tape sizes used for the various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
PFP	44L	24	16
	60L	44	32

SOIC DEVICES



USER DIRECTION OF FEED

A

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow" the standard to ensure lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet 25°C worst case parameters.

Generally, the parameters or parameter limits listed in the packaged unit data sheets are tested during electrical probe. However some parameters are impossible to test or test with absolute accuracy on unassembled product. Information regarding any of these parameters/parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	3"	4"	UNITS
Chip Thickness Backlapped wafers	13 ± 1	15 ± 1	mils
Die length/width tolerance	± 1		mils
Bonding pads dimensions (minimum)	4.0 x 4.0		mils
Bonding pad and interconnect material thickness	10K–15K		A
Storage temperature	-40 to +150		°C
Operating temperature	-20 to +70		°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010.2, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by HF etching or by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

Maxim guarantees die and wafer AQL levels as follows:

Visual 0.65%
Functional Electrical Testing 0.65%
Parametric DC Testing 2.5%
Untested Parameters 6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry ambient—preferably inert gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment or harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Die and wafers are packaged as shown in Figures 1 and 2, respectively.

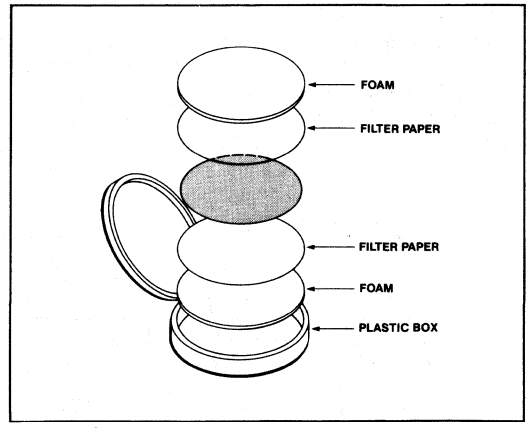


Figure 1. Wafer Carrier Package

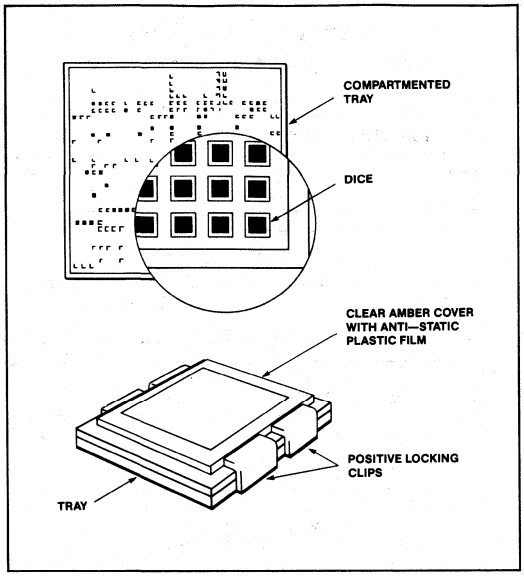


Figure 2. Die Carrier Package

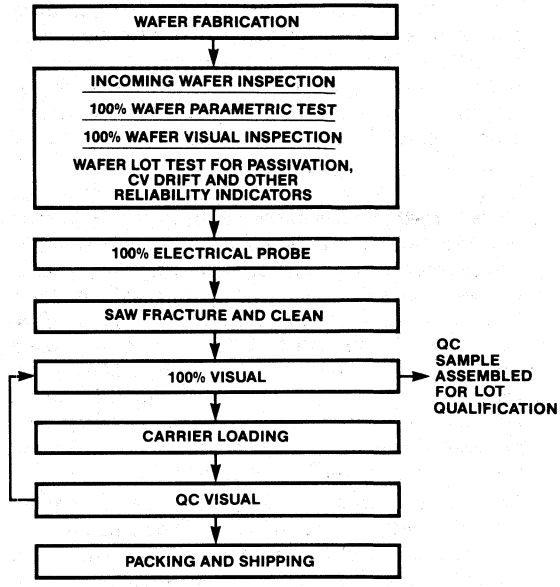
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a /D suffix.
Example: ICL7109C/D

When ordering die in wafer form replace "D" in the part numbers with a "W"
Example: MAX7231C/D Die = MAX7231C/W Wafer.

A

Maxim's /HR Program

Maxim now offers a High Reliability Processing Program that completely emulates ***Rev. B*** of Mil-Std-883, Class B. This program, labeled /HR, produces devices that are tested to operate over the military temperature range and are meticulously processed per established product flows. It is targeted at customers who do not want to pay the cost for certified product in full compliance with ***Rev. C*** of Mil-Std-883, Class B.

In addition to emulating all the manufacturing process steps of method 5004 of Mil-Std-883 Class B, Maxim's /HR program also provides full material traceability and process genealogy from incoming raw materials through final shipment. Additionally, Maxim performs Q.A. lot acceptance to an AQL of 0.1% and lot qualification emulating method 5005 (5008 for hybrids) of Mil-Std-883. Compliance with method 5005 (5008) was not required for ***Rev. B*** of Mil-Std-883, Class B per Mil-Std-217D quality level B2. A comparison between Maxim's /HR flow and ***Rev. B*** of Mil-Std-883, Class B is shown on the opposite page.

Devices processed to this program may be ordered by calling out the basic part number, followed by /HR (example IH5043MJE/HR). Lot qualification data (generic data) may be ordered separately at an additional cost. To order /HR devices, customers should contact the Maxim sales representatives or distributors.

Maxim /HR Flow
Hybrid Components

FULL MATERIAL TRACEABILITY AND PROCESS GENEALOGY

DEVICE ASSEMBLY

PRESEAL INTERNAL VISUAL
MIL-STD-883, METHOD 2017, CLASS B 100%

SEAL 100%

STABILIZATION BAKE
MIL-STD-883, METHOD 1008, CONDITION C 100%

TEMPERATURE CYCLING
MIL-STD-883, METHOD 1010, CONDITION C 100%

CONSTANT ACCELERATION
MIL-STD-883, METHOD 2001, CONDITION E (Y1 only 100%)*

FINE LEAK TEST
MIL-STD-883, METHOD 1014, CONDITION B 100%

GROSS LEAK TEST
MIL-STD-883, METHOD 1014, CONDITION C 100%

25°C ELECTRICAL TEST 100%

BURN IN
160 HOURS AT 125°C (OR EQUIVALENT) 100%

ELECTRICAL TEST
25°C, 125°C, -55°C 100%

QA ACCEPTANCE SAMPLE per APPLICABLE DEVICE SPEC

DC @ 25°C	AQL = 0.1%
DC @ Max °C	AQL = 0.1%
DC @ Min °C	AQL = 0.1%
Func @ 25°C	AQL = 0.1%
Func @ Min/Max °C	AQL = 0.1%
AC @ 25°C	AQL = 0.1%

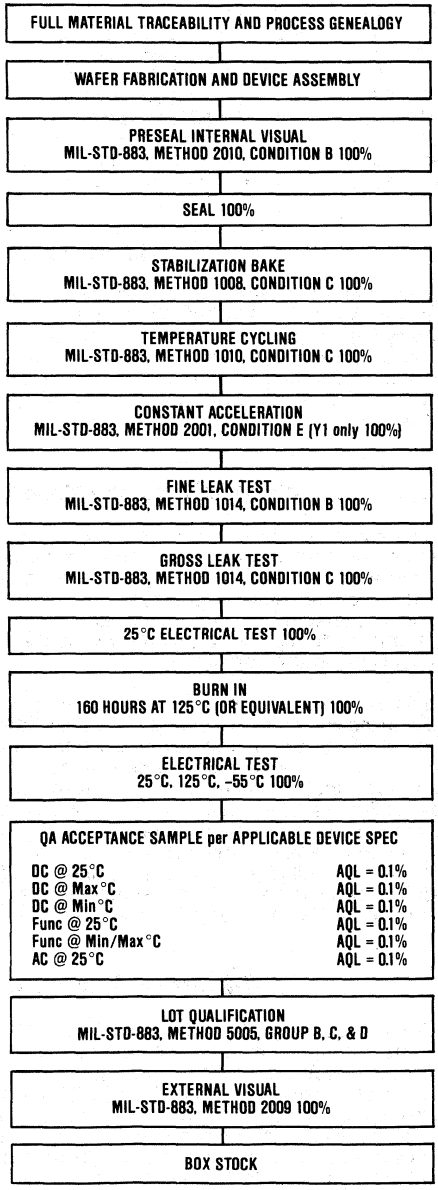
LOT QUALIFICATION
MIL-STD-883, METHOD 5008, GROUP B, C & D

EXTERNAL VISUAL
MIL-STD-883, METHOD 2009 100%

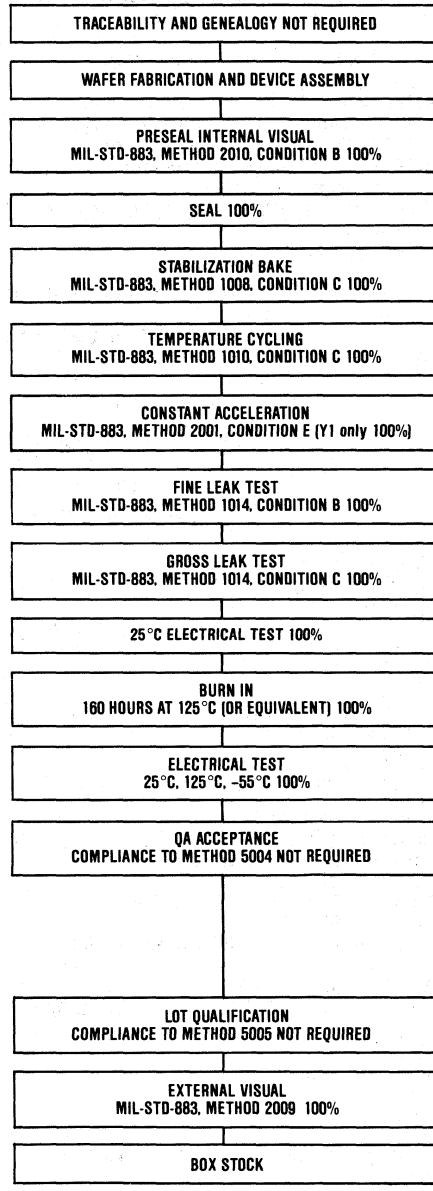
BOX STOCK

*If seal perimeter is greater than 2.0 inches, Condition A applies.

Maxim /HR Flow Monolithic ICs



Mil-Std-883, Class B, Rev. B Monolithic ICs (for comparison purposes only)



A

Proprietary and Second Source Numbering System

Maxim's Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped by their functions into certain categories. Maxim presently uses a "MAX" as the prefix to the device's unique number. The categories are as follows:

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op-Amps, Buffers and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power Supply Circuits and Voltage References
MAX700-799	µP Peripherals and Display Drivers
MAX800-899	Open
MAX900-999	Open

Within each category, blocks of numbers are reserved for sub-groups.

3 Letter Suffixes

EXAMPLE: MAX358CPD

- C — Lead Count
- P — Package Designator
- D — Operating Temperature

Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	TO-237
"C"	TO-220
"D"	Ceramic Sidebraze
"F"	Ceramic Flat-Pack
"H"	TO-66
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71)
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Z"	TO-92
"/D"	Dice
"/W"	Wafer
"-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8	"P"	20
"B"	10	"Q"	2
"C"	12	"R"	3
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44		
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32		
"K"	35	"Y"	8 (0.200" pin circle, case to pin 4)
"L"	40		
"M"	48	"Z"	10 (0.230" pin circle, case to pin 5)
"N"	18		

4 Letter Suffixes

The first letter of the suffix is used to denote product grade, for example, MAX631ACPA means 5% output accuracy (A), the remaining 3 letters denote temperature range, package type and number of leads. Therefore, the MAX631ACPA operates over the 0°C to +70°C and is in a Plastic Dual-in-Line package and has 8 leads.

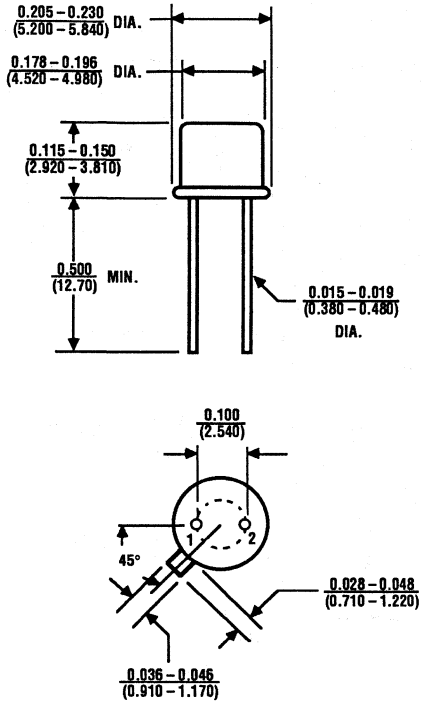
Second Source Products

In most cases, Maxim's part number for a multiple source product follows the numbering system that is most widely accepted in the industry for that particular part, rather than our own convention. This includes original designators for package type, temperature range, and performance grades as well as the most commonly recognized prefix.

Multiple source products are frequently supplied by Maxim in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, such a device is given the part number that it would have if the original numbering convention were followed. For example, if a military temperature grade of a product is not supplied by other sources but is available from Maxim, the original manufacturer's designation for military temperature will be used. As a result, a specific part number supplied by Maxim may not be listed by the "original" manufacturer.

Package Information

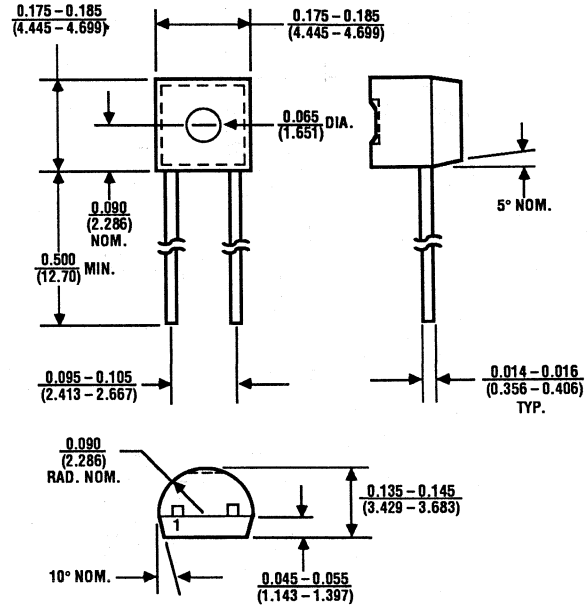
This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two letter code which indicates package type (Plastic DIP, Small Outline, etc.) and number of leads. This code is also used, along with indicators for temperature range and device grade (where appropriate) in the part number suffix for each of Maxim's proprietary devices.



TO-52 Metal Can – 2 Lead (SQ)

θ_{JA} = 220°C/W

θ_{JC} = 60°C/W

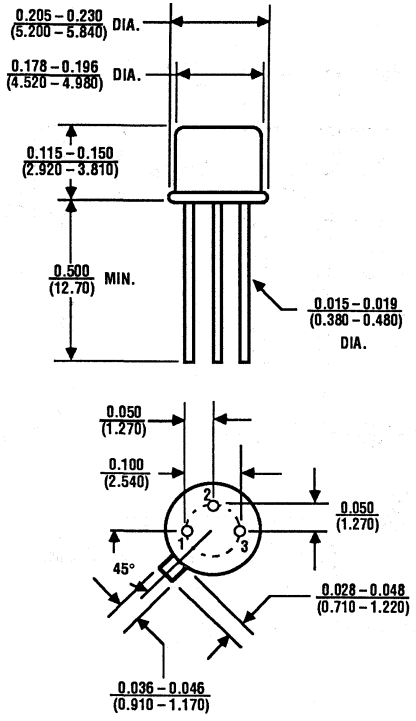


TO-92 Plastic – 2 Lead (ZQ)

θ_{JA} = 200°C/W

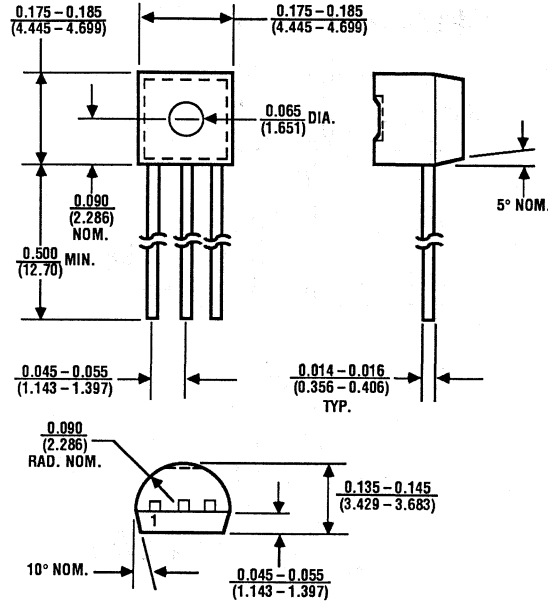
θ_{JC} = 70°C/W

A



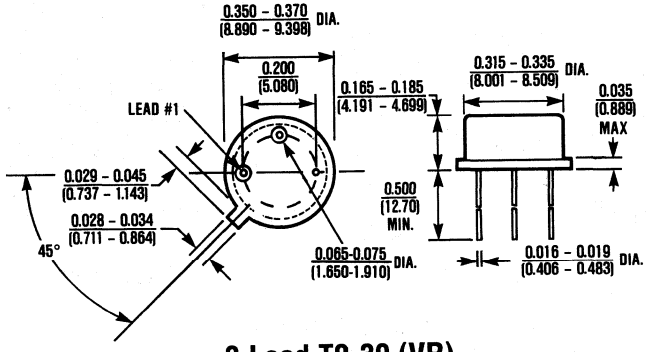
TO-52 Metal Can – 3 Lead (SR)

θ_{JA} = 220°C/W
θ_{JC} = 60°C/W



TO-92 Plastic – 3 Lead (ZR)

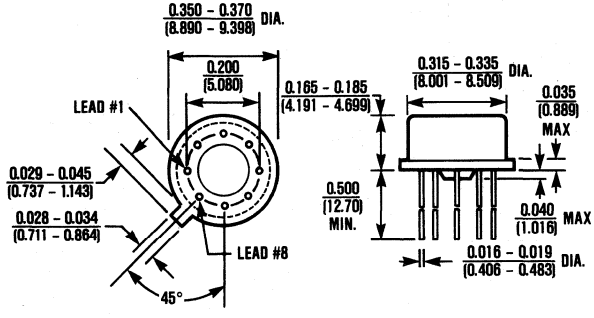
θ_{JA} = 200°C/W
θ_{JC} = 70°C/W



3 Lead TO-39 (VR)

θ_{JA} = 150°C/W

θ_{JC} = 15°C/W

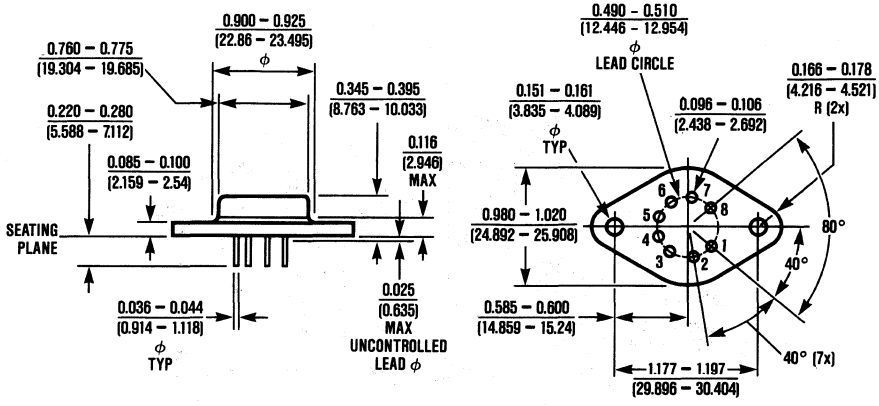


8 Lead TO-99 (TV)

θ_{JA} = 150°C/W

θ_{JC} = 45°C/W

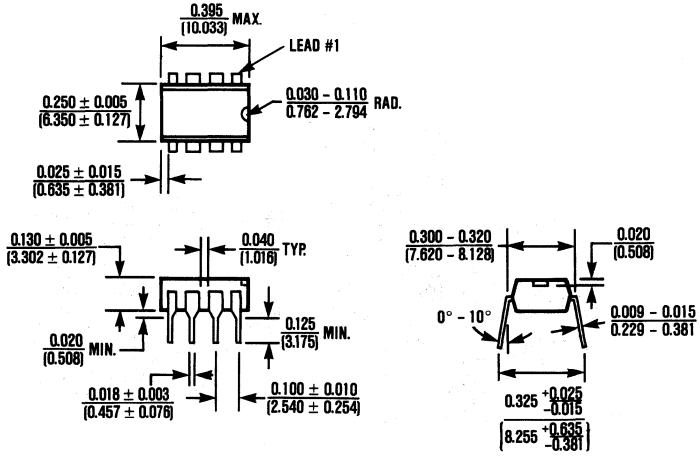
A



8 Lead TO-3 Can (KA)

θ_{JA} = 25°C/W

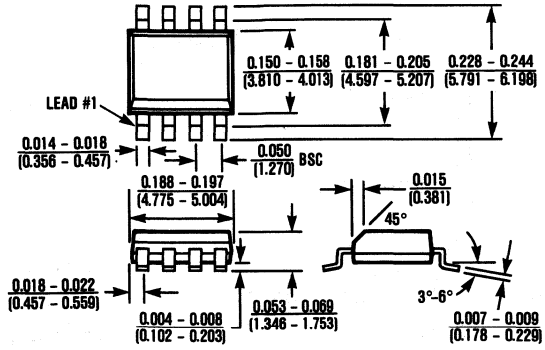
θ_{JC} = 2°C/W



8 Lead Plastic DIP (PA)

θ_{JA} = 160°C/W

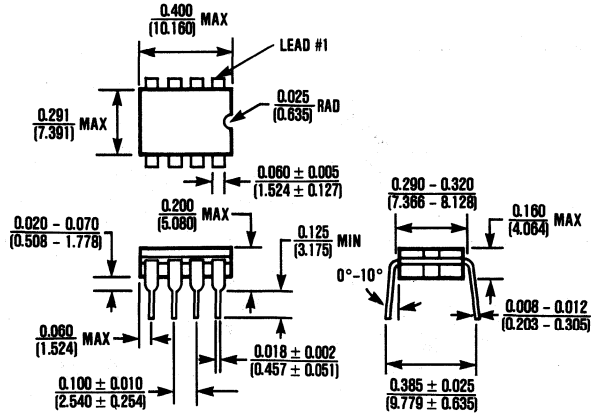
θ_{JC} = 75°C/W



8 Lead Small Outline (SA)

θ_{JA} = 170°C/W

θ_{JC} = 80°C/W

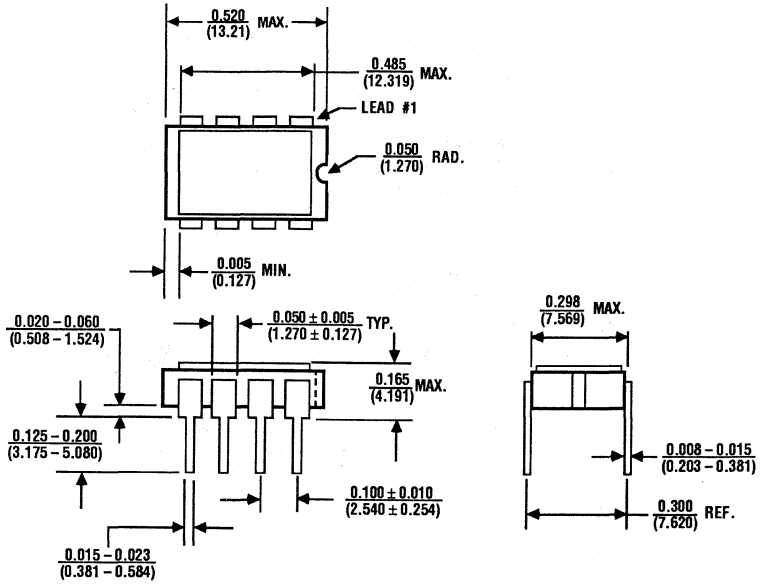


8 Lead CERDIP (JA)

θ_{JA} = 125°C/W

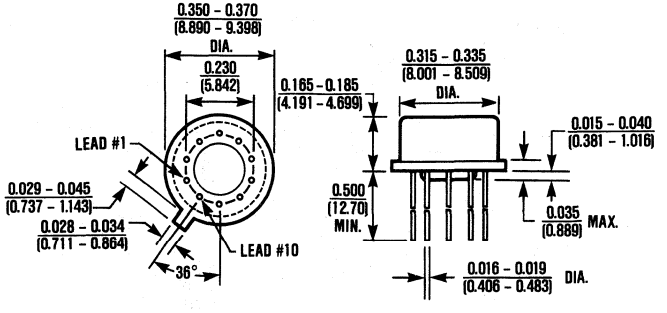
θ_{JC} = 55°C/W

A



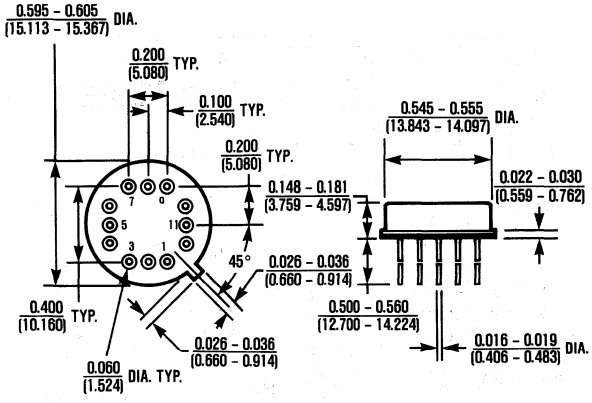
8 Lead Ceramic Sidebraze (DA)

θ_{JA} = 120°C/W
θ_{JC} = 50°C/W



10 Lead TO-100 Can (TW)

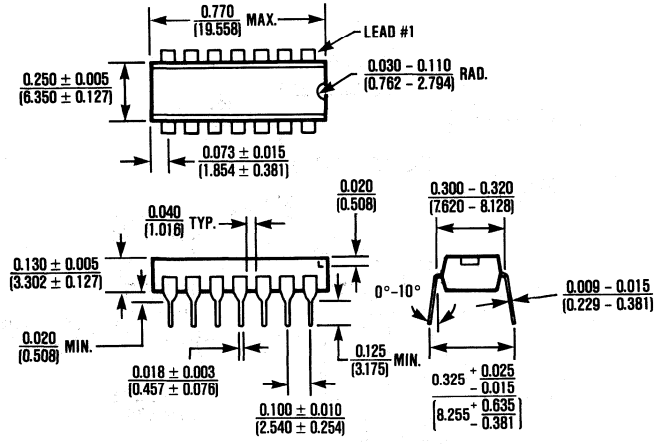
θ_{JA} = 150°C/W
θ_{JC} = 45°C/W



12 Lead TO-8 Can (G)

θ_{JA} = 100°C/W

θ_{JC} = 60°C/W

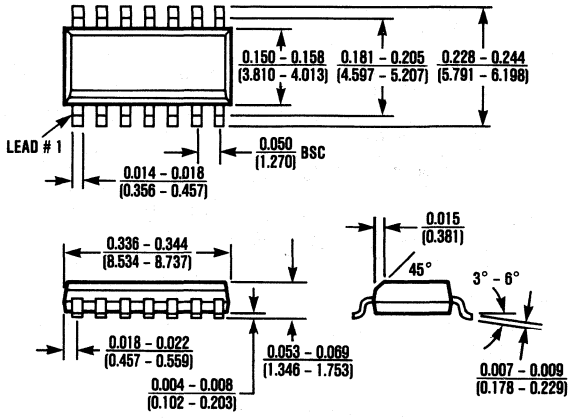


14 Lead Plastic DIP (PD)

θ_{JA} = 140°C/W

θ_{JC} = 70°C/W

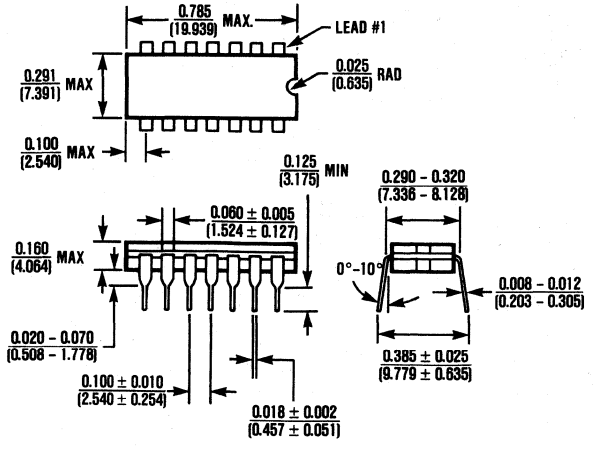
A



14 Lead Small Outline (SD)

θ_{JA} = 115°C/W

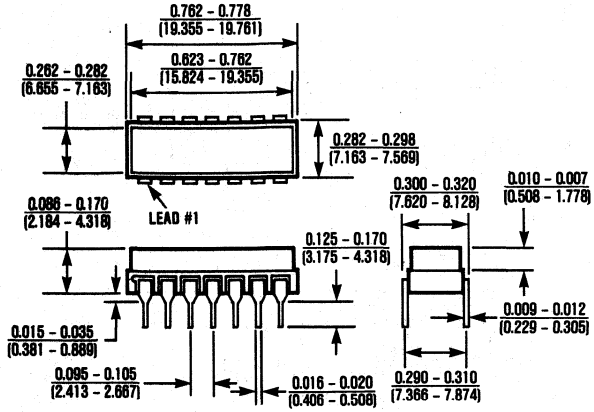
θ_{JC} = 60°C/W



14 Lead CERDIP (JD)

θ_{JA} = 105°C/W

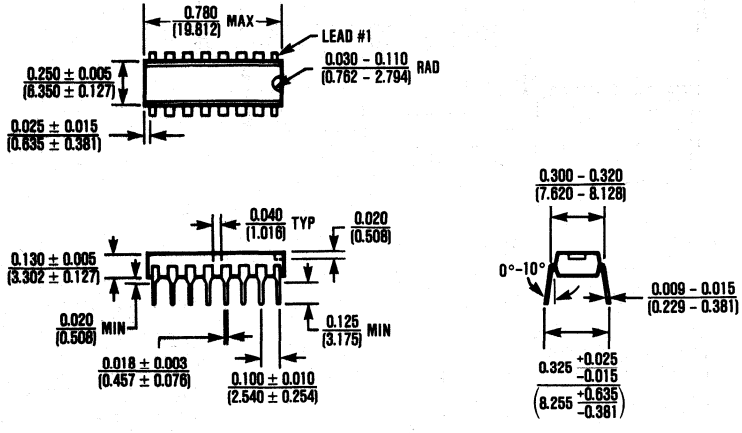
θ_{JC} = 50°C/W



14 Lead Ceramic Sidebraze (DD) -1

θ_{JA} = 100°C/W

θ_{JC} = 45°C/W

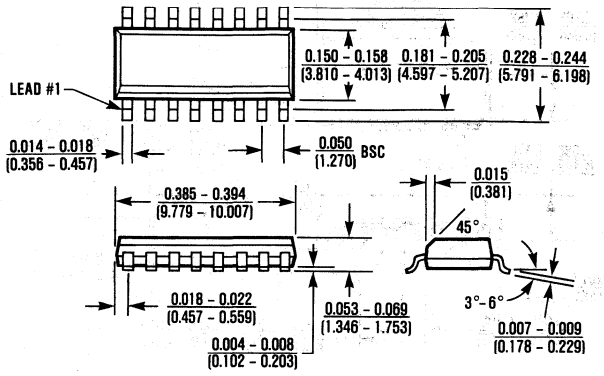


16 Lead Plastic DIP (PE)

θ_{JA} = 135°C/W

θ_{JC} = 65°C/W

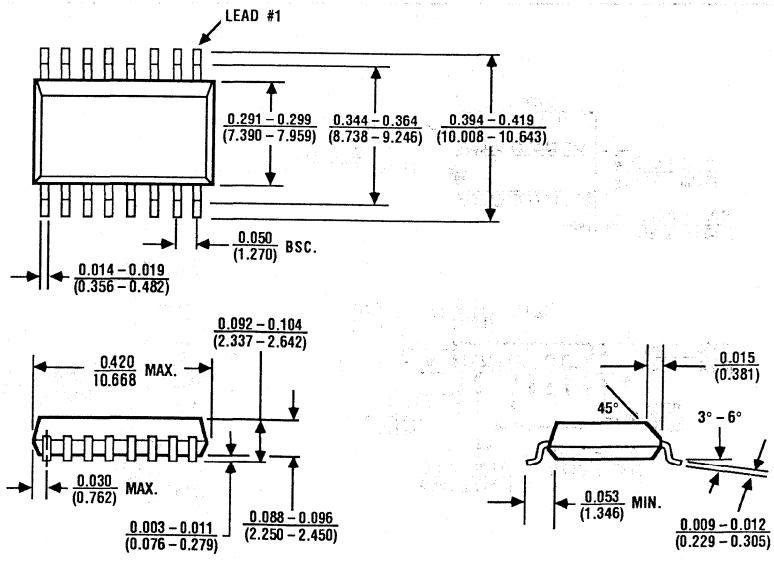
A



16 Lead Small Outline (SE)

θ_{JA} = 110°C/W

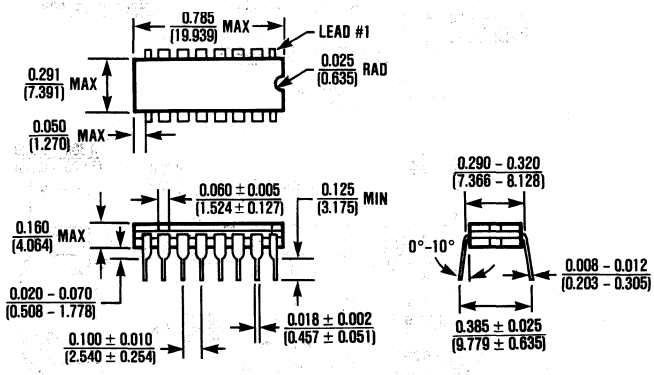
θ_{JC} = 60°C/W



16 Lead Small Outline, Wide (WE)

θ_{JA} = 105°C/W

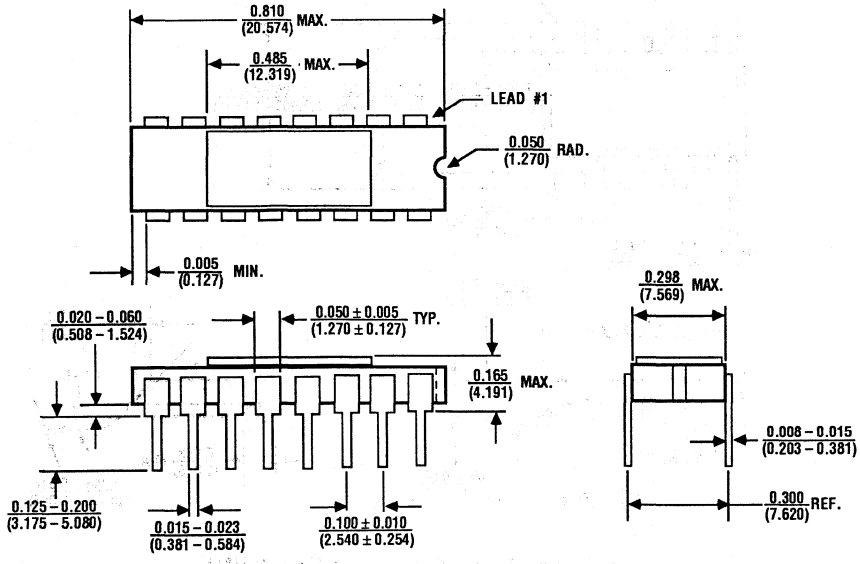
θ_{JC} = 60° C/W



16 Lead CERDIP (JE)

θ_{JA} = 100°C/W

θ_{JC} = 50°C/W

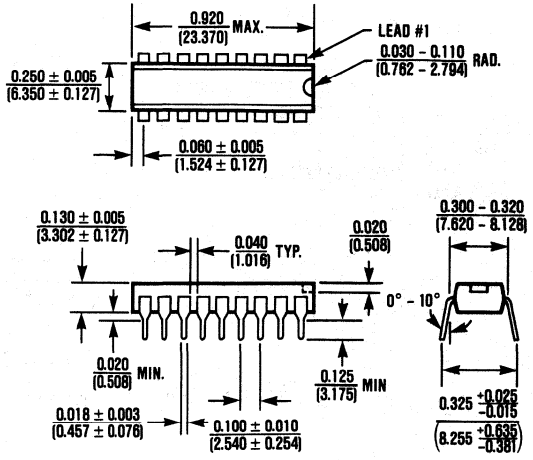


16 Lead Ceramic Sidebraze (DE)

θ_{JA} = 95°C/W

θ_{JC} = 45°C/W

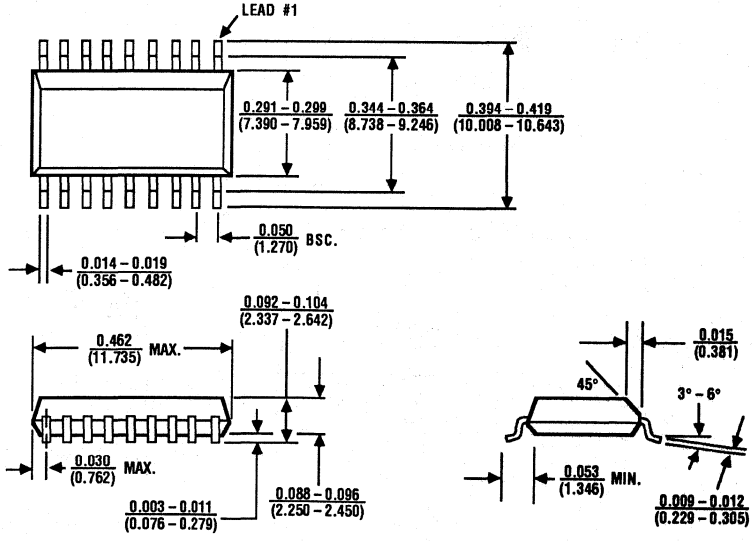
A



18 Lead Plastic DIP (PN)

θ_{JA} = 130°C/W

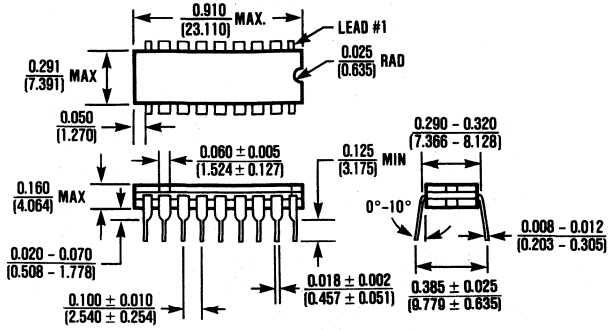
θ_{JC} = 60°C/W



18 Lead Small Outline, Wide (WN)

θ_{JA} = 105°C/W

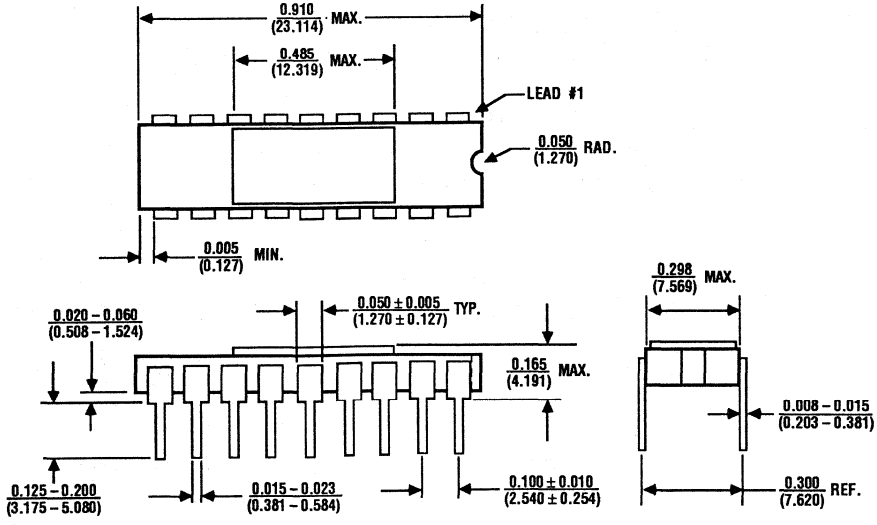
θ_{JC} = 60° C/W



18 Lead CERDIP (JN)

θ_{JA} = 90°C/W

θ_{JC} = 45°C/W

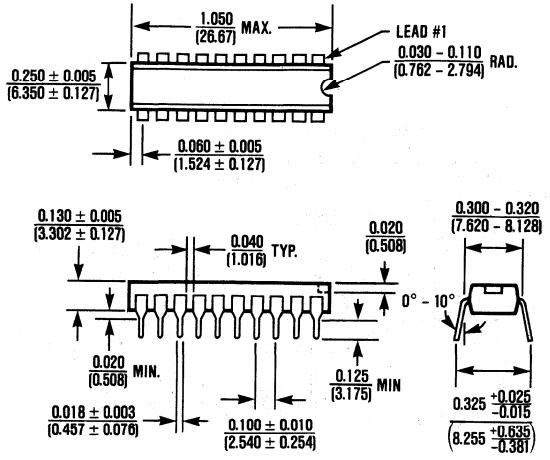


18 Lead Ceramic Sidebraze (DN)

θ_{JA} = 90°C/W

θ_{JC} = 40°C/W

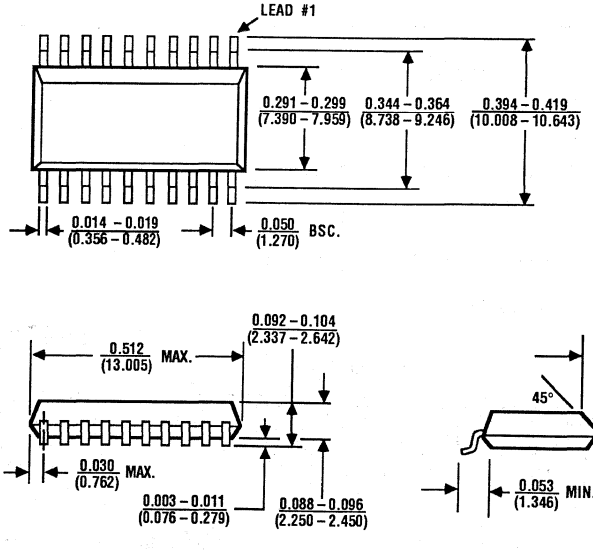
A



20 Lead Plastic DIP (PP)

θ_{JA} = 125°C/W

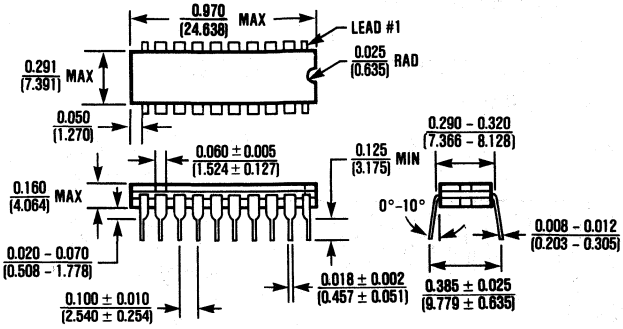
θ_{JC} = 60°C/W



20 Lead Small Outline, Wide (WP)

θ_{JA} = 100°C/W

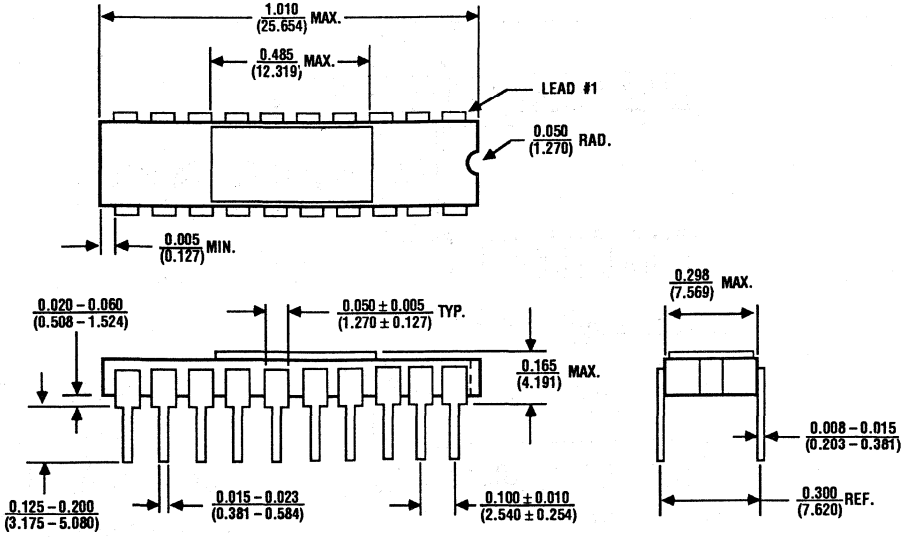
θ_{JC} = 50° C/W



20 Lead CERDIP (JP)

θ_{JA} = 90°C/W

θ_{JC} = 40°C/W

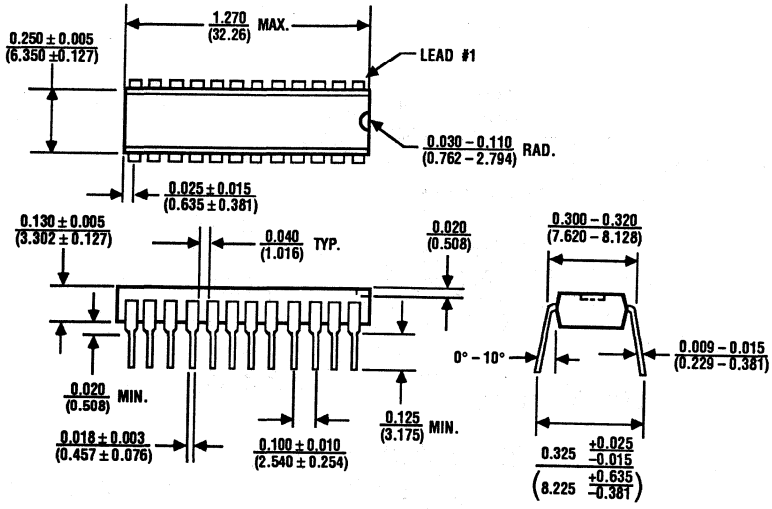


20 Lead Ceramic Sidebraze (DP)

θ_{JA} = 85°C/W

θ_{JC} = 35°C/W

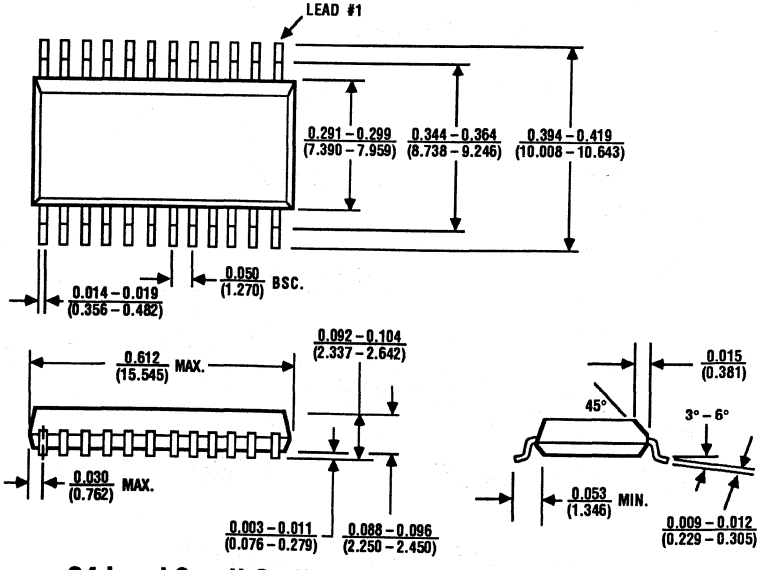
A



24 Lead Plastic Narrow DIP (NG)

θ_{JA} = 120°C/W

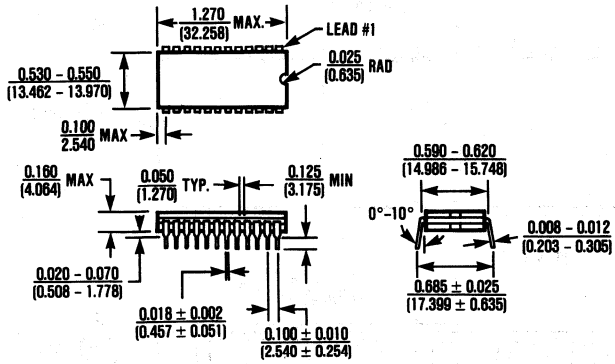
θ_{JC} = 60°C/W



24 Lead Small Outline, Wide (WG)

θ_{JA} = 85°C/W

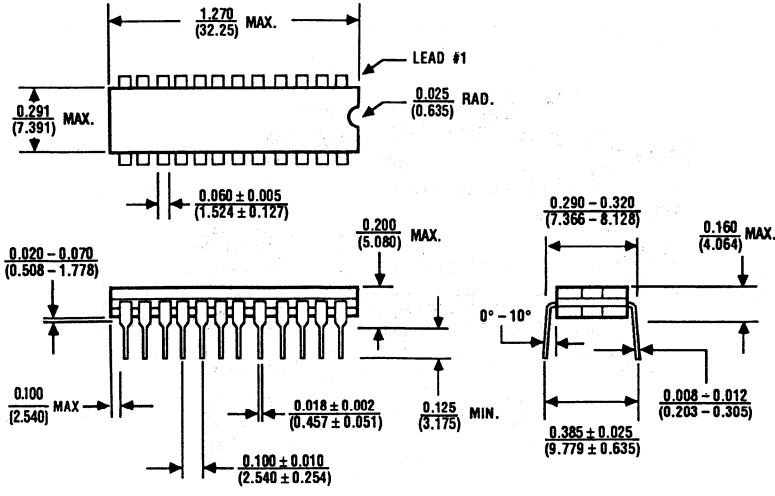
θ_{JC} = 45° C/W



24 Lead CERDIP (JG)

θ_{JA} = 55°C/W

θ_{JC} = 20°C/W

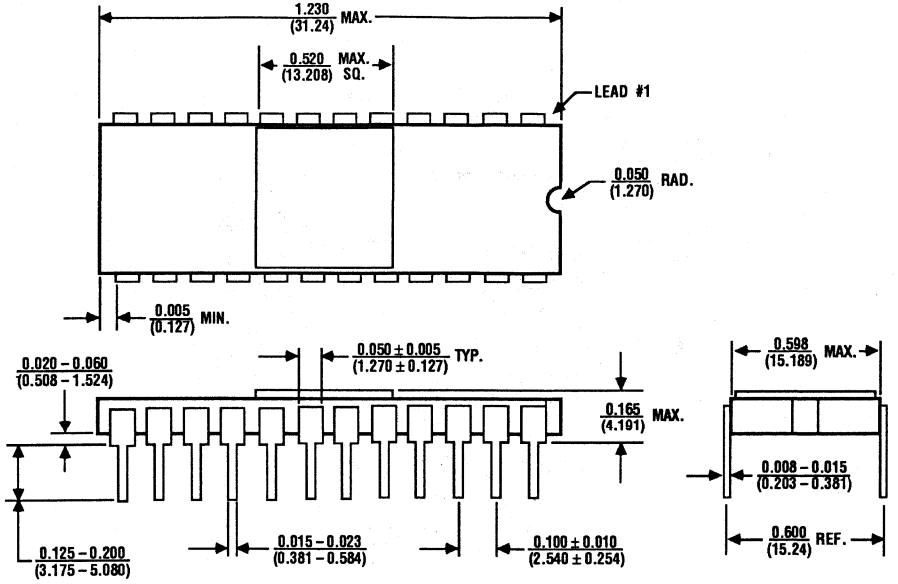


24 Lead Narrow CERDIP (RG)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W

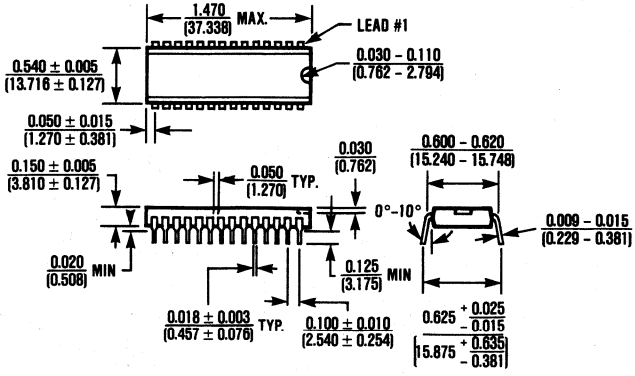
A



24 Lead Ceramic Sidebraze (DG)

θ_{JA} = 50°C/W

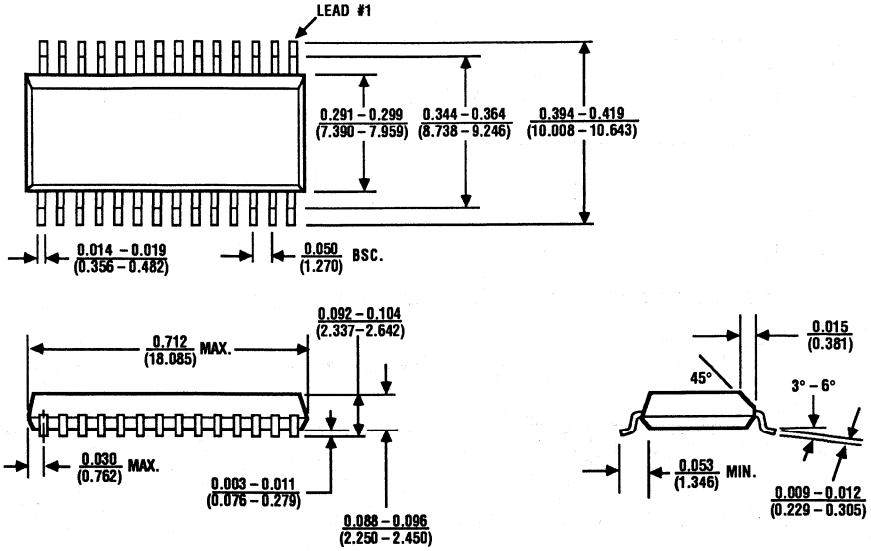
θ_{JC} = 15°C/W



28 Lead Plastic DIP (PI)

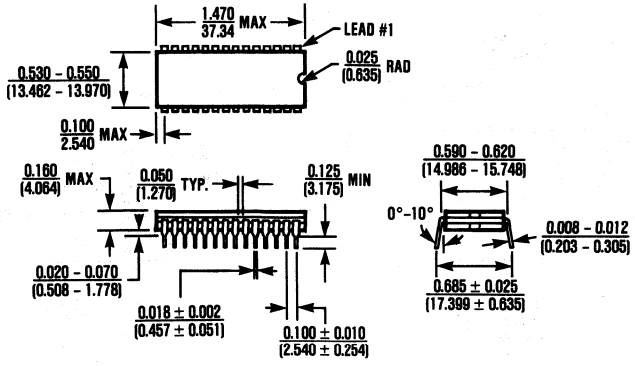
θ_{JA} = 110°C/W

θ_{JC} = 50°C/W



28 Lead Small Outline, Wide (WI)

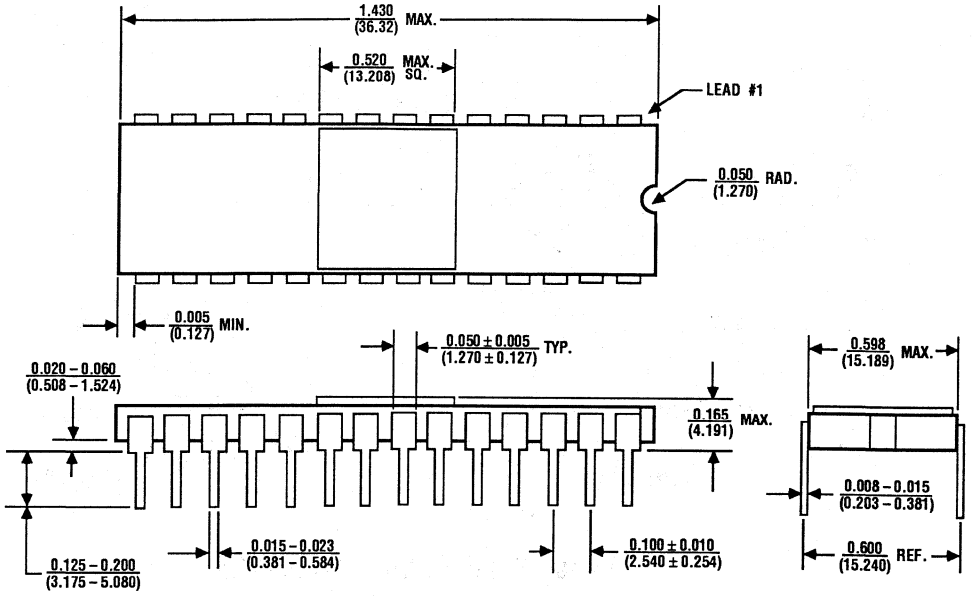
θ_{JA} = 80°C/W
θ_{JC} = 45°C/W



28 Lead CERDIP (JI)

θ_{JA} = 55°C/W
θ_{JC} = 20°C/W

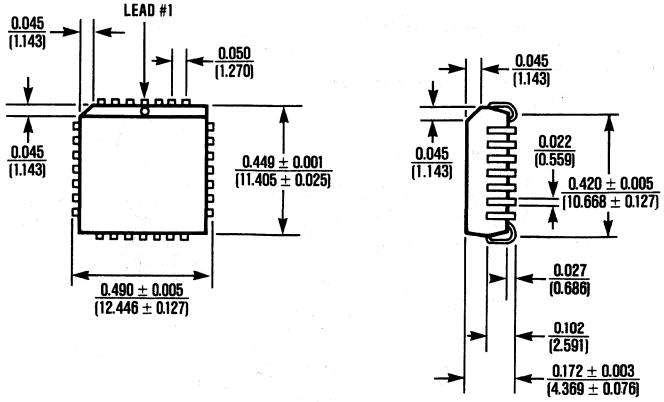
A



28 Lead Ceramic Sidebraze (DI)

θ_{JA} = 50°C/W

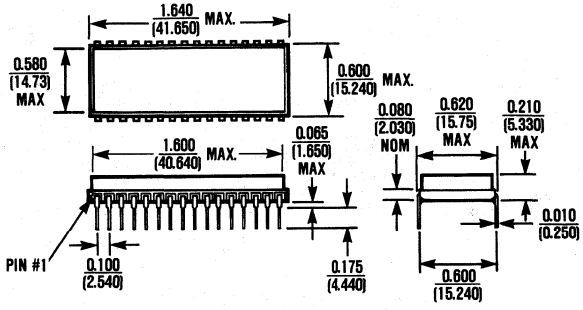
θ_{JC} = 15°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (QI)

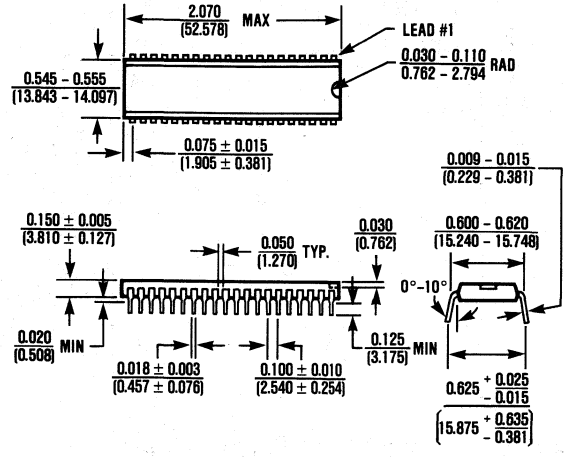
θ_{JA} = 100°C/W

θ_{JC} = 45°C/W



32 Lead Ceramic Sidebraze (DJ) -1

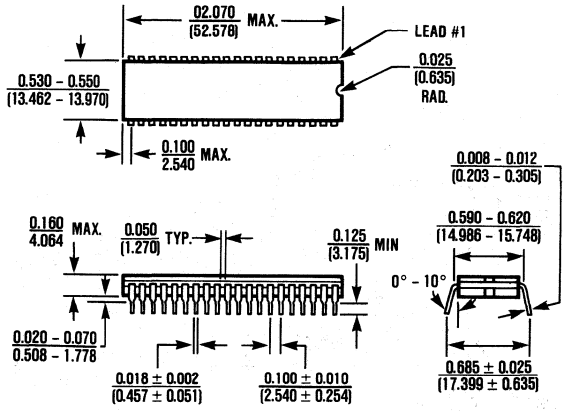
θ_{JA} = 7°C/W
θ_{JC} = 30°C/W



40 Lead Plastic DIP (PL)

θ_{JA} = 100°C/W
θ_{JC} = 45°C/W

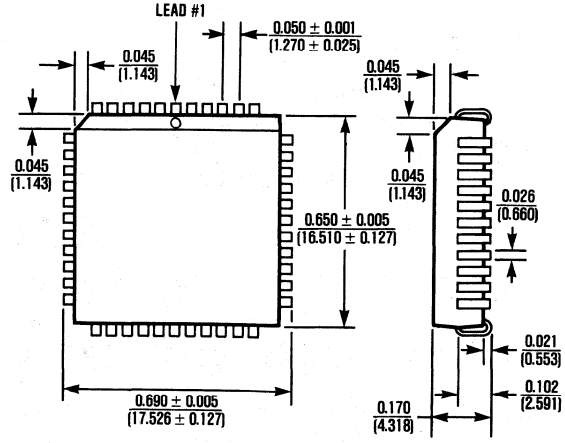
A



40 Lead CERDIP (JL)

θ_{JA} = 45°C/W

θ_{JC} = 20°C/W



44 Lead Plastic Chip Carrier (Quad Pak) (QH)

θ_{JA} = 80°C/W

θ_{JC} = 40°C/W

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Tel: (305) 428-8877
Telex: 510-955-9653
FAX: (305) 481-2950

Georgia

Bell Industries
3020 A Business Park Drive
Norcross, GA 30092
Tel: (404) 662-0923
FAX: (404) 449-6901

Hall-Mark Electronics
6410 Atlantic Blvd.
Suite 115
Norcross, GA 30071
Tel: (404) 447-8000
FAX: (404) 448-9654

Pioneer
3100 Northwoods Place
Suite F
Norcross, GA 30071
Tel: (404) 448-1711
Telex: 810-776-4515
FAX: (404) 446-8270

Illinois

Lionex/Anthem
180 Crossen Avenue
Elk Grove Village, IL 60007
Tel: (312) 640-6066
FAX: (312) 640-6302

Bell Industries
515 Busse Road
Elk Grove Village, IL 60007
Tel: (312) 640-1910
Telex: 910-223-4519
FAX: (312) 640-0474

Bell Industries
730 Killarney
Urbana, IL 61801
Tel: (217) 328-1077
FAX: (217) 328-1148

Hall-Mark Electronics
210 Mittel Drive
Wooddale, IL 60191
Tel: (312) 860-3800
FAX: (312) 860-0239

Pioneer
1551 Carmen Drive
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Tel: (312) 437-9680
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FAX: (312) 437-0551

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Fort Wayne, IN 46801
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Telex: 910-997-0701
FAX: (219) 424-2433

Bell Industries
5230 West 79th Street
Indianapolis, IN 46268
Tel: (317) 875-8200
FAX: (317) 875-8219

Hall-Mark Electronics
4275 W. 96th Street
Indianapolis, IN 46268
Tel: (317) 872-8875
FAX: (317) 876-7165

Pioneer
6408 Castleplace Drive
Indianapolis, IN 46250
Tel: (317) 849-7300
Telex: 810-260-1794
FAX: (317) 842-5998

Iowa
Bell Industries
1221 Park Place N.E.
Cedar Rapids, IA 52402
Tel: (319) 395-0730
Telex: 751-093
FAX: (319) 395-9761

Kansas
Hall-Mark Electronics
10809 Lakeview Drive
Lenexa, KS 66215
Tel: (913) 888-4747
FAX: (913) 888-0523

Pioneer
10551 Lackman Road
Lenexa, KS 66215
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FAX: (913) 492-7832

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9020A Mendenhall Court
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FAX: (301) 381-4379

Hall-Mark Electronics
10240 Old Columbia Road
Columbia, MD 21046
Tel: (301) 988-9800
FAX: (301) 381-2036

Pioneer
9100 Gaither Road
Gaitherburg, MD 20877
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FAX: (301) 921-4255

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Lionex/Anthem
36 Jonspin Road
Wilmington, MA 01887
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Bell Industries
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FAX: (617) 729-6839

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Telex: 710-348-0617
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44 Hartwell Avenue
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FAX: (617) 863-1547

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814 Phoenix Drive
Ann Arbor, MI 48104
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FAX: (313) 971-9178

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4505 Broadmoor Avenue, S.E.
Grand Rapids, MI 49508
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Telex: 510-600-8456
FAX: (616) 698-1831

Pioneer
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Hall-Mark Electronics
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FAX: (612) 941-5778

Pioneer
7625 Golden Triangle Drive
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Hall-Mark Electronics
13750 Shoreline Drive
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19 Park Avenue
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Tel: (603) 882-1133
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New Jersey
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311 Route 46 West
Fairfield, NJ 07006
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FAX: (201) 227-9246

Hall-Mark Electronics
107 Fairfield Road
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FAX: (609) 235-3381

Nu Horizons
258 Route 46
Fairfield, NJ 07006
Tel: (201) 882-8300
FAX: (201) 882-8398

Pioneer
45 Route 46
Pine Brook, NJ 07058
Tel: (201) 575-3510
Telex: 710-734-4382
FAX: (201) 575-3454

New Mexico
Bell Industries
11728 Linn N. E.
Albuquerque, NM 87123
Tel: (505) 292-2700
Telex: 910-989-0625
FAX: (505) 275-2819

New York
Lionex/Anthem
400 Oser Avenue
Hauppauge, NY 11787
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FAX: (516) 273-1823

Bell Industries
52 Central Drive
Farmingdale, NY 11735
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Hall-Mark Electronics
101 Comac Street
Ronkonkoma, NY 11779
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FAX: (516) 737-0838

Nu Horizons
6000 New Horizons Blvd.
Amityville, NY 11701
Tel: (516) 226-6000
FAX: (516) 226-6262

Nu Horizons
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Pioneer
840 Fairport Park
Fairport, NY 14450
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Telex: 510-253-7001
FAX: (716) 381-5955

New York (continued)
Pioneer
68 Corporate Drive
Binghamton, NY 13904
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Telex: 510-252-0893
FAX: (607) 722-9562

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60 Crossways Park West
Woodbury, NY 11797
Tel: (516) 921-8700
Telex: 510-221-2184
FAX: (516) 921-2143

Summit Distributors Inc.
916 Main Street
Buffalo, NY 14202
Tel: (716) 887-2800
Telex: 710-522-1692
FAX: (716) 887-2866

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Hall-Mark Electronics
5237 N. Boulevard
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FAX: (919) 878-8729

Pioneer
9801 A Southern Pine Blvd.
Charlotte, NC 28210
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Telex: 810-621-0366
FAX: (704) 522-8564

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Bell Industries
118 Westpark Drive
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FAX: (513) 434-8103

Bell Industries
444 Windsor Park Drive
Dayton, OH 45459
Tel: (513) 435-8660
Telex: 810-459-1615
FAX: (513) 435-6765

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5821 Harper Road
Solon, OH 44139
Tel: (216) 349-4632
FAX: (216) 248-4803

Hall-Mark Electronics
400 E. Wilson Bridge Rd., # S
Worthington, OH 43085
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FAX: (614) 888-0767

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4800 E. 131st Street
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FAX: (216) 587-3906

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Telex: 810-459-1622

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101 Rock Road
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FAX: (215) 675-9875

CAM-RPC Electronics
620 Alpha Drive
RIDC Park
Pittsburgh, PA 15238
Tel: (412) 782-3770
Telex: 4974222

Pioneer
261 Gibraltar Road
Horsham, PA 19044
Tel: (215) 674-4000
Telex: 510-665-6778
FAX: (215) 674-3107

Pioneer
259 Kappa Drive
Pittsburgh, PA 15238
Tel: (412) 782-2300
Telex: 710-795-3122
FAX: (412) 963-8255

Tennessee

Bell Industries
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FAX: (615) 367-4540

Texas

Hall-Mark Electronics
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Austin, TX 78727
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FAX: (512) 258-3777

Hall-Mark Electronics
11420 Pagemill Road
Dallas, TX 75243-5506
Tel: (214) 553-4300
FAX: (214) 553-4395

Hall-Mark Electronics
11333 Pagemill Road
P.O. Box 660091
Dallas, TX 75243
Tel: (214) 343-5000
FAX: (214) 343-5988

Hall-Mark Electronics
8000 Westglen
Houston, TX 77063
Tel: (713) 781-6100
FAX: (713) 953-8420

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1826 Kramer Lane
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Telex: 910-874-1323

Pioneer
13710 Omega Road
Dallas, TX 75244
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Telex: 910-860-5563
FAX: (214) 490-6419

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Pioneer
5853 Point West Drive
Houston, TX 77036
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Telex: 910-881-1606
FAX: (713) 988-1732

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Anthem
1279 West 2200 South
Salt Lake City, UT 84119
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FAX: (801) 973-8909

Bell Industries
3639 West 2150 South
Salt Lake City, UT 84120
Tel: (801) 972-6969
Telex: 910-925-5686
FAX: (801) 974-5739

Hall-Mark Electronics
2265 South 1300 West
West Valley City, UT 84119-1461
Tel: (801) 972-1008

Washington

Anthem
5020-148th Avenue N.E.
Redmond, WA 98052
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FAX: (206) 885-4041

Washington (continued)

Bell Industries
1900 132nd N.E.
Bellevue, WA 98005
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Telex: 910-443-2482
FAX: (206) 641-6082

Wisconsin

Bell Industries
W227 N913 Westmound Drive
Waukesha, WI 53186
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Telex: 910-265-3665
FAX: (414) 547-6547

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16255 W. Lincoln Avenue
New Berlin, WI 53151
Tel: (414) 797-7844
FAX: (414) 797-9259

Maxim U.S. Chip Distributors

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West Peabody Office Park
West Peabody, MA 01960
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Telex: 710-248-0423
FAX: (617) 535-1601

U.S. Hybrid Supply, Inc.

89 U.S. Route 1
Ipswich, MA 01938
Tel: (617) 356-7212
Telex: 710-321-9337
FAX: (617) 356-0749

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R & D Electronics Pty. Ltd.
4 Florence Street
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Australia
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Telex: (790) 33288 RADET
FAX: (03) 288-9168

R & D Electronics Pty. Ltd.
Ste. 2, 156 Great North Rd.
Five Dock, N.S.W. 2046
Sydney, Australia
Tel: (02) 712-3855
Telex: (790) 25468 SECCO
FAX: (02) 712-2507

Austria
Othmar Lackner
A-1031-WIEN
Landstr. Hauptstr. 37
Austria
Tel: (0222) 75 26 18
Telex: 111198
FAX: (0222) 75 26 185

Belgium
Master Chips
Saint Lazaruslaan 4
1210 Brussels, Belgium
Tel: (322) 195 862

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Tech-Trek
5050 Kings Way
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Burnaby
British Columbia V5H 4H2,
Canada
Tel: (604) 439-1373
FAX: (604) 439-1367

Tech-Trek Ltd.
1015 Matheson Blvd.
Unit #6
Mississauga
Ontario L4W 3A4, Canada
Tel: (416) 238-0366
FAX: (416) 238-0319

Tech-Trek
148 Colonnade Road
Unit 13
Nepean
Ontarioa K2E 7R4, Canada
Tel: (613) 225-5161
FAX: (613) 723-1426

Tech-Trek
7033 Trans-Canada Hwy.
Suite 202
Ville St. Laurent
Quebec H4T 1S2, Canada
Tel: (514) 337-7540
FAX: (514) 337-7544

Canada/Distributors
Future Electronics
239 Hymus Blvd.
Pointe Claire
Quebec H9R 5C7, Canada
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Telex: 05-823-554/9
610-421-3251
FAX: (514) 695-3707

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Future Electronics
Baxter Centre
1050 Baxter Road
Ottawa
Ontario K2C 3P2, Canada
Tel: (613) 820-8313
FAX: (613) 820-3271

Future Electronics
82 St. Regis Crescent N.
Downsview
Ontario M3J 1Z3, Canada
Tel: (416) 638-4771
FAX: (416) 638-2936

Future Electronics
106 King Edwards St., East
Winnipeg
Manitoba R3H 0N8, Canada
Tel: (204) 786-7711

Future Electronics
3220 5th Avenue, N.E.
Calgary
Alberta T2A 5N1, Canada
Tel: (403) 235-5325
FAX: (403) 294-1206

Future Electronics
1695 Boundary Road
Vancouver
British Columbia V5K 4X7,
Canada
Tel: (604) 294-1166
FAX: (604) 294-1206

Future Electronics
5312 Calgary Trail S.
Edmonton
Alberta T6H 4J8, Canada
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FAX: (403) 484-7103

Zentronics
8 Tilbury Court
Brampton
Ontario L6T 3T4, Canada
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FAX: (416) 451-8320

Zentronics
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Alberta T2A 6J4, Canada
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Zentronics
817 McCaffrey Street
Ville St. Laurent
Quebec H4T 1N3, Canada
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FAX: (514) 737-5212

Zentronics
155 Colonnade Road South
Units 17 & 18
Nepean
Ontario K2E 7K1, Canada
Tel: (613) 226-8840
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Zentronics
93-1313 Border
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Manitoba R3H 0X4, Canada
Tel: (204) 694-1957
FAX: (204) 633-9255

Canada/Distributors (continued)
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173-1222 Alberta Avenue
Saskatoon
Saskatchewan S7K 1R4,
Canada
Tel: (306) 955-2202
FAX: (306) 244-3731

Zentronics
11400 Bridgeport Road
Unit 108
Richmond
British Columbia V6X 1T2,
Canada
Tel: (640) 273-5575

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Exatec
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Exatec
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Th. Eriksensvej 18 H
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Telex: (042) 698-376F
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Franelec
Z.I Les Glaises
6-8 Rue Ambroise Croizat
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Hong Kong
Tektron Elect. (HK Ltd.)
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636 Nathan Road
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Dynatek Electronics Limited
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Hong Leong Industrial
Complex
4 Wang Kwong Street
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India
Contact Factory

Israel
Vectronics
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00141 Rome, Italy
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FAX: (06) 82 75 270

Italy/Distributors
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20099 Sesto San Giovanni
(Milano)
Via Modena 1, Italy
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Telex: (843) 32-2383
FAX: (02) 240-9255

Esco Italiana
Bologna, Italy
Tel: (051) 32 30 42

Esco Italiana
Roma, Italy
Tel: (068) 39 56 48

Esco Italiana
Torino, Italy
Tel: (011) 20 51 384

Esco Veneto S.R.L.
36100 Vicenza
Viale Mazzini 131, Italy
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Japan/Distributors
Internix, Inc.
7-4-7 Nishi-shinjuku,
Shinjuku-Ku
Tokyo 160, Japan
Tel: (03) 369-1101
Telex: (781) J26733
FAX: (03) 366-8566

Microtek, Inc.
Itoh Bldg.
9-7-17 Nishi-Shinjuku
7-Chome
Shinkjuku-Ku
Tokyo 160, Japan
Tel: (03) 363-2317, 371-1811
Telex: (781) J27466
FAX: (03) 369-5623

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6-7, Nakamachi 1-Chome
Musashino-Shi,
Tokyo 180, Japan
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Sil-Walker, Inc.
Royal Bldg., 1-1
Shinjuku 5-Chome
Shinjuku-Ku,
Tokyo 160, Japan
Tel: (03) 341-3651
Telex: 02323398 Silwkr J
FAX: (03) 341-3974

Korea
J-Tek Corp.
6th Fl. Government Pension Bldg.
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Young Dung Po-Ku
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Tel: (78) 28 039
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Netherlands
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FAX: (31) 041 89 18 72

New Zealand
Bell irh Components
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Glenfield
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Nordisk Elektronik (Norge) A/S
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1364 Hvalstad, Norway
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FAX: (02) 84 65 45

Singapore
Desner Elect. (Far East)
PTE Ltd.
190 Middle Road #16-07
Fortune Centre
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On Board Electronics Ltd.
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Telex: 847575
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Spezial-Electronic KG
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Spezial-Electronic KG
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